PHILIPS

Data handbook

Electronic components and materials

Components and materials

Part 1 November 1975

Functional units

Input/output devices

Peripheral devices

COMPONENTS AND MATERIALS

Part 1 **November 1975**

DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, subassemblies and materials; it is made up of three series of handbooks each comprising several parts.

ELECTRON TUBES	**BLUE**
SEMICONDUCTORS AND INTEGRATED CIRCUITS	**RED**
COMPONENTS AND MATERIALS	**GREEN**

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

December 1972

ELECTRON TUBES (BLUE SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1a Transmitting tubes for communications and Tubes for r.f. heating Types PB2/500 ÷ TBW15/125 — **April 1973**

Part 1b Transmitting tubes for communication
Tubes for r.f. heating
Amplifier circuit assemblies — **August 1974**

Part 2 Microwave products — **October 1974**

Communication magnetrons
Magnetrons for microwave heating
Klystrons
Travelling-wave tubes
Diodes
Triodes
T-R Switches
Microwave Semiconductor devices
Isolators Circulators

Part 3 Special Quality tubes;
Miscellaneous devices — **January 1975**

Part 4 Receiving tubes — **March 1975**

Part 5a Cathode-ray tubes — **April 1975**

Part 5b Camera tubes; Image intensifier tubes — **May 1975**

Part 6 Products for nuclear technology — **July 1975**
Photodiodes
Neutron tubes
Channel electron multipliers
Geiger-Mueller tubes
N.B. Photomultiplier tubes and Photo diodes will be issued in Part 9

Part 7 Gas-filled tubes — **August 1975**

Voltage stabilizing and reference tube
Counter, selector, and indicator tubes
Trigger tubes
Switching diodes
Thyratrons
Ignitrons
Industrial rectifying tubes
High-voltage rectifying tubes

Part 8 TV Picture tubes — **October 1975**

SEMICONDUCTORS AND INTEGRATED CIRCUITS (RED SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1a **Rectifier diodes and thyristors** — **June 1974**

Rectifier diodes
Voltage regulator diodes (> 1,5 W)
Transient suppressor diodes
Thyristors, diacs, triacs
Rectifier stacks

Part 1b **Diodes** — **October 1975**

Small signal germanium diodes
Small signal silicon diodes
Special diodes
Voltage regulator diodes (< 1,5 W)
Voltage reference diodes
Tuner diodes

Part 2 **Low frequency transistors** — **July 1974**

Part 3 **High frequency and switching transistors** — **October 1974**

Part 4a **Special semiconductors** — **November 1974**

Transmitting transistors
Microwave devices
Field-effect transistors
Dual transistors
Microminiature devices for thick- and thin-film circuits

Part 4b **Devices for opto-electronics** — **December 1974**

Photosensitive diodes and transistors
Light emitting diodes
Photocouplers
Infra-red sensitive devices
Photoconductive devices

Part 5 **Linear integrated circuits** — **March 1975**

Part 6 **Digital integrated circuits** — **April 1974**

DTL (FC family)
CML (GX family)
MOS (FD family)
MOS (FE family)

COMPONENTS AND MATERIALS (GREEN SERIES)

These series consists of the following parts, issued on the dates indicated.

Part 1 Functional units, Input/output devices, Peripheral devices — **November 1975**

- High noise immunity logic FZ/30-Series
- Circuit blocks 40-Series and CSA70
- Counter modules 50-Series
- Norbits 60-Series, 61-Series
- Circuit blocks 90-Series
- Input/output devices
- Hybrid integrated circuits
- Peripheral devices

Part 2a Resistors — **September 1974**

- Fixed resistors
- Variable resistors
- Voltage dependent resistors (VDR)
- Light dependent resistors (LDR)
- Negative temperature coefficient thermistors (NTC)
- Positive temperature coefficient thermistors (PTC)
- Test switches

Part 2b Capacitors — **November 1974**

- Electrolytic and solid capacitors
- Paper capacitors and film capacitors
- Ceramic capacitors
- Variable capacitors

Part 3 Radio, Audio, Television — **February 1975**

- FM tuners
- Loudspeakers
- Television tuners, aerial input assemblies
- Components for black and white television
- Components for colour television

Part 4a Soft ferrites — **April 1975**

- Ferrites for radio, audio and television
- Beads and chokes
- Ferroxcube potcores and square cores
- Ferroxcube transformer cores

Part 4b Piezoelectric ceramics, Permanent magnet materials — **May 1975**

Part 5 Ferrite core memory products — **July 1975**

- Ferroxcube memory cores
- Matrix planes and stacks
- Core memory systems

Part 6 Electric motors and accessories — **September 1975**

- Small synchronous motors
- Stepper motors
- Miniature direct current motors

Part 7 Circuit blocks — **September 1971**

- Circuit blocks 100 kHz-Series
- Circuit blocks 1-Series
- Circuit blocks 10-Series
- Circuit blocks for ferrite core memory drive

Part 8 Variable mains transformers — **July 1975**

Part 10 Connectors — **November 1975**

HNIL FZ/30-Series

High noise immunity logic

HIGH NOISE IMMUNITY LOGIC

INTRODUCTION

In noisy environments - in data handling and processing, in industrial control, in computer peripherals - you need High Noise Immunity Logic. You need the FZ/30-Series. It gives you a comprehensive range of logic elements - plus such indispensable ancillaries as timers, power amplifiers, lamp or relay drive modules, and interface modules. And they have one outstanding advantage, by adding a capacitor you can slow-down the system response and raise the a.c. noise threshold to meet your needs.

The modules are small, over a hundred would fit on this page, and have an operating temperature range up to 70 °C. Wide voltage tolerances make these circuits first choice for a host of industrial and professional applications. And they're easy to use - a simple loading table tells you what each unit can drive, and what's needed to drive it. And we supply a full set of bits to go round them - input/output devices - printed-wiring boards - connectors - sticker symbols - name it - its in the FZ/30-Series range of auxiliaries.

Check with us for full details of the FZ/30-Series. You get fast, reliable deliveries, attractive quotations, and an applications service that is second to none.

SURVEY OF TYPES

type	description	catalogue number
FZH101/4.NAND32	Quad 2-input NAND gate	2722 006 01081
FZH111/4.NAND30	Quad 2-input NAND gate Two gates can be slowed down	2722 006 01001
FZH121/2.NAND30	Dual 5-input NAND gate	2722 006 01061
FZH131/2.NAND31	Dual 5-input NAND gate Both gates can be slowed down	2722 006 01011
FZH141/2.NAND32	Dual 5-input power NAND gate Both gates can be slowed down	2722 006 01021
FZH151/2.AOR30	Dual 5-input AND-AND-OR gate One gate can be slowed down	2722 006 02001
FZH161/4.LI31	Quad logic interface gate HNIL to 5 V logic; all gates can be slowed down	2722 006 04011
FZH171/2.NAND33	Dual 4-input NAND gate With expandable inputs; both gates can be slowed down	2722 006 01091

SURVEY OF TYPES (continued)

type	description	catalogue number
FZH181/4.LI30	Quad logic interface gate 5 V logic to HNIL	2722 006 04001
FZH191/3.NAND33	Triple 3-input NAND gate Two gates can be slowed down	2722 006 01031
FZH201/6.IN30	Sextuple inverter with strobe input	2722 006 07001
FZH211/4.NAND34	Quad 2-input NAND gate Two gates can be slowed down, outputs have open collectors	2722 006 01041
FZH231/2.NAND35	Dual 5-input NAND gate Both outputs can be slowed down, outputs have open collectors	2722 006 01051
FZH241/2.AST30	Dual 4-input NAND Schmitt trigger with expandable inputs; output can be slowed down	2722 006 12001
FZH251/4.AND30	Quad 2-input AND gate Two gates can be slowed down	2722 006 13001
FZH261/2.N-4.I30	Dual NAND gate/quad inverter	2722 006 08001
FZH271/4.EO30	Quad EXCLUSIVE-OR gate Two gates can be slowed down	2722 006 11001
FZH281/4.NOR30	Quad NOR gate Two gates can be slowed down	2722 006 10001
FZH291/4.OR30	Quad OR gate Two gates can be slowed down	2722 006 09001
FZJ101/FF30	Single JK flip-flop Slave can be slowed down	2722 006 00001
FZJ111/FF31	Single JK flip-flop Master and slave can be slowed down	2722 006 00011
FZJ121/2.FF32	Dual JK master-slave flip- flop	2722 006 00021
FZJ131/4.FF33	Quad D-type latch flip-flop	2722 006 00031

SURVEY OF TYPES (continued)

type	description	catalogue number
FZJ141/FF34	Single synchronous decimal counter Has parallel-set and common reset inputs	2722 006 00041
FZJ151/FF35	Single synchronous 4-bit binary counter. Has parallel-set and common reset inputs	2722 006 00051
FZJ161/FF36	Single synchronous 4-bit shift register. Two gates can be slowed down	2722 006 00061
FZK101/OS30	Single monostable multivibrator Input can be slowed down	2722 006 03001
FZL101/ND30	Single BCD-decimal decoder numerical indicator tube driver	2722 006 06021
2.LRD30	Dual lamp/relay driver Can be slowed down	2722 006 06011
PA30	Power amplifier Can be slowed down	2722 006 00091
TU30	Single timer unit	2722 006 05001

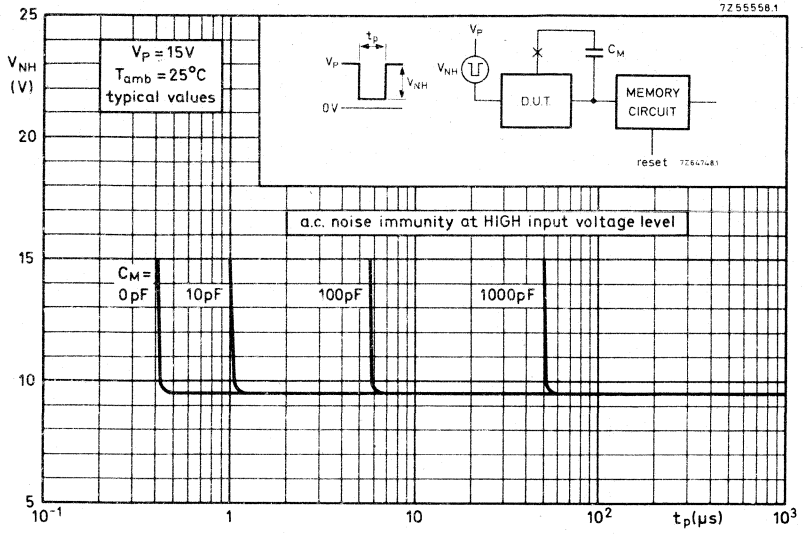
MAIN CHARACTERISTICS

Operating ambient temperature			0 to +70	°C	
Storage temperature			−25 to +85	°C	
Package outline			dual in-line		
Supply voltage : range I			12 $^{+12\frac{1}{2}\%}_{-5\%}$	V	1)
range II			15 $^{+13\%}_{-10\%}$	V	1)
Power consumption (per gate)	typ.		30	mW	
(per flip-flop)	typ.		165	mW	
Counting rate (flip-flops) can be slowed down	<		500	kHz	
Fan-out (in gate loads) : NAND gates and flip-flops	N_{aL}		10		
POWER-NAND gates	N_{aL}		30		
for all units	N_{aH}		100		
Propagation delay : (gates)	typ.		150	ns	2)
(flip-flops)	typ.		430	ns	2)
Output short circuit duration non-repetitive value	$t_{Q_{sc}}$	max.	1	s	3)
D.C. noise margin	typ.		5	V	
A.C. noise threshold (With an external capacitor the response time of a function can be slowed down, resulting in an increased a.c. noise threshold.)			see curves next page		

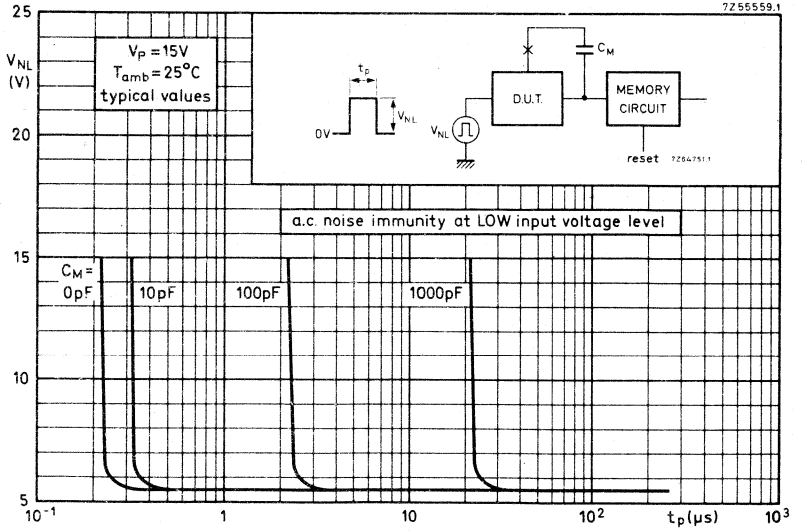
1) Voltage steps within the specified supply limits are allowed.

2) Can be increased to raise a.c. noise threshold.

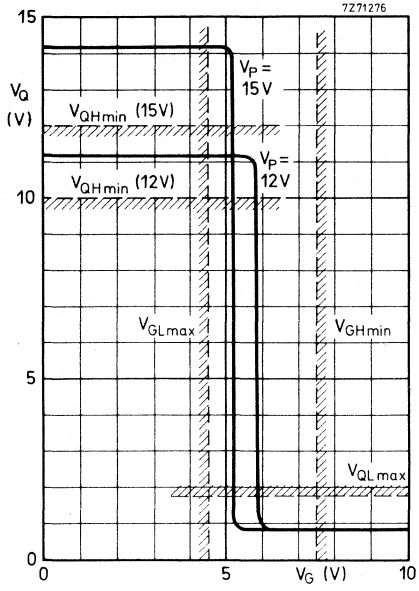
3) Only one output may be shorted at a time.

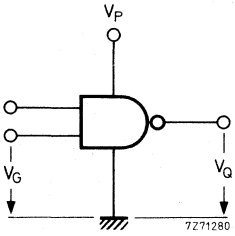


Typical curves for HIGH-input voltage level.

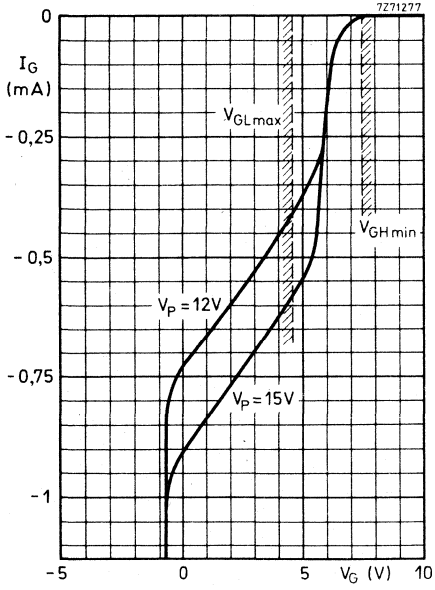


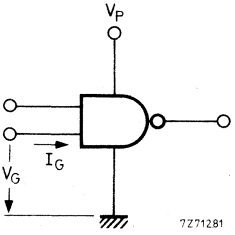
Typical curves for LOW-input voltage level.



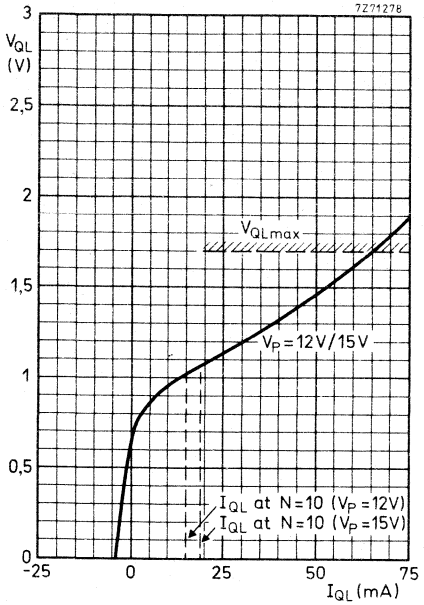


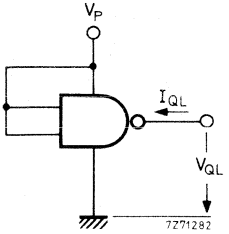
Typical transfer function of NAND gates at V_P = 12 V and V_P = 15 V.



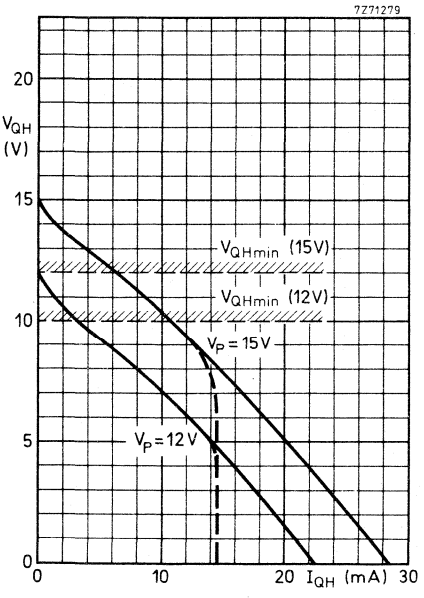


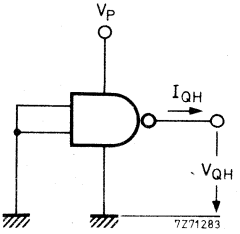
Typical input characteristic of NAND gates.





Typical output characteristic of the LOW-state outputs at V_P = 12 V, 15 V.





Typical output characteristic of the HIGH-state
—— FZH101 to FZH171, FZJ101 and FZJ111
---- FZH191 to FZH291, FZJ121 to FZJ161, and FZK101.

LOADING TABLE (T_{amb} = 0 to +70 °C; V_P = 15 V)

type	function	input (D.U.)		output (D.U.)	
		terminal	required	terminal	available
FZH101/4.NAND32	Quad 2-input NAND	G_1 - G_8	1	Q_1 - Q_4	10
FZH111/4.NAND30	Quad 2-input NAND	G_1 - G_8	1	Q_1 - Q_4	10
FZH121/2.NAND30	Dual 5-input NAND	G_1 - G_{10}	1	Q_1 ; Q_2	10
FZH131/2.NAND31	Dual 5-input NAND	G_1 - G_{10}	1	Q_1 ; Q_2	10
FZH141/2.NAND32	Dual 5-input power NAND	G_1 - G_{10}	1	Q_1 ; Q_2	30
FZH151/2.AOR30	Dual AND-AND-OR	G_2, G_3, G_9, G_{10}	1, 5	Q_1 ; Q_2	16
		other gates	1		
FZH161/4.LI31	Quad logic interface HNIL to 5 V logic	G_2 - G_5	1	Q_1 - Q_4	$V_{QL} \leq 0,4$ V I_{QL} = 20 mA V_P = 13,5 V
		G_1, G_6	2		
FZH171/2.NAND33	Dual 4-input NAND	G_1 - G_8	1	Q_1 ; Q_2	10
FZH181/4.LI30	Quad logic interface 5 V to HNIL	G_1 - G_8	1	Q_1 - Q_4	27
FZH191/3.NAND33	Triple 3-input NAND	G_1 - G_9	1	Q_1 - Q_3	10
FZH201/6.IN30	Sextuple inverter with strobe input	G_1 - G_6	1	Q_1 - Q_6	10
FZH211/4.NAND34	Quad 2-input NAND	G_1 - G_8	1	Q_1 - Q_4	10
FZH231/2.NAND35	Dual 5-input NAND	G_1 - G_{10}	1	Q_1 ; Q_2	10
FZH241/2.AST30	Dual 4-input NAND Schmitt trigger	G_1 - G_8	1	Q_1 ; Q_2	10
FZH251/4.AND30	Quad 2-input AND	G_1 - G_8	1	Q_1 - Q_4	10
FZH261/2.N-4.I30	Dual NAND/Quad inverter	G_1 - G_8	1	Q_1 - Q_6	10
FZH271/4.EO30	Quad EXCLUSIVE-OR	G_1 - G_8	1	Q_1 - Q_4	10

LOADING TABLE (continued)

type	function	input (D.U.)		output (D.U.)	
		terminal	required	terminal	available
FZH281/4.NOR30	Quad NOR	G_1-G_8	1	Q_1-Q_4	10
FZH291/4.OR30	Quad OR	G_1-G_8	1	Q_1-Q_4	10
FZJ101/FF30	Single JK master-slave flip-flop	J_1;J_2;K_1;K_2	1	Q_1;Q_2	10
		T	2		
		S_1;S_2	1,5		
FZJ111/FF31	Single JK master-slave flip-flop	J_1;J_2;K	1	Q_1;Q_2	10
		T	2		
		S_1;S_2	1,5		
FZJ121/2.FF32	Dual JK master-slave flip-flop	J_1;J_2;K_1;K_2	1	Q_1-Q_4	10
		T_1;T_2	2		
		S_1-S_4	1,5		
FZJ131/4.FF33	Quad D-type latch flip-flop	D_1-D_4	2	Q_1-Q_8	10
		T_1;T_2	4		
FZJ141/FF34	Single synchronous decimal counter	all inputs	1	Q_A;Q_B;Q_C;Q_D	10
FZJ151/FF35	Single synchronous 4-bit binary counter	all inputs	1	Q_A;Q_B;Q_C;Q_D	10
FZJ161/FF36	Single synchronous 4-bit shift register	C_S input	4	Q_A;Q_B;Q_C;Q_D	10
		all other inputs	1		
FZK101/OS30	Monostable multivibrator	G_1-G_4	1	Q	10
FZL101/ND30	Single BCD-decimal decoder N.I.T. driver	I_1;I_2;I_4;I_8	1	Q_0-Q_9	I_{QH} = 50 mA, V_{QH} = 70 V: input comb. 0 to 9 I_{QH} = 5 mA, V_{QH} = 60 V: input comb. 10 to 15

LOADING TABLE (continued)

type	function	input (D.U.)		output (D.U.)	
		terminal	required	terminal	available
2. LRD30	Dual lamp/relay driver	G_1;G_2 E_1:E_2	3 3 (max 15 Si-diodes)	Q_1;Q_2	$I_{QL} \leq 200$ mA $V_{Pmax} = 17$ V
PA30	Power amplifier	G	$I_{GL} = 5,1$ mA; $V_{GL} = 1,7$ V	Q	$I_{QL} = 2$ A $V_{QL} = 1,3$ V
TU	Timer unit	G	$I_{GL} = 0,95$ mA $V_P = 11,4$ V $V_{GL} = 1,7$ V $I_{GL} = 1,6$ mA $V_P = 17$ V $V_{GL} = 1,7$ V	Q	22

NOTE

The figures quoted above for the fan-out in Drive Units (D.U.) are calculated for worst-case conditions: input Drive Units are simply added together to find the output Drive Units that the driving stage should be capable of supplying. To interface with other sorts of circuit, Drive Units can be interpreted as having the values shown below. These values are not applicable to the table.

LOW level:

1 input D.U. : 1,8 mA at 0 to 1,7 V
1 output D.U. : 1,5 mA at 1,7 V

HIGH level:

input voltage = between 10 V and V_P
output voltage = between 0,75 x V_P and V_P

LETTER SYMBOLS

1. General

The voltages and currents are related to the terminals to which they are applied or at which they appear. Each terminal is indicated by a letter relating to the function of the device or the function of the pertinent signal.
In order to avoid confusion by any ambiguity in logical conventions, signal levels are indicated by H (= HIGH, for the more positive potential) and L (= LOW, for the less positive potential). Where circuit functions or logical equations are involved, the logical convention is mentioned specifically (for positive logic: H = 1, and for negative logic: H = 0).

2. Terminal designations

CE = condition enable for output QE
C_Q = slow-down terminal
CT = condition enable trigger at input T
D = D input of D-type latch flip-flops
E = expander input (if necessary, this letter may be followed by a subscript, e.g. E_1 or E_2 or by one of the input letters, such as EG = gate expander input)
G = gate input
J, K = J, K input of JK flip-flops
N = negative supply
P = positive supply
Q = output
QE = output enable
R = direct Reset input
S = direct Set input
T = trigger (or toggle) input
ϕ = common supply return and voltage reference

3. Subscript sequence for voltages and currents

First subscript : terminal designation letter.
Second subscript : H (for HIGH) or L (for LOW), if applicable.
Third subscript : min or max, if applicable.
Examples : V_P, I_{QL}, V_{QHmin}, I_{PH} (in the latter case H denotes that the output level is HIGH).

4. Polarity of current and voltage

A current is defined as positive when its conventional direction of flow is into the device.
Unless otherwise specified, a voltage is measured with respect to the reference terminal (ϕ). Its polarity is defined as positive when the potential is higher than that of the reference terminal.

5. Time designations

If required for reasons of unambiguity, the related terminals may be included in the designations given below (e.g. t_{fQ1}).

t_f = fall time (transition from HIGH to LOW, see Fig. 1)

t_{hold} = hold time

t_H = signal HIGH duration (Fig. 1)

t_L = signal LOW duration (Fig. 1)

t_{pd} = average propagation delay time, defined as $\frac{t_{pdr} + t_{pdf}}{2}$

t_{pdf} = fall propagation delay time (output voltage falling, see Fig. 2)

t_{pdr} = rise propagation delay time (output voltage rising, see Fig. 2)

t_r = rise time (transition from LOW to HIGH, see Fig. 1)

t_{rec} = recovery time

t_{sc} = duration of short circuit (from relevant terminal to common return terminal)

t_{su} = set-up time

V_{pd} = reference voltage level for propagation delay measurement

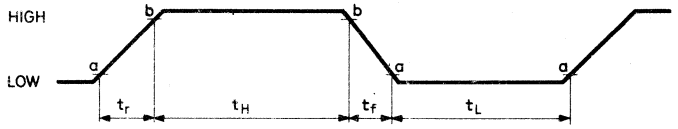


Fig. 1

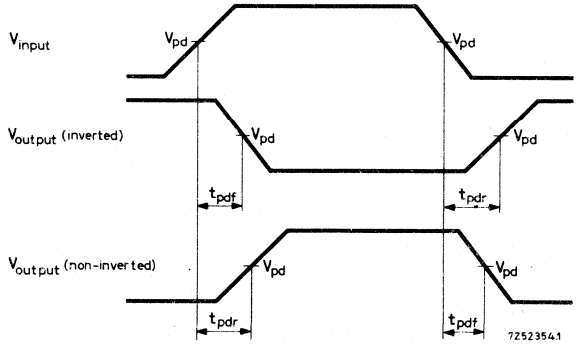


Fig. 2

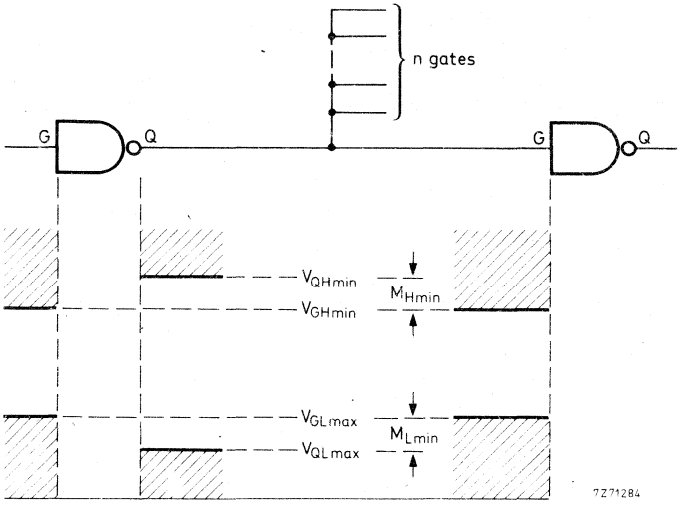
6. Other designations

i.c. = internally connected
Terminals with this indication should be left open. Otherwise correct working cannot be ensured; the device may even be damaged

I_P = supply current
The logic state of the device indicated by H of L is normally referred to the output level, unless otherwise specified

I_{Pmax} = supply current
Maximum d.c. value under defined conditions

M = d.c. noise margin



M_L = d.c. noise margin, signal level LOW
(defined as: $M_L = V_{GLmax} - V_{QLmax}$ under defined loading, temperature and supply voltage conditions)

M_H = d.c. noise margin, signal level HIGH
(calculated from: $M_H = V_{QHmin} - V_{GHmin}$ under defined loading, temperature and supply voltage conditions)

Na_L = available d.c. fan-out (defined as: $N_{aL} = \frac{I_{QLmax}}{-I_{GLmax}}$ under defined temperature and supply voltage conditions)

N_{aH} = available d.c. fan-out (defined as: $N_{aH} = \frac{-I_{QHmax}}{I_{GHmax}}$ under defined temperature and supply voltage conditions)

P_H;P_L = power consumption, defined as the product of the supply current(s) and of the corresponding supply voltage(s). The logical state of the device, indicated by a letter subscript H or L, is normally referred to the output level, unless otherwise specified

P_{av} = average power consumption at 50% duty cycle, unless otherwise specified. It is defined as: $P_{av} = V_P \cdot \frac{I_{PH} + I_{PL}}{2}$

P_{tot} = power dissipation, defined as the total power dissipated by the device. It is the sum of the products of all currents and voltages at each of the input, output and supply terminals, their polarities being taken into account. The logical state of the device indicated by a letter subscript H or L is normally referred to the output level, unless otherwise specified

T_{amb} = operating ambient temperature, i.e. the temperature of the free air in which the normally operating device is placed without external heat conduction, unless otherwise specified

T_{stg} = storage temperature, i.e. the temperature of the ambient medium in which the non-operating device is stored

V_{GLmax} = input voltage LOW at terminal G. With the specified level applied to the input of an inverting gate the output level will not be lower than the specified value V_{QHmin} at given I_{QH}.

V_{GHmin} = input voltage HIGH at terminal G. With the specified level applied to the input of an inverting gate the output level will not exceed the specified value V_{QLmax} at given I_{QL}.

V_H = hysteresis ($V_H = V_{TP} - V_{TN}$)

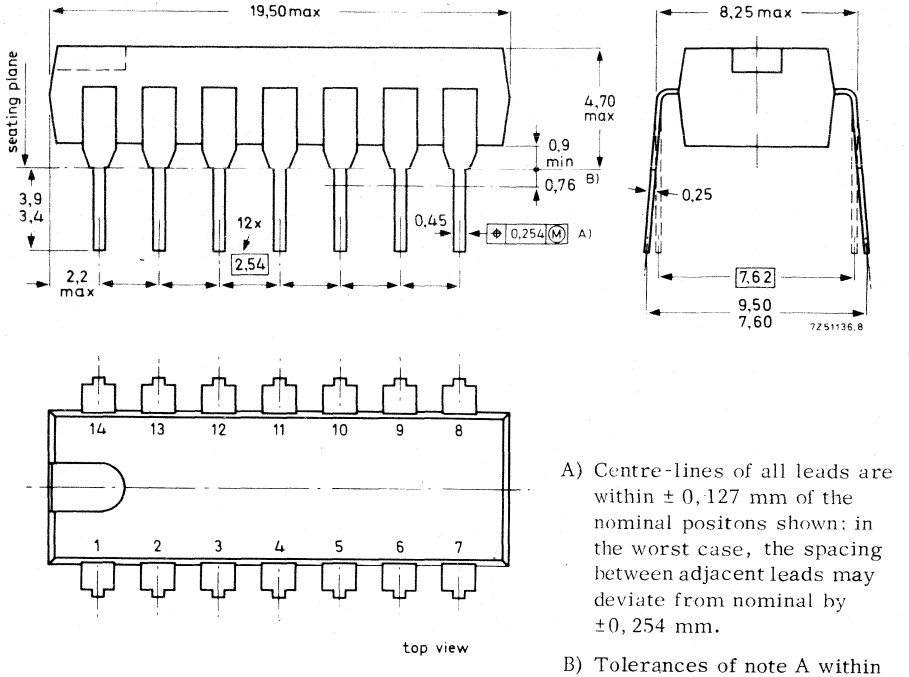
V_{TP} = positive-going threshold voltage

V_{TN} = negative-going threshold voltage

ΔV_Q = change of output voltage caused by a specified change of output current

14 LEAD PLASTIC DUAL IN-LINE

Dimensions in mm



A) Centre-lines of all leads are within ± 0,127 mm of the nominal positons shown: in the worst case, the spacing between adjacent leads may deviate from nominal by ±0,254 mm.

B) Tolerances of note A within this distance

⊕ Locational truth

Ⓜ Maximum Material Condition

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

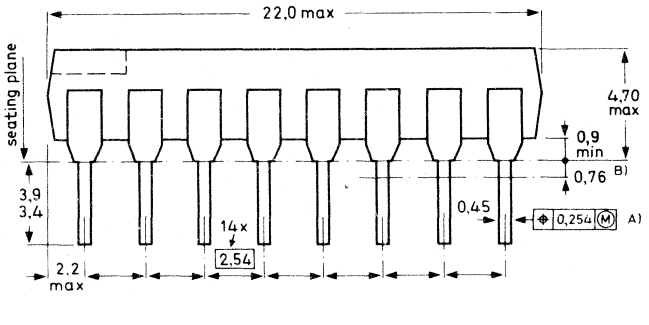
   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

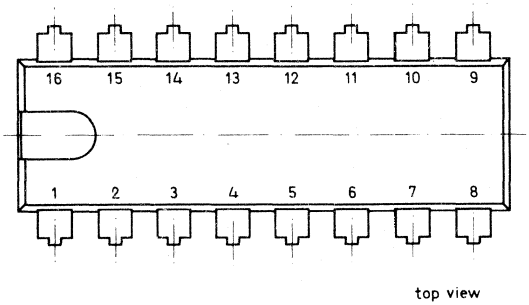
3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

16 LEAD PLASTIC DUAL IN-LINE

Dimensions in mm





A) Centre-lines of all leads are within ±0,127 mm of the nominal positions shown: in the worst case, the spacing between adjacent leads may deviate from nominal by ±0,254 mm.

B) Tolerances of note A within this distance

⊕ Locational truth

Ⓜ Maximum Material Condition

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

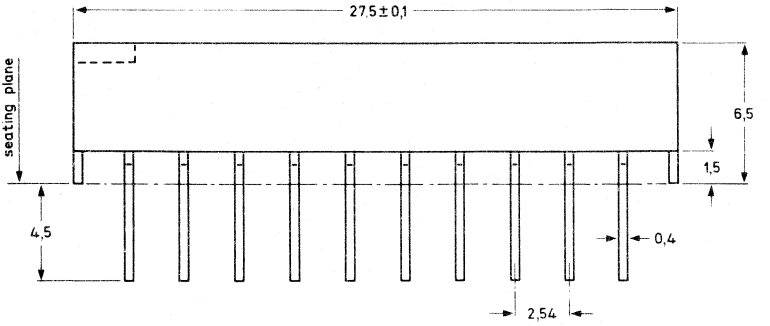
2. By dip or wave

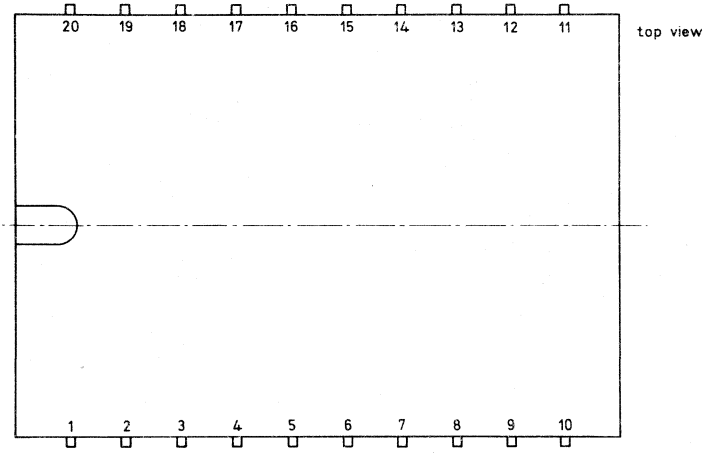
   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

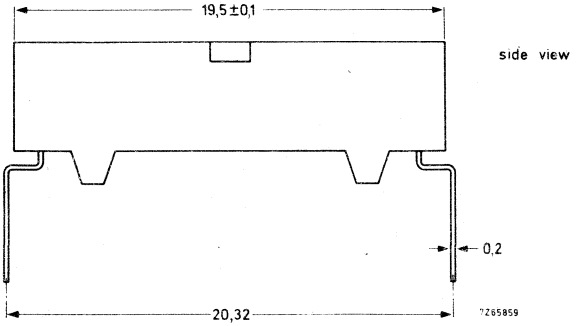
3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

20 LEAD DUAL IN-LINE

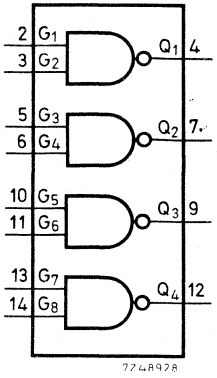




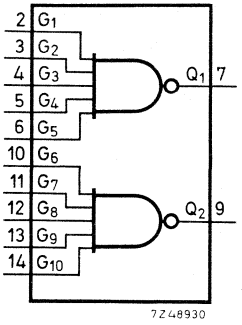


The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

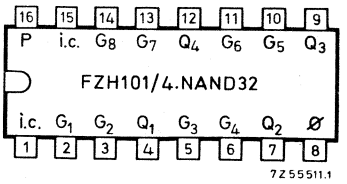
QUADRUPLE 2-INPUT NAND GATE
DUAL 5-INPUT NAND GATE

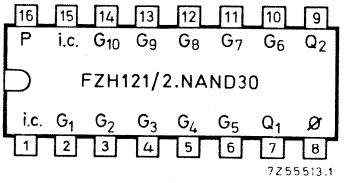


FZH101/4.NAND32



FZH121/2.NAND30





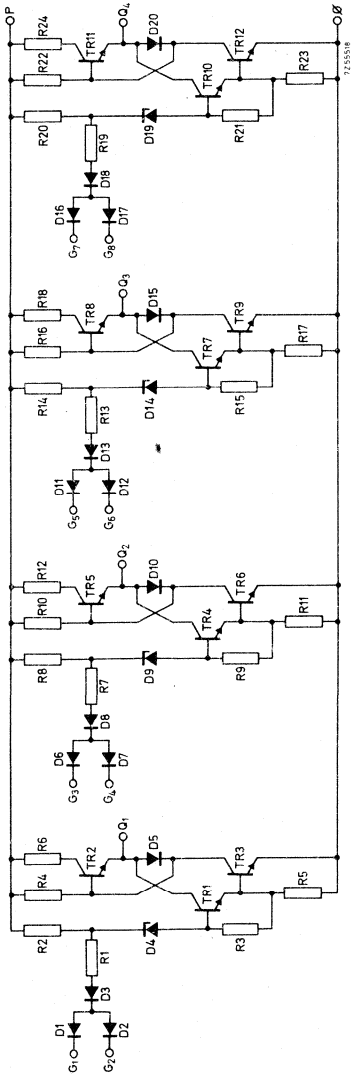
QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}	0 to +70		°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	170	ns
Available d.c. fan-out ($T_{amb} = 0$ to +70 °C) LOW state	N_{aL}	max.	10	
D.C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	16	mW
range II: $V_P = 15$ V	P_{av}	typ.	27	mW

The FZH101/4.NAND32 and FZH121/2.NAND30 consists of a number of independent NAND gates without slow-down capability.

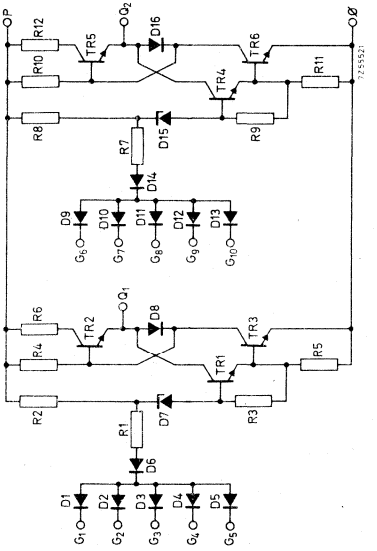
PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAMS

FZH101/4.NAND32



FZH121/2.NAND30



LOGIC FUNCTION

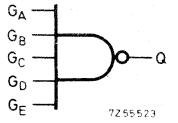
FZH101/4.NAND32

$Q = \overline{G_A \cdot G_B}$ (positive logic)

Function tables

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

FZH121/2.NAND30



$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot G_E}$

(positive logic)

G_A	G_B	G_C	G_D	G_E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	←
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max	18	V
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C
Output short-circuit duration	t_{Qsc}	max.	1 s [1]	←

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature		T_{amb}	0 to	+70	°C
Uniform system supply voltage (range I)		V_P	11,4 to	13,5	V
(range II)		V_P	13,5 to	17	V
Available d.c. fan-out		N_{aL}	max.	10	
		N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}		M_L	min.	2,8	V
		M_H	min.	2,5	V
range II at V_{Pmin}		M_L	min.	2,8	V
		M_H	min.	4,5	V
→ Supply current per gate	range I ; output HIGH	I_{Pav}	typ.	0,9	mA
	output LOW	I_{Pav}	typ.	1,7	mA
	range II; output HIGH	I_{Pav}	typ.	1,2	mA
	output LOW	I_{Pav}	typ.	2,3	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}		P_{tot}	max.	31	mW
at range II; V_{Pmax}		P_{tot}	max.	52	mW
Thermal resistance from system to ambient		R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.	Conditions and references: V_P (V)	Conditions and references
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4,5 V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 15 mA
Output HIGH	V_{QH}	10,0	11,3	– V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7 V	11,4	V_{GH} = 7,5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	– V	11,4	
LOW	M_L	2,8	5,0	– V	11,4	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1,0 µA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5 mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	– mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	– mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	10	30	50 mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	0,9	1,6 mA	13,5	V_G = 0 V
at V_{QL}	I_P	–	1,7	3,0 mA	13,5	V_G = 13,5 V
Dynamic data						
Times						
Propagation delay:						
fall time	t_{pdf}	90	175	310 ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	90	175	310 ns	12	
output rise time	t_r	200	340	570 ns	12	
output fall time	t_f	70	120	210 ns	12	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
[2] Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

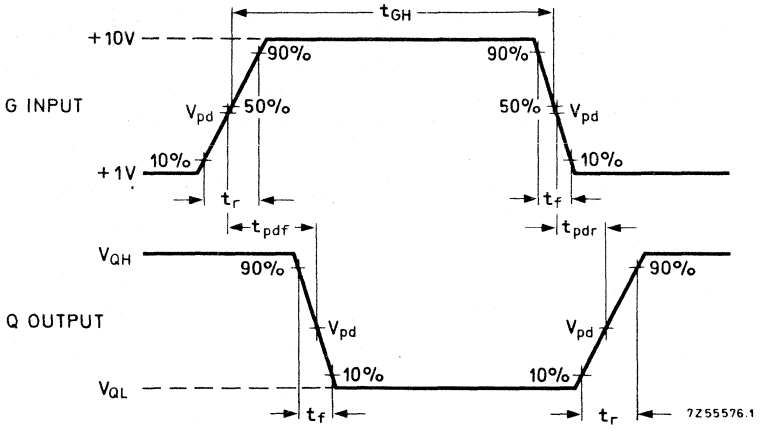
	Sym-bol	min.	typ.[1]	max.	Conditions and references: V_P (V)	
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5 V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	– V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7 V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	– V	13,5	
LOW	M_L	2,8	5,0	– V	13,5	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1,0 µA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8 mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	– mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	$-I_{QL}$	18	–	– mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited[2]	$-I_{Qsc}$	15	37	60 mA	17	V_G = 0 V; V_Q = 0 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	1,2	2,1 mA	17	V_G = 0 V
at V_{QL}	I_P	–	2,3	4,0 mA	17	V_G = 17 V
Dynamic data						
Times						
Propagation delay:						
fall time	t_{pdf}	–	140	– ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	–	195	– ns	15	
output rise time	t_r	–	410	– ns	15	
output fall time	t_f	–	75	– ns	15	

[1] All typical values under test conditions : T_{amb} = 25 °C and V_P = 15 V.

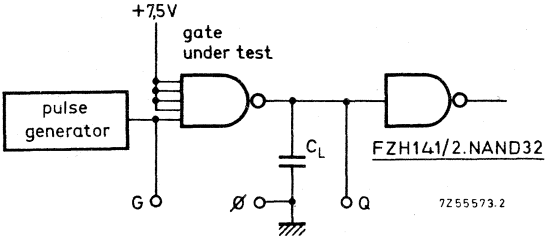
[2] Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = + 4,5 V
t_f = 120 ns
t_{GH} = 1 µs

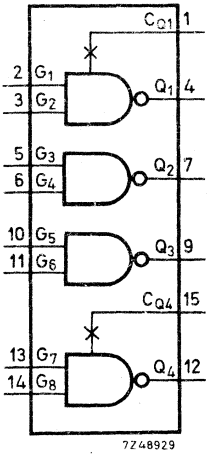


Measuring conditions: V_P = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C

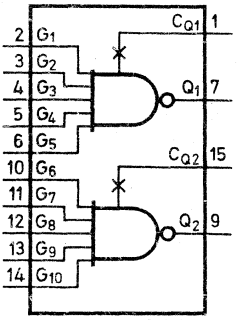
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

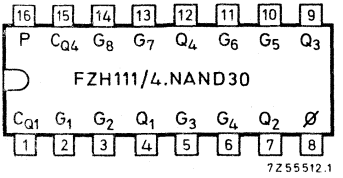
QUADRUPLE 2-INPUT NAND GATE
DUAL 5-INPUT NAND GATE
both having slow-down capability

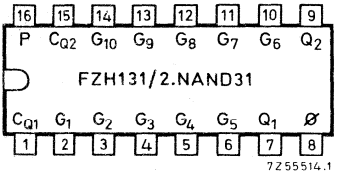


FZH111/4.NAND30



FZH131/2.NAND31





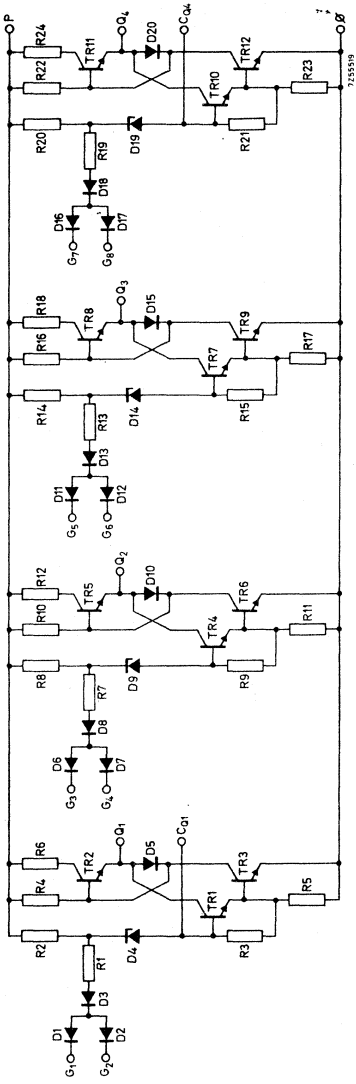
QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}	0 to +70		°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	170	ns
Available d.c. fan-out ($T_{amb} = 0$ to +70 °C) LOW state	N_{aL}	max.	10	
D.C. noise margin at $T_{amb} = 25$ °C				
range I ; $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II; $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	16	mW
range II: $V_P = 15$ V	P_{av}	typ.	27	mW

The FZH111/4.NAND30 and FZH131/2.NAND31 consist of a number of independent NAND gates at which two NAND gates per type have a special terminal (C_Q). It is possible to connect a capacitor between the output (Q) and the corresponding slow-down terminal (C_Q) to increase the propagation delay.

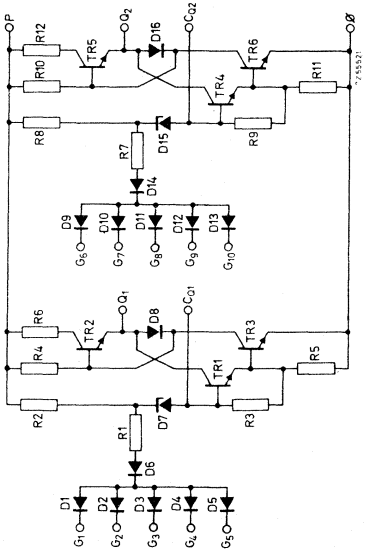
PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAMS

FZH111/4.NAND30

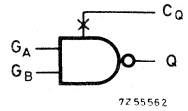


FZH131/2.NAND31



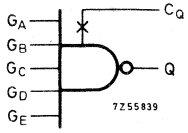
LOGIC FUNCTION

FZH111/4.NAND30



$Q = \overline{G_A \cdot G_B}$ (positive logic)

FZH131/2.NAND31



$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot G_E}$
(positive logic)

Function tables

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

G_A	G_B	G_C	G_D	G_E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)	V_P	11,4 to 13,5		V
(range II)	V_P	13,5 to 17		V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current per gate; range I ; output HIGH	I_{Pav}	typ.	0,9	mA
output LOW	I_{Pav}	typ.	1,7	mA
range II; output HIGH	I_{Pav}	typ.	1,2	mA
output LOW	I_{Pav}	typ.	2,3	mA
Power consumption per gate (50% duty cycle) at range I; V_{Pmax}	P_{tot}	max.	31	mW
at range II; V_{Pmax}	P_{tot}	max.	52	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ.[1]	max.	Conditions and references: V_P (V)	
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	11,4	$V_{QL} \leqslant 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4,5 V	11,4 and 13,5	$V_{QH} \geqslant 10$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	– V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7 V	11,4	V_{GH} = 7,5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	– V	11,4	
LOW	M_L	2,8	5,0	– V	11,4	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1,0 μA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5 mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	– mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	– mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited[2]	$-I_{Qsc}$	10	30	50 mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	0,9	1,6 mA	13,5	V_G = 0 V
at V_{QL}	I_P	–	1,7	3,0 mA	13,5	V_G = 13,5 V
Dynamic data						
Times						
Propagation delay						
fall time	t_{pdf}	90	175	310 ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	90	175	310 ns	12	
output rise time	t_r	200	340	570 ns	12	
output fall time	t_f	70	120	210 ns	12	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
[2]) Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

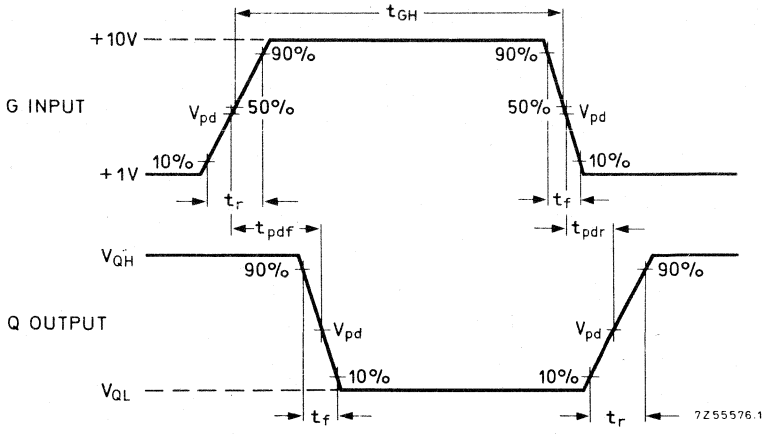
	Sym-bol	min.	typ.[1]	max.	Conditions and references: V_P (V)	Conditions and references
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	13,5	$V_{QL} \leqslant 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5 V	13,5 and 17	$V_{QH} \geqslant 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	– V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7 V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	– V	13,5	
LOW	M_L	2,8	5,0	– V	13,5	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1,0 μA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8 mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	– mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	– mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	15	37	60 mA	17	V_G = 0 V; V_Q = 0 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	1,2	2,1 mA	17	V_G = 0 V
at V_{QL}	I_P	–	2,3	4,0 mA	17	V_G = 17 V
Dynamic data						
Times						
Propagation delay						
fall time	t_{pdf}	–	140	– ns	15	C_L = 10 pF; N = 1; Tamb = 25 °C; Vdp = 4,5 V
rise time	t_{pdr}	–	195	– ns	15	
output rise time	t_r	–	410	– ns	15	
output fall time	t_f	–	75	– ns	15	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

→ [2]) Short-circuit duration max. 1 s.

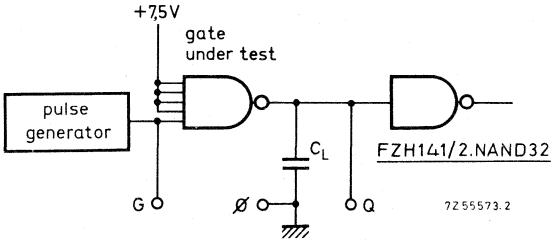
CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns
t_f = 120 ns
t_{GH} = 1 µs

V_{pd} = + 4,5 V



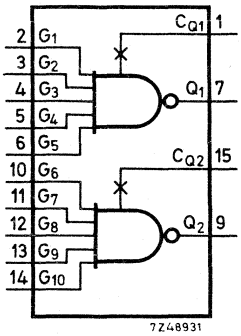
Measuring conditions: V_P = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
Slow-down terminals are not connected

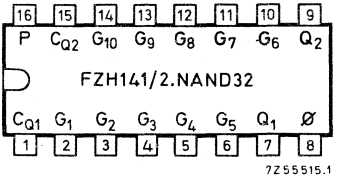
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL 5-INPUT POWER NAND GATE

with slow-down capability



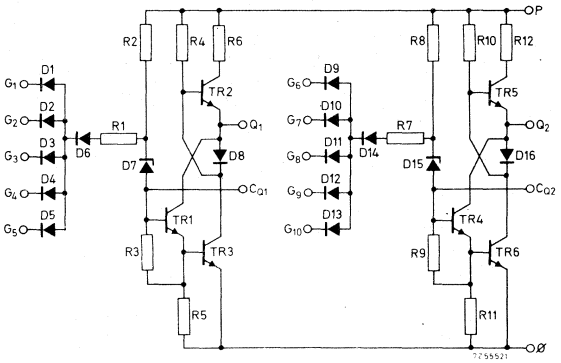


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}	0 to +70		°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	170	ns
Available d.c. fan-out ($T_{amb} = 0$ to +70 °C) LOW state	N_{aL}	max.	30	
D.C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C				
(50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	16	mW
range II: $V_P = 15$ V	P_{av}	typ.	27	mW

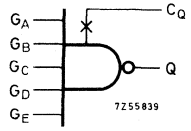
The FZH141/2.NAND32 is a dual 5-input power NAND gate with on each gate a special base connection (C_Q). It is possible to connect a capacitor between the output (Q) and the corresponding slow-down terminal (C_Q) to increase the propagation delay.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot G_E}$$
(positive logic)

Function table

G_A	G_B	G_C	G_D	G_E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
→ Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C
→ Output **short-circuit duration**	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70	°C
Uniform system supply voltage (range I)	V_P	11,4 to 13,5	V
(range II)	V_P	13,5 to 17	V
Available d.c. fan-out	N_{aL}	max. 30	
	N_{aH}	max. 100	
D.C. noise margin; range I at V_{Pmin}	M_L	min. 2,8	V
	M_H	min. 2,5	V
range II at V_{Pmin}	M_L	min. 2,8	V
	M_H	min. 4,5	V
Supply current per gate; range I; output HIGH	I_{Pav}	typ. 0,9	mA
output LOW	I_{Pav}	typ. 1,7	mA
range II; output HIGH	I_{Pav}	typ. 1,2	mA
output LOW	I_{Pav}	typ. 2,3	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max. 31	mW
at range II ; V_{Pmax}	P_{tot}	max. 52	mW
Thermal resistance from system to ambient	R_{th}	max. 150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.	Conditions and references: V_P (V)	Conditions and references
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	-	- V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 45 mA
Input LOW	V_{GL}	-	-	4,5 V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	- V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	-	1,3	1,7 V	11,4	V_{GH} = 7,5 V; I_{QL} = 45 mA
D. C. noise margin: HIGH	M_H	2,5	5,0	- V	11,4	
LOW	M_L	2,8	5,0	- V	11,4	
Currents (per gate)						
Input HIGH	I_{GH}	-	-	1,0 µA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	-	0,8	1,5 mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	-	- mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	45	-	- mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	10	30	50 mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	-	0,9	1,6 mA	13,5	V_G = 0 V
at V_{QL}	I_P	-	1,7	3,0 mA	13,5	V_G = 13,5 V
Dynamic data						
Times						
Propagation delay						
fall time	t_{pdf}	90	175	310 ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	90	175	310 ns	12	
output rise rime	t_r	200	340	570 ns	12	
output fall time	t_f	70	120	210 ns	12	

1) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

2) Short-circuit duration max. 1 s.

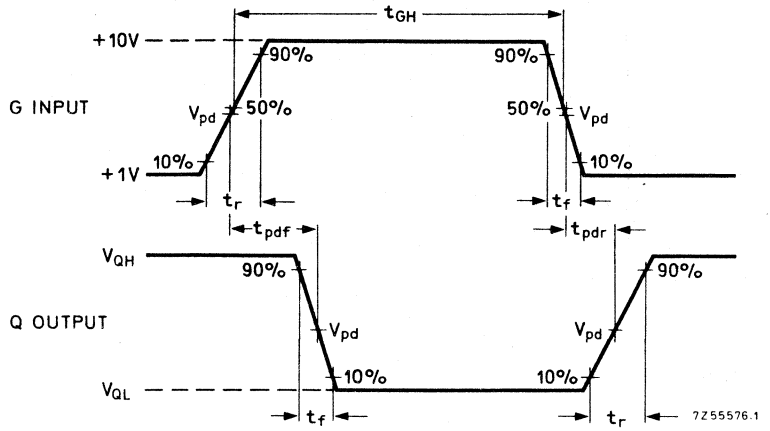
CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references: V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	-	-	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 54 mA
Input LOW	V_{GL}	-	-	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	-	V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	-	1,4	1,7	V	13,5	V_{GH} = 7,5 V; I_{QL} = 54 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	-	V	13,5	
LOW	M_L	2,8	5,0	-	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	-	-	1,0	µA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	-	-	1,8	mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	54	-	-	mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	15	37	60	mA	17	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	-	1,2	2,1	mA	17	V_G = 0 V
at V_{QL}	I_P	-	2,3	4,0	mA	17	V_G = 17 V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	-	140	-	ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{dp} = 4,5 V
rise time	t_{pdr}	-	195	-	ns	15	
output rise time	t_r	-	410	-	ns	15	
output fall time	t_f	-	75	-	ns	15	

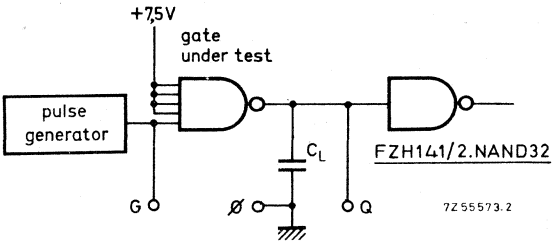
1) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.
2) Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = +4,5 V
t_f = 120 ns
t_{GH} = 1 µs

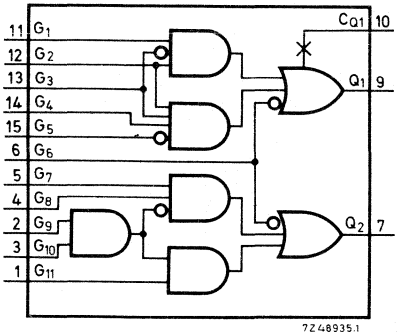


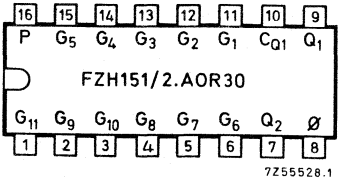
Measuring conditions: V_P = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
Slow-down terminals are not connected

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL AND-AND-OR GATE
with slow-down capability





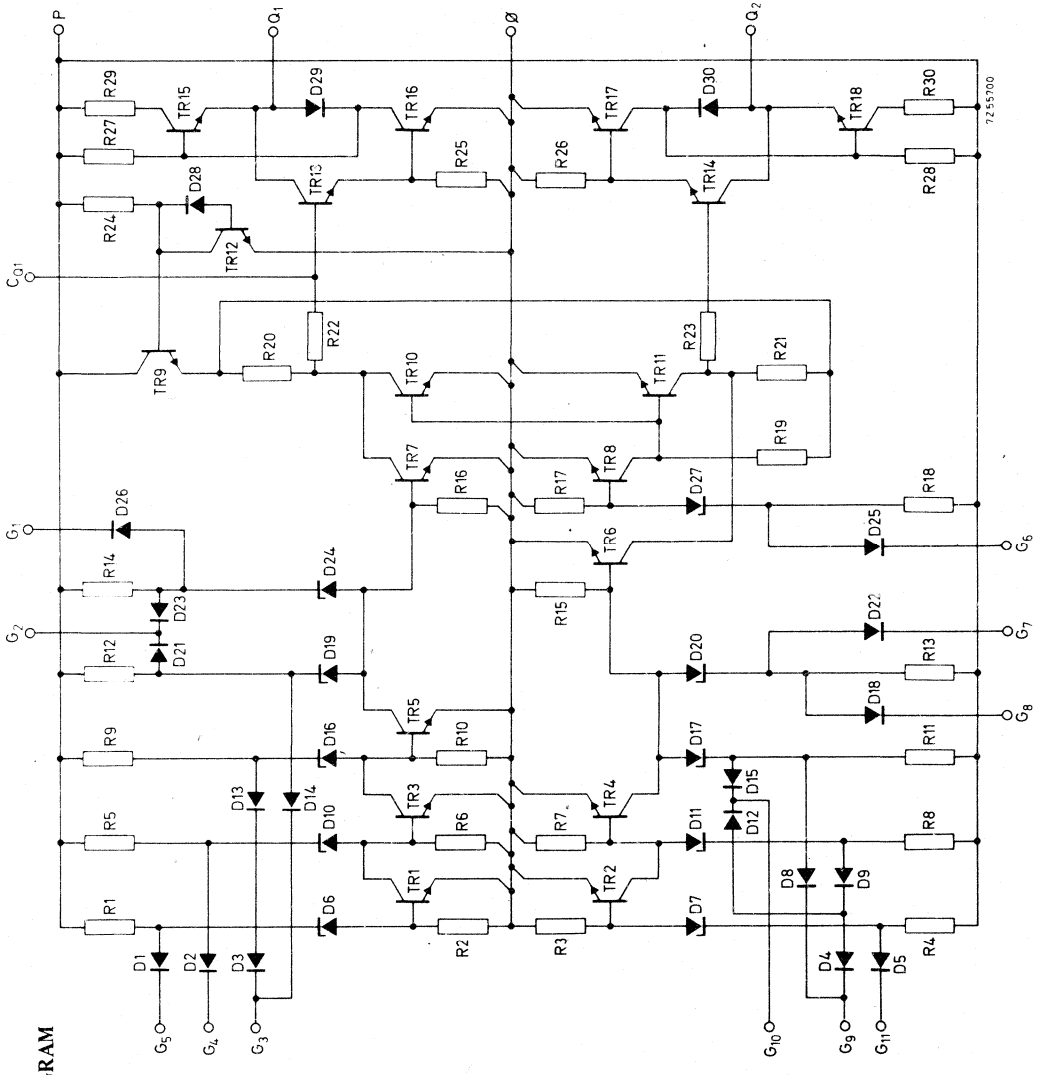
QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}	0 to +70		°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	380	ns
Available d.c. fan-out ($T_{amb} = 0$ to +70 °C) LOW state	N_{aL}	max.	20	1)
	N_{aL}	max.	16	2)
D.C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	132	mW
range II: $V_P = 15$ V	P_{av}	typ.	225	mW

1) At FZH151/2.AOR30 load.
2) At HNIL gate load.

G_2, G_3, G_9 and G_{10} count for two inputs.

The FZH151/2.AOR30 consists of two combinations AND and OR gates with some common inputs to the AND gates and a common override input to the OR gates. One of the OR gates has a special terminal (C_{Q1}) to provide slow-down capability.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).



CIRCUIT DIAGRAM

LOGIC FUNCTION

$$Q_1 = G_1 \cdot G_2 \cdot \overline{G_3} + G_2 \cdot G_3 \cdot G_4 \cdot \overline{G_5} + \overline{G_6}$$

$$Q_2 = G_7 \cdot G_8 \cdot \overline{G_9 \cdot G_{10}} + G_9 \cdot G_{10} \cdot G_{11} + \overline{G_6}$$

} for positive logic

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]

[1] Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to	70	°C
Uniform system supply voltage (range I)	V_P	11,4 to	13,5	V
(range II)	V_P	13,5 to	17	V
Available d.c. fan-out: at FZH151/2.AOR30	N_{aL}	max.	20	*)
at HNIL gate load	N_{aL}	max.	16	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current per gate: range I ; output HIGH	I_{Pav}	typ.	14	mA
output LOW	I_{Pav}	typ.	8,0	mA
range II; output HIGH	I_{Pav}	typ.	18	mA
output LOW	I_{Pav}	typ.	12	mA
Power consumption per gate (50% duty cycle) at range I , V_{Pmax}	P_{tot}	max.	250	mW
at range II, V_{Pmax}	P_{tot}	max.	425	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

*) G_2, G_3, G_9 and G_{10} count for two inputs.

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ.[1]	max.		Conditions and references: V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	11,4	V_{QL} = max 1,7 V; I_{QL} = 30 mA
Input LOW	V_{GL}	–	–	4,5	V	11,4	V_{QH} = min 10 V; $-I_{GH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	–	V	11,4	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	V_{GH} = 7,5 V; I_{QL} = 30 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V		
LOW	M_L	2,8	5,0	–	V		
Currents							
Input HIGH: $G_2;G_3;G_9;G_{10}$	I_{GH}	–	–	2	μA	13,5	V_{GH} = 13,5 V; other inputs 0 V
at other G inputs	I_{GH}	–	–	1	μA		
Input LOW: $G_2;G_3;G_9;G_{10}$	$-I_{GL}$	–	1,0	2,5	mA	13,5	V_{GL} = 1,7 V; other inputs 13,5V
at other G inputs	$-I_{GL}$	–	0,5	1,25	mA		
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	30	–	–	mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	10	30	50	mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data							
Currents							
at V_{QH}	I_P	–	14,0	22,0	mA	13,5	V_G = 0 V
at V_{QL}	I_P	–	8,0	15,0	mA	13,5	V_{G11} = V_{GL}; other G inputs: V_{GH}

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
[2]) Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	V_{QL} = max. 1,7 V; I_{QL} = 36 mA
Input LOW	V_{GL}	–	–	4,5	V	13,5	V_{QH} = min. 12 V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{GH} = 7,5 V; I_{QL} = 36 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents							
Input HIGH: $G_2;G_3;G_9;G_{10}$	I_{GH}	–	–	2,0	μA	17	V_{GH} = 17 V; other inputs 0 V
at other G inputs	I_{GH}	–	–	1,0	μA		
Input LOW: $G_2;G_3;G_9;G_{10}$	$-I_{GL}$	–	1,2	3,0	mA	17	V_{GL} = 1,7 V; other inputs 17 V
at other G inputs	$-I_{GL}$	–	0,6	1,5	mA		
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5	V_{GL} = 4,5 V; V_{QH} = 12 V
→ Output LOW	I_{QL}	30	–	–	mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	15	37	60	mA	17	V_G = 0 V; V_Q = 0 V
Supply data							
Currents							
at V_{QH}	I_P	–	18	29	mA	17	V_G = 0 V
at V_{QL}	I_P	–	12	21	mA	17	V_{G11} = V_{GL}; other G inputs: V_{GH}

[1] All typical values under test condiotions: T_{amb} = 25 °C and V_P = 15 V.

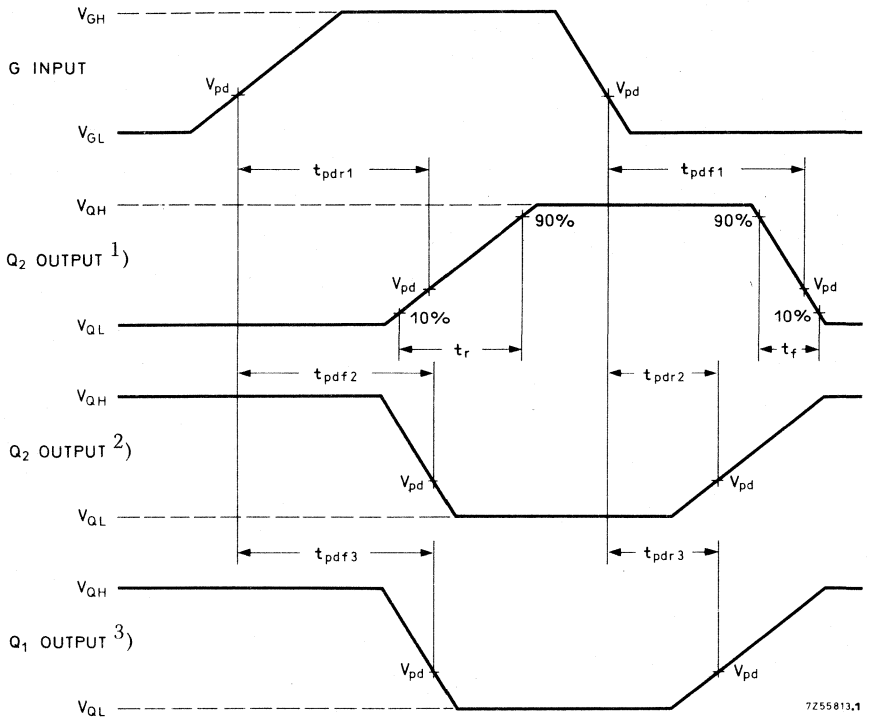
→ [2] Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

	Symbol	min.	typ.[1]	max.		V_P (V)	Conditions and references
Dynamic data							
Times							
Propagation delay							
fall times at output Q	t_{pdf1}	–	230	–	ns	12	C_L = 10 pF N = 1 T_{amb} = 25 °C V_{pd} = 4,5 V
at output $\overline{Q}$	t_{pdf2}	–	300	–	ns	12	
at input G_5	t_{pdf3}	–	400	–	ns	12	
rise times at output Q	t_{pdr1}	–	340	–	ns	12	
at output $\overline{Q}$	t_{pdr2}	–	340	–	ns	12	
at input G_5	t_{pdr3}	–	270	–	ns	12	
Output rise time	t_r	–	330	–	ns	12	
Output fall time	t_f	–	200	–	ns	12	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)



Waveforms illustrating measurement of t_{pdr} and t_{pdf}

1) If G input = G_7, G_8, G_{11}.

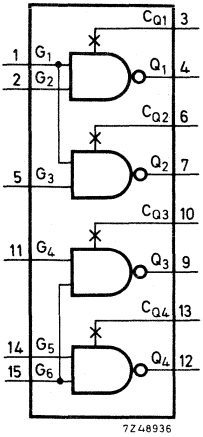
2) If G input = G_6.

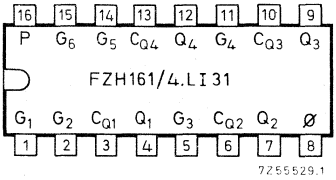
3) If G input = G_5.

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE LOGIC INTERFACE GATE

HNIL to 5 V logic; with slow-down capability



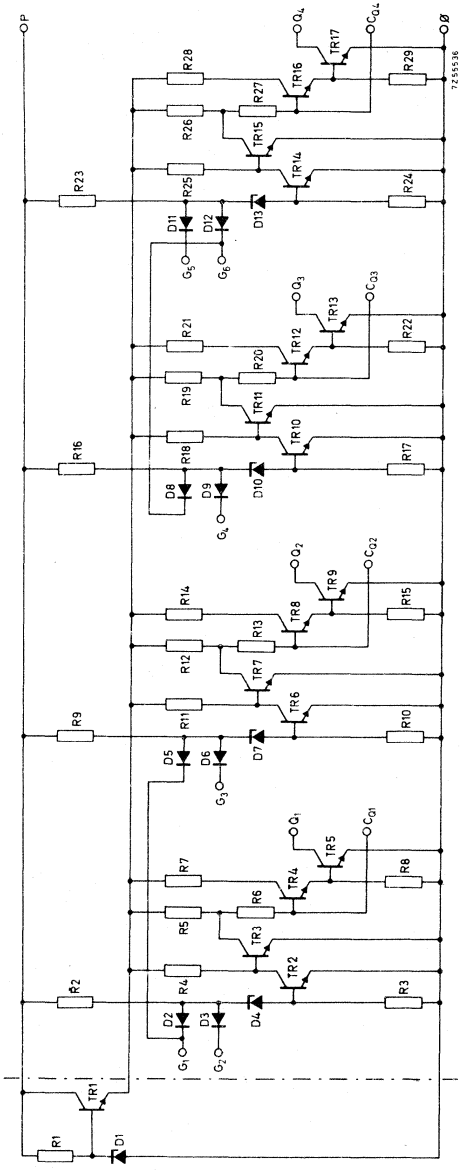


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}	0 to +70		°C
Average propagation delay				
V_P = 12 V; N = 1 ; V_Q = 12 V	t_{pd1}	typ.	115	ns
V_{pd} = 4,5 V; T_{amb} = 25 °C ; V_Q = 5 V	t_{pd2}	typ.	105	ns
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II: V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at T_{amb} = 25 °C				
(50% duty cycle) range I : V_P = 12 V	P_{av}	typ.	39	mW
range II: V_P = 15 V	P_{av}	typ.	55	mW

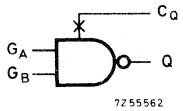
The FZH161/4. LI31 is a level converter with open-collector outputs for HNIL to TTL and consists of 4 gates and some common inputs.
Each gate has slow-down capability.

PACKAGE OUTLINE 16 leads plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$Q = \overline{G_A \cdot G_B}$

(for positive logic)

Function table

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage (HIGH state)	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA
Storage temperature	T_{stg}	-65 to +150		°C
Operating ambient temperature	T_{amb}	0 to + 70		°C

SYSTEM DESIGN DATA

Uniform system temperature		T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)		V_P	11,4 to 13,5		V
(range II)		V_P	13,5 to 17		V
Available output current		I_{QL}	min.	20	mA
		I_{QH}	max.	50	µA
D.C. noise margin; range I at V_{Pmin}		M_L	min.	2,8	V
		M_H	min.	2,5	V
range II at V_{Pmin}		M_L	min.	2,8	V
		M_H	min.	4,5	V
Supply current per gate	range I ; output HIGH	I_{Pav}	typ.	2,5	mA
	output LOW	I_{Pav}	typ.	4,0	mA
	range II; output HIGH	I_{Pav}	typ.	2,8	mA
	output LOW	I_{Pav}	typ.	4,5	mA
Power consumption per gate (50 % duty cycle) at range I ; V_{Pmax}		P_{tot}	max.	71	mW
at range II; V_{Pmax}		P_{tot}	max.	98	mW
Average propagation delay					
at V_{pd1} = 4,5 V; (V_Q = 12 V)		t_{pd1}	max.	275	ns
at V_{pd2} = 1,5 V; (V_Q = 5 V)		t_{pd2}	max.	275	ns
Thermal resistance from system to ambient		R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C.

	Sym-bol	min.	typ. [1])	max.	Conditions and references: V_P (V)	
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	11,4	V_{QL} = 0,4 V; I_{QL} = 20 mA
Input LOW	V_{GL}	–	–	4,5 V	11,4	V_{QH} = 13,5 V; I_{QH} = 40 µA
Output LOW	V_{QL}	–	–	0,4 V	11,4	V_{GH} = 7,5 V; I_{QL} = 20 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	11,4	
LOW	M_L	2,8	5,0	–	11,4	
Currents (per gate)						
Input HIGH; G_2; G_3; G_4; G_5	I_{GH}	–	–	1,0 µA	13,5	V_{GH} = 13,5 V; other inputs 0V
G_1; G_6	I_{GH}	–	–	2,0 µA		
Input LOW; G_2;G_3; G_4; G_5	$-I_{GL}$	–	0,8	1,5 mA	13,5	V_{GL}= 1,7 V; other inputs 13,5V
G_1; G_6	$-I_{GL}$	–	1,6	3,0 mA		
Output HIGH	I_{QH}	–	–	80 µA	11,4	V_{QH} = 13,5 V; V_{GH} = 4,5 V
Output LOW	I_{QL}	20	–	– mA	11,4	V_{QL} = 0,4 V; V_{GH} = 7,5 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	2,5	4,5 mA	13,5	V_G = 0 V
at V_{QL}	I_P	–	4,0	6,0 mA	13,5	V_G = 13,5 V
Dynamic data						
Times						
Propagation delay						
fall time: V_Q = 12 V	t_{pdf1}	–	100	250 ns		R_L =390 Ω; N = 1; T_{amb} = 25 °C
V_Q = 5 V	t_{pdf2}	–	90	250 ns		
rise time: V_Q = 12 V	t_{pdr1}	–	130	300 ns		R_L =3,9kΩ; N = 1; T_{amb} = 25 °C
V_Q = 5 V	t_{pdr2}	–	120	300 ns		

[1]) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.		Conditions and references	
						V_P (V)	
Static data							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	V_{QL} = 0,4 V; I_{QL} = 20 mA
Input LOW	V_{GL}	–	–	4,5	V	13,5	V_{QH} = 17 V; I_{QH} = 40 µA
Output LOW	V_{QL}	–	–	0,4	V	13,5	V_{GH} = 7,5 V; I_{QL} = 20 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH: G_2;G_3;G_4;G_5	I_{GH}	–	–	1,0	µA	17	V_{GH} = 17 V; other inputs 0 V
G_1;G_6	I_{GH}	–	–	2,0	µA		
Input LOW: G_2;G_3;G_4;G_5	$-I_{GL}$	–	1,0	1,8	mA	17	V_{GL} = 1,7 V; other inputs 17V
G_1;G_6	$-I_{GL}$	–	2,0	3,6	mA		
Output HIGH	I_{QH}	–	–	80	µA	13,5	V_{QH} = 17 V; V_{GL} = 4,5 V
Output LOW	I_{QL}	20	–	–	mA	13,5	V_{QL} = 0,4 V; V_{GL} = 7,5 V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	2,8	4,5	mA	17	V_G = 0 V
at V_{QL}	I_P	–	4,5	7,0	mA	17	V_G = 17 V

[1]) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

CHARACTERISTICS (continued)

Calculation of collector resistor R_Q

The collector resistor R_Q has to be calculated from voltages and input- and output currents of the gates.

$$R_{Qmax} = \frac{V_P - V_{QH} \quad (V)}{m \cdot I_{QH} + N \cdot I_{GH} \quad (\mu A)} \qquad R_{Qmin} = \frac{V_P - V_{QL} \quad (V)}{I_{QLmax} - N \cdot I_{GL} \quad (mA)}$$

m = number of interconnected outputs
N = number of used inputs
V_P = supply voltage of TTL-inputs
V_{QH} = output voltage HIGH of TTL-circuit
V_{QL} = output voltage LOW of TTL-circuit
I_{GH} = input current HIGH of TTL-circuit
I_{GL} = input current LOW of TTL-circuit

For interfacing HNIL to TTL:

$$R_{Qmax} = \frac{5 - 2,4 \quad (V)}{m \cdot 80 + N \cdot 80 \, (\mu A)} \qquad R_{Qmin} = \frac{5 - 0,4 \quad (V)}{20 - N \cdot 1,6 \quad (mA)}$$

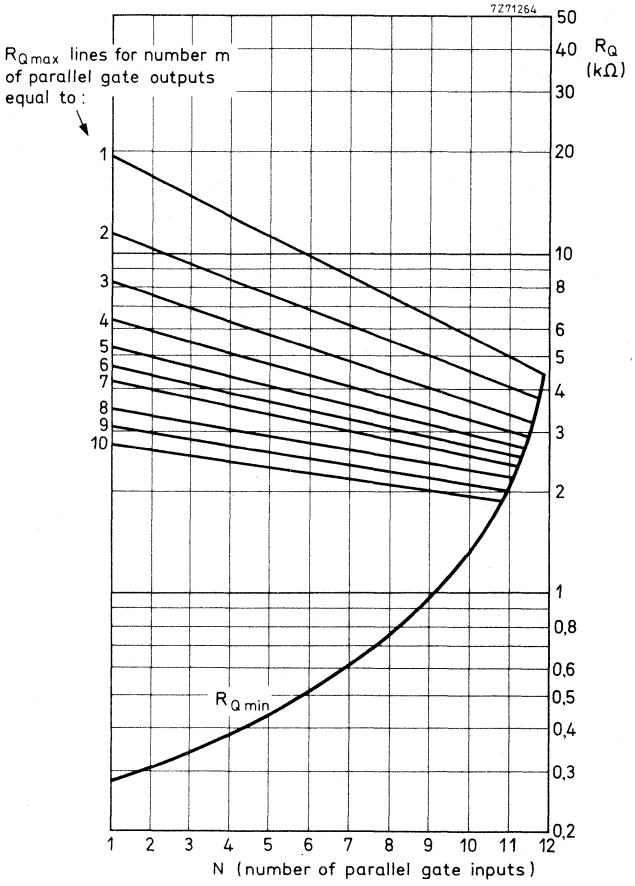
If FZH161/4. LI31 is used as wired-OR combination

for range I: $V_P = 12$ V

$$R_{Qmax} = \frac{12 - 10 \quad (V)}{m \cdot 80 + N \cdot 1 \, (\mu A)} \qquad R_{Qmin} = \frac{12 - 0,4 \quad (V)}{20 - N \cdot 1,5 \quad (mA)}$$

for range II: $V_P = 15$ V

$$R_{Qmax} = \frac{15 - 12 \quad (V)}{m \cdot 80 + N \cdot 1 \, (\mu A)} \qquad R_{Qmin} = \frac{15 - 0,4 \quad (V)}{20 - N \cdot 1,8 \quad (mA)}$$

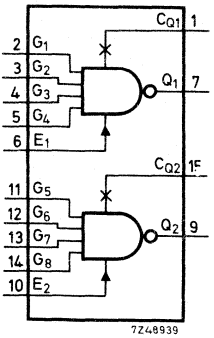


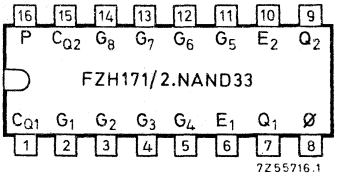
R_Q as a function of m and N loaded with TTL gates.

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL 4-INPUT NAND GATE

with slow-down capability and expandable inputs



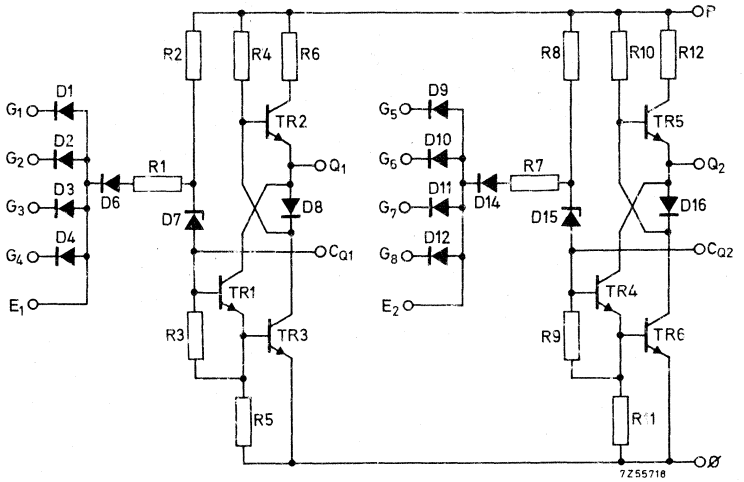


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}	0 to +70		°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	170	ns
Available d.c. fan-out $T_{amb} = 0$ to +70 °C } LOW state	N_{aL}	max.	10	
D.C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	16	mW
range II: $V_P = 15$ V	P_{av}	typ.	27	mW

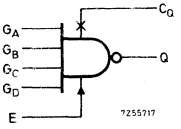
The FZH171/2.NAND33 consists of two independent NAND gates and each gate has a special terminal (C_Q). It is possible to connect a capacitor between the output (Q) and the corresponding slow-down terminal (C_Q) to increase the propagation delay.
Non-used expander inputs E_1 and E_2 must be left floating.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot E}\ ^{*})$$

(positive logic)

*) When provided with a diode

G_A	G_B	G_C	G_D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA
Expandable input voltage	V_E	min.	0	V
Expandable input current	$-I_E$	max.	25	mA

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature		T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)		V_P	11,4 to 13,5		V
(range II)		V_P	13,5 to 17		V
Available d.c. fan-out		N_{aL}	max.	10	
		N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}		M_L	min.	2,8	V
		M_H	min.	2,5	V
range II at V_{Pmin}		M_L	min.	2,8	V
		M_H	min.	4,5	V
Supply current per gate	range I; output HIGH	I_{Pav}	typ.	0,9	mA
	output LOW	I_{Pav}	typ.	1,7	mA
	range II; output HIGH	I_{Pav}	typ.	1,2	mA
	output LOW	I_{Pav}	typ.	2,3	mA
Power consumption per gate (50% duty cycle) at range I; V_{Pmax}		P_{tot}	max.	31	mW
at range II; V_{Pmax}		P_{tot}	max.	52	mW
Thermal resistance from system to ambient		R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1])	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4,5	V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	–	V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	V_{GH} = 7,5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5	mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	–	mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2])	$-I_{Qsc}$	10	30	50	mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	0,9	1,6	mA	13,5	V_G = 0 V
at V_{QL}	I_P	–	1,7	3,0	mA	13,5	V_G = 13,5 V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	90	175	310	ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	90	175	310	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

[1]) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
[2]) Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

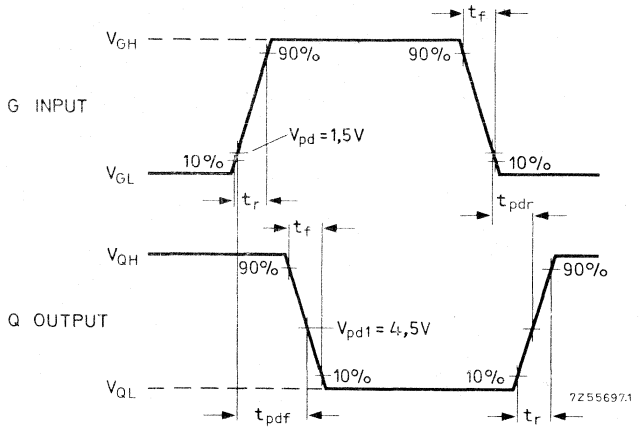
	Sym-bol	min.	typ.[1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8	mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	15	37	60	mA	17	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	1,2	2,1	mA	17	V_G = 0 V
at V_{QL}	I_P	–	2,3	4,0	mA	17	V_G = 17 V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	–	140	–	ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	–	195	–	ns	15	
output rise time	t_r	–	410	–	ns	15	
output fall time	t_f	–	75	–	ns	15	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

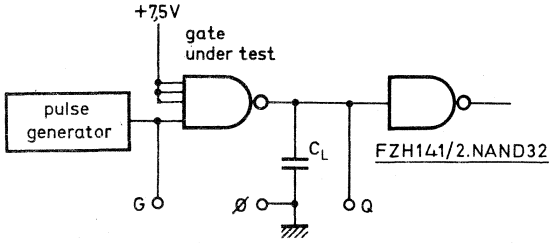
[2] Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = +4,5 V
t_f = 120 ns
t_{GH} = 1 µs



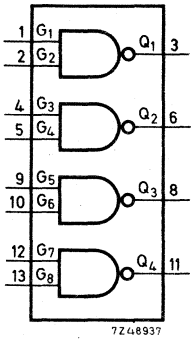
Measuring conditions: V_P = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
Slow-down terminals are not connected

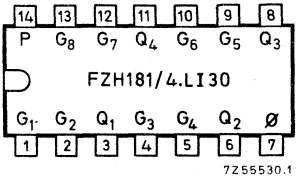
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE LOGIC INTERFACE GATE

5 V logic to HNIL



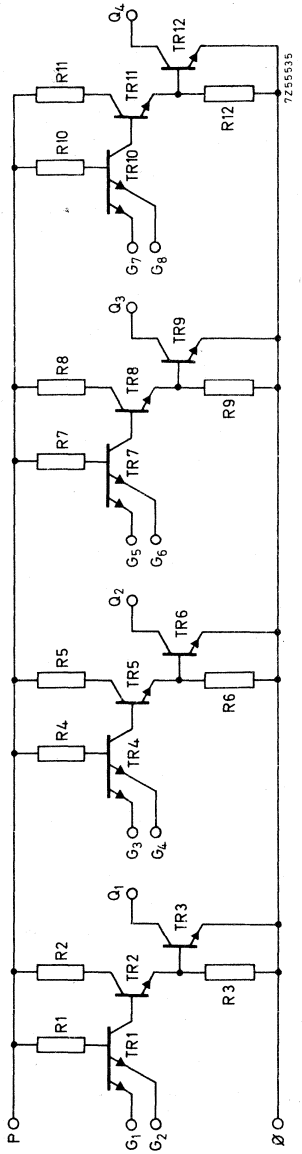


QUICK REFERENCE DATA				
Supply voltage	V_P		5±5%	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out (T_{amb} = 0 to +70 °C) LOW state	N_{aL}	max.	27	
Power consumption per gate at T_{amb} = 25 °C (50% duty cycle)	P_{av}	typ.	24	mW

The FZH181/4. LI30 is a level converter with open-collector outputs for interfacing TTL to HNIL and consists of 4 gates.

PACKAGE OUTLINE 14 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION

$Q = \overline{G_A \cdot G_B}$

(for positive logic)

Function table

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7	V
Output voltage	V_Q	max.	V_P	[1] ←
Input voltage	V_G	max.	5,5	V
Input current (V_P = 5 V)	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	5,5	V
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to	+70	°C
Uniform system supply voltage	V_P	4,75 to	5,25	V
Available d.c. fan-out	N_a	max.	27	
D.C. noise margin	M	min.	0,4	V
Supply current per gate; output HIGH (V_P = 5 V; V_G = 0 V)	I_{Pav}	max.	2,0	mA ←
output LOW (V_P = 5 V; V_G = 5 V)	I_{Pav}	max.	12,0	mA
Power consumption per gate at V_{Pmax} (50% duty cycle)	P_{tot}	max.	37	mW ←
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

[1]) For HNIL.

CHARACTERISTICS Test conditions: V_P = 5 V; T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1])	max.	Conditions and references: V_P (V)	Conditions and references:
Static data						
Voltages						
Input HIGH	V_{GH}	2,0	–	– V	4,75	V_{QL} = 1,0 V; I_{QL} = 50 mA
Input LOW	V_{GL}	–	–	0,8 V	4,75	V_{QH} = 18,0 V; I_{QH} = 250 µA
Output LOW	V_{QL}	–	–	0,4 V	4,75	V_{GH} = 2 V; I_{QL} = 16 mA
	V_{QL}	–	–	1,0 V	4,75	V_{GH} = 2 V; I_{QL} = 50 mA
D.C. noise margin: HIGH	M_H	0,4	–	– V		
LOW	M_L	0,4	–	– V		
Currents (per gate)						
Input HIGH	I_{GH}	–	–	40 µA	5,25	V_{GH} = 2,4 V
Input LOW	$-I_{GL}$	–	–	1,6 mA	5,25	V_{GL} = 0,4 V
Output HIGH	I_{QH}	–	–	250 µA	4,75	V_{QH} = 18 V; V_{GL} = 0,8 V
Output LOW	I_{QL}	50	–	– mA	4,75	V_{GH} = 2 V; V_{QL} = 1,0 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	1,0	2,0 mA	5	V_{GL} = 0 V
at V_{QL}	I_P	–	8,5	12,0 mA	5	V_{GH} = 5 V
Dynamic data						
Times						
Propagation						
fall time	t_{pdf}	–	20	60 ns	12	V_Q = 12 V; R_L = 390 Ω
rise time	t_{pdr}	–	130	300 ns	12	V_Q = 12 V; R_L = 3,9 kΩ

[1]) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Calculation of collector resistor R_Q

The collector resistor R_Q has to be calculated from voltages and input - and output currents of the gates.

$$R_{Qmax} = \frac{V_P - V_{QH} \quad (V)}{m \cdot I_{QH} + N \cdot I_{GH} \quad (\mu A)} \qquad R_{Qmin} = \frac{V_P - V_{QL} \quad (V)}{I_{QLmax} - N \cdot I_{GL} \quad (mA)}$$

m = number of interconnected outputs
N = number of used inputs
V_P = supply voltage of HNIL inputs
V_{QH} = output voltage HIGH of HNIL-circuit
V_{QL} = output voltage LOW of HNIL-circuit
I_{GH} = input current HIGH of HNIL-circuit
I_{GL} = input current LOW of HNIL-circuit

For interfacing TTL to HNIL (range I; V_P = 12 V)

$$R_{Qmax} = \frac{12 - 10 \quad (V)}{m \cdot 250 + N \cdot 1 \quad (\mu A)} \qquad R_{Qmin} = \frac{12 - 1,0 \quad (V)}{50 - N \cdot 1,5 \quad (mA)}$$

For interfacing TTL to HNIL (range II; V_P = 15 V)

$$R_{Qmax} = \frac{15 - 12 \quad (V)}{m \cdot 250 - N \cdot 1 \quad (\mu A)} \qquad R_{Qmin} = \frac{15 - 1,0 \quad (V)}{50 - N \cdot 1,8 \quad (mA)}$$

If FZH181/4. LI30 is used as wired-OR combination

HIGH state

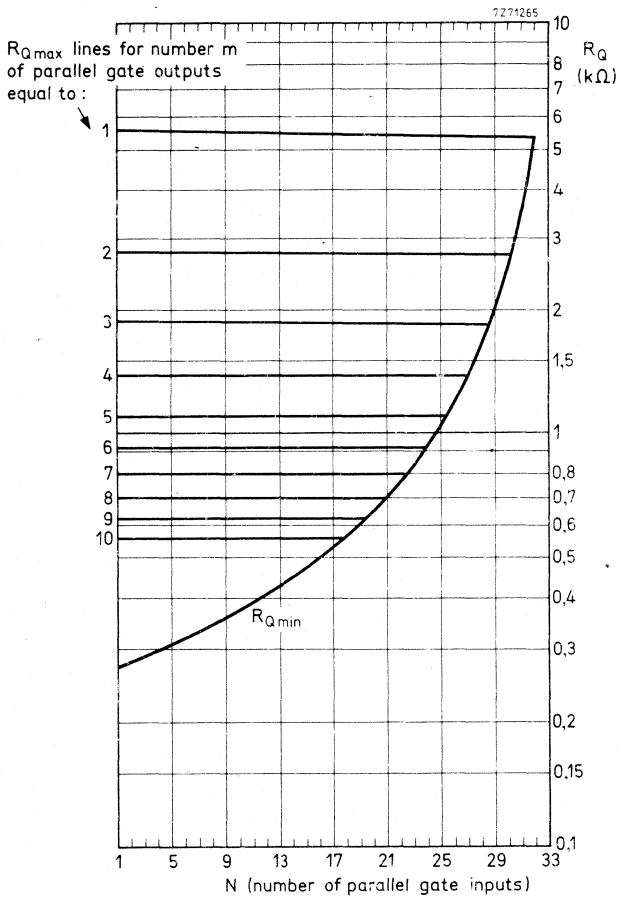
$$R_{Qmax} = \frac{V_P - 2,4 \quad (V)}{m \cdot 250 - N \cdot 40 \quad (\mu A)}$$

LOW state

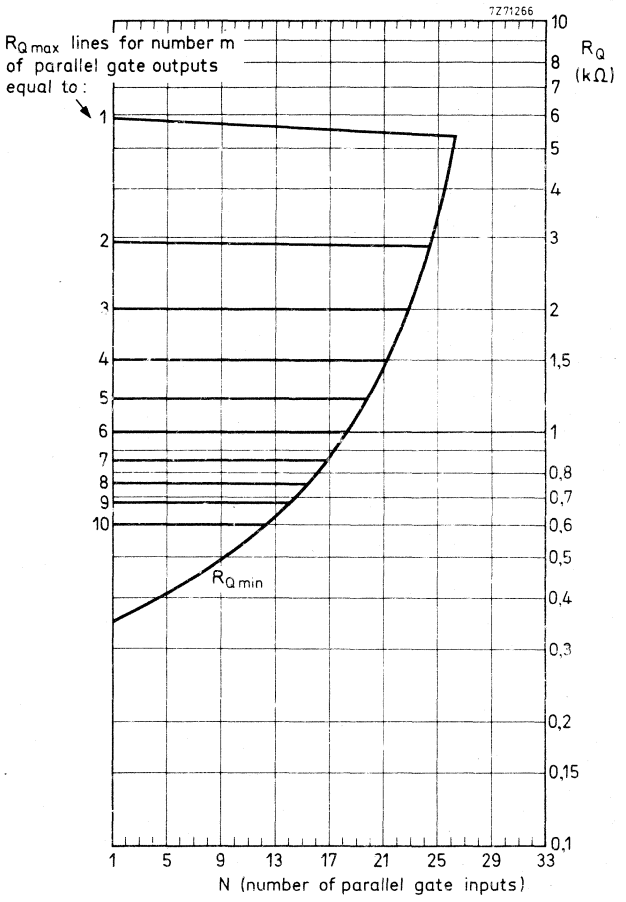
$$R_{Qmin} = \frac{V_P - 0,4 \quad (V)}{16 - N \cdot 1,6 \quad (mA)}$$

of which m = number of FZH181/4. LI30 OR combinations

N = number of used inputs



R_Q as a function of m and N at V_P = 12 V (range I).

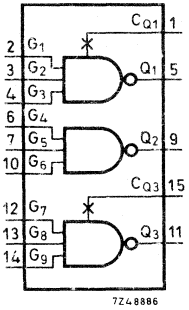


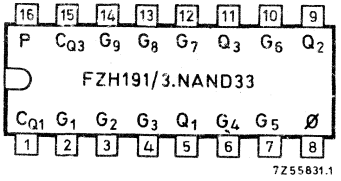
R_Q as a function of m and N at V_P = 15 V (range II).

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

TRIPLE 3-INPUT NAND GATE

with slow-down capability



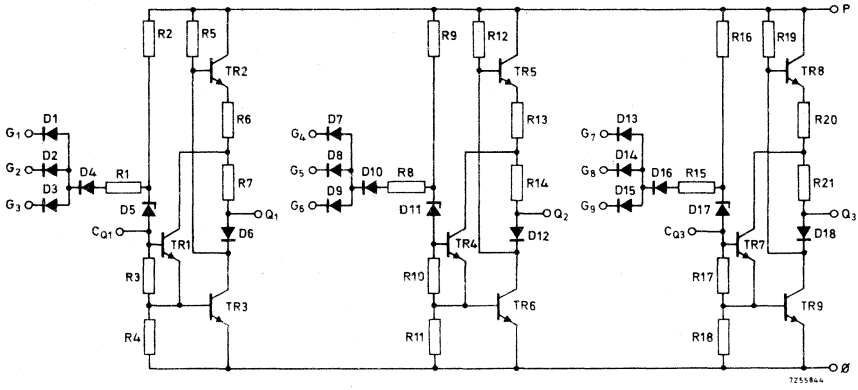


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}	0 to	+70	°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	170	ns
Available d.c. fan-out $T_{amb} = 0$ to +70 °C } LOW state	N_{aL}	max.	10	
D.C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	16	mW
range II: $V_P = 15$ V	P_{av}	typ.	27	mW

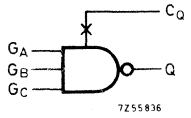
The FZH191/3.NAND33 consists of a number of independent NAND gates at which two NAND gates have a special terminal (C_Q). It is possible to connect a capacitor between the output (Q) and the corresponding slow-down terminal (C_Q) to increase the propagation delay.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$Q = \overline{G_A . G_B . G_C}$
(positive logic)

Function table

G_A	G_B	G_C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)	V_P	11,4 to 13,5		V
(range II)	V_P	13,5 to	17	V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current at range I ; output HIGH	I_{Pav}	typ.	0,9	mA
output LOW	I_{Pav}	typ.	1,7	mA
at range II ; output HIGH	I_{Pav}	typ.	1,2	mA
output LOW	I_{Pav}	typ.	2,3	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	31	mW
at range II ; V_{Pmax}	P_{tot}	max.	52	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

[1] Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.	Conditions and references: V_P (V)	Conditions and references
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4,5 V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	– V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7 V	11,4	V_{GH} = 7,5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	– V	11,4	
LOW	M_L	2,8	5,0	– V	11,4	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1,0 μA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5 mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	– mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	– mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25 mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	0,9	1,6 mA	13,5	V_G = 0 V
at V_{QL}	I_P	–	1,7	3,0 mA	13,5	V_G = 13,5 V
Dynamic data						
Times						
Propagation delay						
fall time	t_{pdf}	90	175	310 ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	90	175	310 ns	12	
output rise time	t_r	200	340	570 ns	12	
output fall time	t_f	70	120	210 ns	12	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

[2] Short-circuited duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

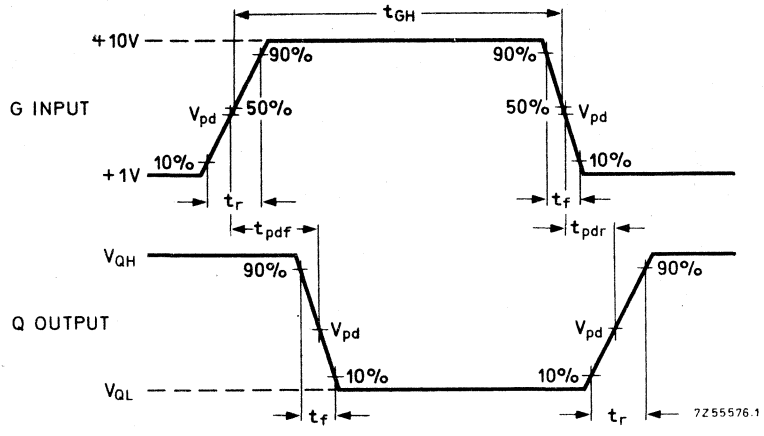
	Sym-bol	min.	typ.[1]	max.	Conditions and references: V_P (V)	Conditions and references
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	13,5	$V_{QL} \leqslant 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5 V	13,5 and 17	$V_{QH} \geqslant 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	– V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7 V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	– V	13,5	
LOW	M_L	2,8	5,0	– V	13,5	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1,0 μA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8 mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	– mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	– mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25 mA	17	V_G = 0 V; V_Q = 0 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	1,2	2,1 mA	17	V_G = 0 V
at V_{QL}	I_P	–	2,3	4,0 mA	17	V_G = 17 V
Dynamic data						
Times						
Propagation delay						
fall time	t_{pdf}	–	140	– ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{dp} = 4,5 V
rise time	t_{pdr}	–	195	– ns	15	
output rise time	t_r	–	410	– ns	15	
output fall time	t_f	–	75	– ns	15	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

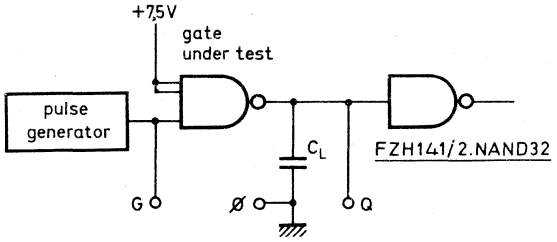
[2] Short-circuited duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = + 4,5 V
t_f = 120 ns
tGH = 1 µs

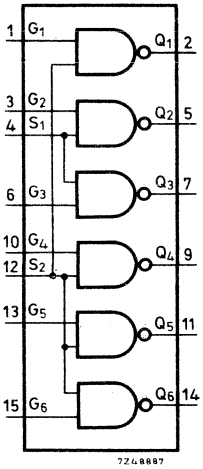


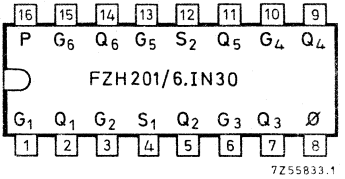
Measuring conditions: V_P = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
Slow-down terminals are not connected

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

SEXTUPLE INVERTER WITH STROBE INPUT



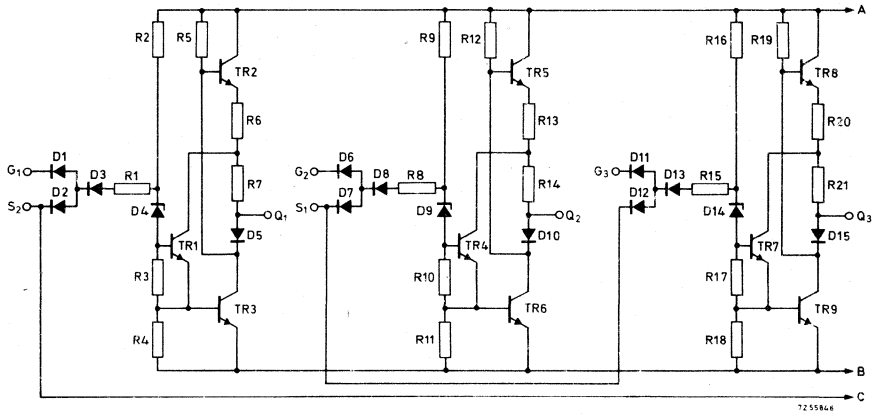


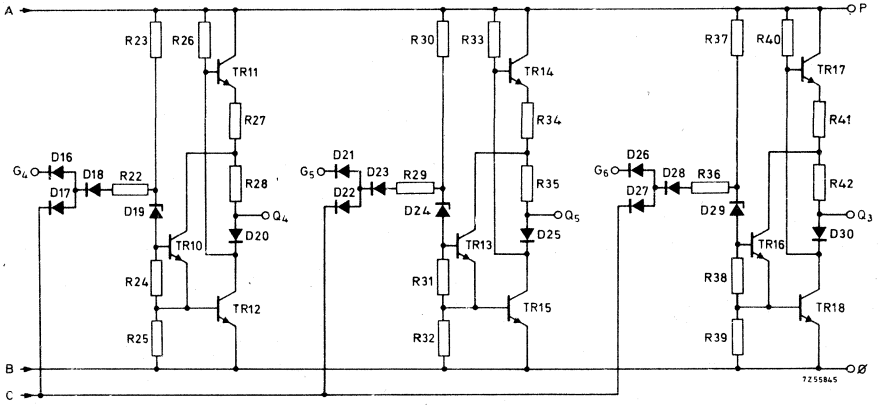
QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay time ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	170	ns
Available d.c. fan-out $T_{amb} = 0$ to +70 °C } LOW state	N_{aL}	max.	10	
D.C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	16	mW
range II: $V_P = 15$ V	P_{av}	typ.	27	mW

The FZH201/6.IN30 consists of a number of independent inverters without slow-down capability, but with a common strobe input.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM





LOGIC FUNCTION

$Q = \overline{G_A \cdot S}$ (positive logic)

Function table

G_A	S	Q
L	X	H
X	L	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.		18	V
Output voltage	V_Q	max.		V_P	
Input voltage	V_G	max.		18	V
Input current at V_P = 17 V	$-I_{GL}$	max.		25	mA
Voltage difference between any two inputs		max.		18	V
Storage temperature	T_{stg}	−65	to	+150	°C
Operating ambient temperature	T_{amb}	0	to	+70	°C
Output short-circuit duration	t_{Qsc}	max.		1	s [1]

[1] Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)	V_P	11,4 to 13,5		V
(range II)	V_P	13,5 to 17		V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current per gate; range I ; output HIGH	I_{Pav}	typ.	0,9	mA
output LOW	I_{Pav}	typ.	1,7	mA
range II; output HIGH	I_{Pav}	typ.	1,2	mA
output LOW	I_{Pav}	typ.	2,3	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	31	mW
at range II; V_{Pmax}	P_{tot}	max.	52	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.	Conditions and references: V_P (V)	Conditions and references:
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4,5 V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	– V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7 V	11,4	V_{GH} = 7,5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	– V	11,4	
LOW	M_L	2,8	5,0	– V	11,4	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1,0 µA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5 mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	– mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	– mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25 mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	0,9	1,6 mA	13,5	V_G = 0 V
at V_{QL}	I_P	–	1,7	3,0 mA	13,5	V_G = 13,5 V
Dynamic data						
Times						
Propagation delay: fall time	t_{pdf}	90	175	310 ns	12	
rise time	t_{pdr}	90	175	310 ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
output rise time	t_r	200	340	570 ns	12	
output fall time	t_f	70	120	210 ns	12	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

[2] Short-circuited duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

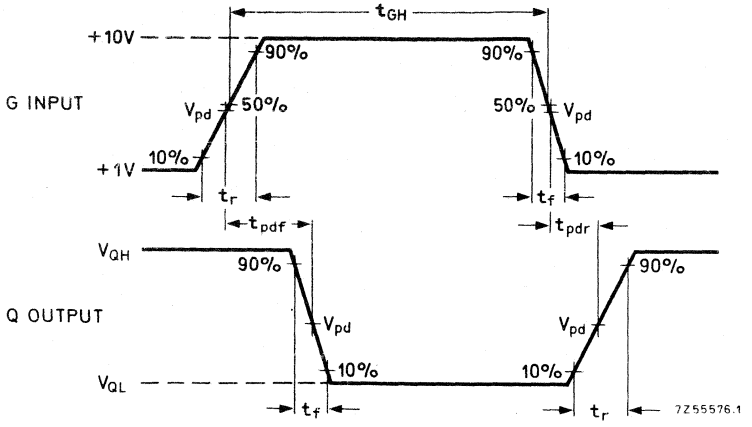
	Sym-bol	min.	typ.[1]	max.	Conditions and references: V_P (V)	Conditions and references
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	13,5	$V_{QL} \leqslant 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5 V	13,5 and 17	$V_{QH} \geqslant 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	– V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7 V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	– V	13,5	
LOW	M_L	2,8	5,0	– V	13,5	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1,0 µA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8 mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	– mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	– mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25 mA	17	V_G = 0 V; V_Q = 0 V
Dynamic data						
Currents (per gate)						
at V_{QH}	I_P	–	1,2	2,1 mA	17	V_G = 0 V
at V_{QL}	I_P	–	2,3	4,0 mA	17	V_G = 17 V
Supply data						
Times						
Propagation delay:						
fall time	t_{pdf}	–	140	– ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	–	195	– ns	15	
output rise time	t_r	–	410	– ns	15	
output fall time	t_f	–	75	– ns	15	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

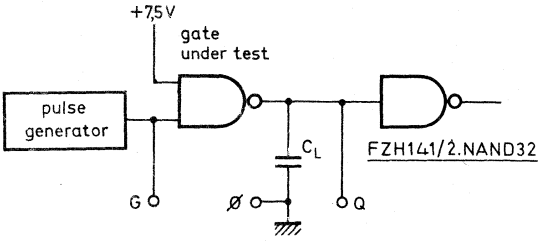
[2] Short-circuited duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = + 4,5 V
t_f = 120 ns
t_{GH} = 1 µs



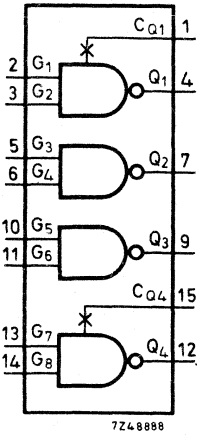
Measuring conditions: V_P = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

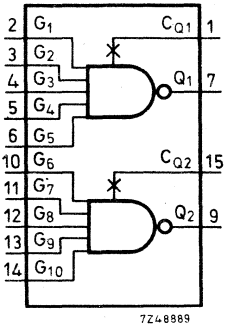
The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE 2-INPUT NAND GATE
DUAL 5-INPUT NAND GATE

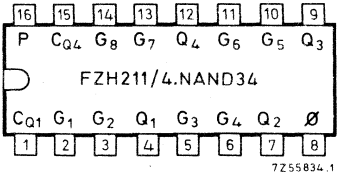
both having slow-down capability and open collector

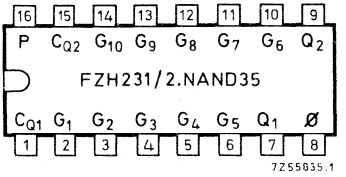


FZH211/4.NAND34



FZH231/2.NAND35





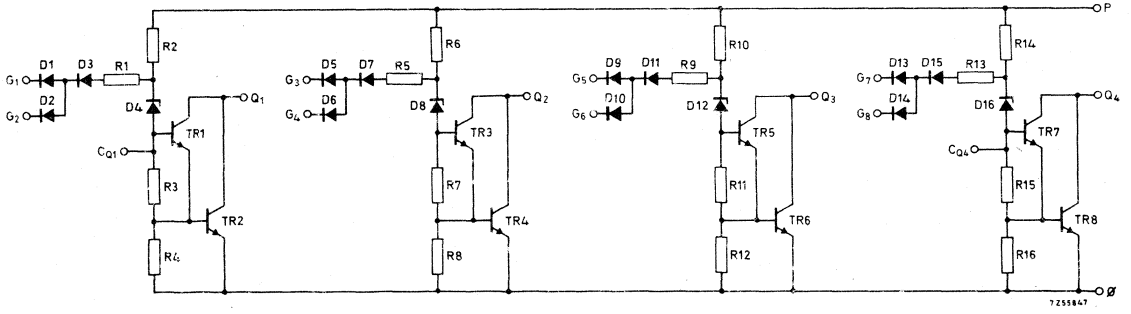
QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out T_{amb} = 0 to +70 °C } LOW state	N_{aL}	max.	10	
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II: V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at T_{amb} = 25 °C				
(50% duty cycle) range I: V_P = 12 V	P_{av}	typ.	8,5	mW
range II: V_P = 15 V	P_{av}	typ.	15	mW

The FZH211/4.NAND34 and FZH231/2.NAND35 consist of a number of independent NAND gates with open collector and two gates of each circuit have a slow-down terminal. It is possible to connect a capacitor between the output Q and the corresponding slow-down terminal C_Q to increase the propagation delay.
The outputs of these gates may be interconnected to perform the AND-OR-NOT function.

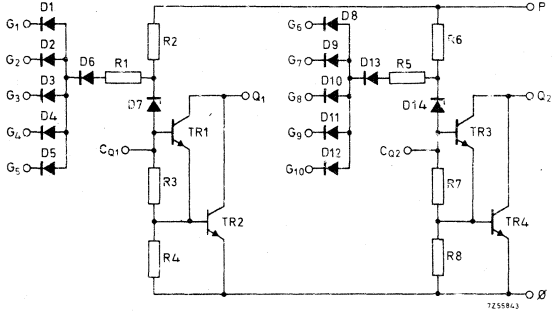
PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAMS

FZH211/4.NAND34



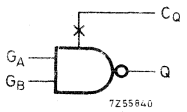
FZH231/2.NAND35



LOGIC FUNCTION

1. Individual gate operation

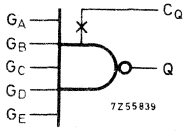
FZH211/4.NAND34



$$Q = \overline{G_A \cdot G_B}$$

(positive logic)

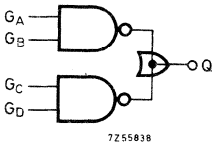
FZH231/2.NAND35



$$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot G_E}$$

(positive logic)

2. Wired-OR combination



$$Q = \overline{(G_A \cdot G_B)} \cdot \overline{(G_C \cdot G_D)} = \overline{(G_A \cdot G_B) + (G_C \cdot G_D)}$$

(positive logic)

FUNCTION TABLES

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

G_A	G_B	G_C	G_D	G_E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

G_A	G_B	G_C	G_D	Q
L	X	L	X	H
L	X	X	L	H
X	L	X	L	H
X	L	L	X	H
H	H	X	X	L
X	X	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)	V_P	11,4 to 13,5		V
(range II)	V_P	13,5 to	17	V
Available d.c. fan-out	N_{aL}	max.	10	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current per gate; range I; output HIGH	I_{Pav}	max.	2,1	mA
output LOW	I_{Pav}	max.	1,2	mA
range II; output HIGH	I_{Pav}	max.	2,1	mA
output LOW	I_{Pav}	max.	1,4	mA
Power consumption per gate (50% duty cycle) at range I; V_{Pmax}	P_{tot}	max.	18	mW
at range II; V_{Pmax}	P_{tot}	max.	30	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ.[1])	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4,5	V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	V_{GH} = 7,5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5	mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	I_{QH}	–	–	80	µA	11,4	V_{GL} = 4,5 V; V_{QH} = 18 V
Output LOW	I_{QL}	15	–	–	mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	1,0	1,7	mA	13,5	V_G = 0 V
at V_{QL}	I_P	–	0,4	1,0	mA	13,5	V_G = 13,5 V

[1]) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1])	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8	mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	I_{QH}	–	–	80	µA	13,5	V_{GL} = 4,5 V; V_{QH} = 18 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	1,3	2,1	mA	17	V_G = 0 V
at V_{QL}	I_P	–	0,7	1,4	mA	17	V_G = 17 V

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

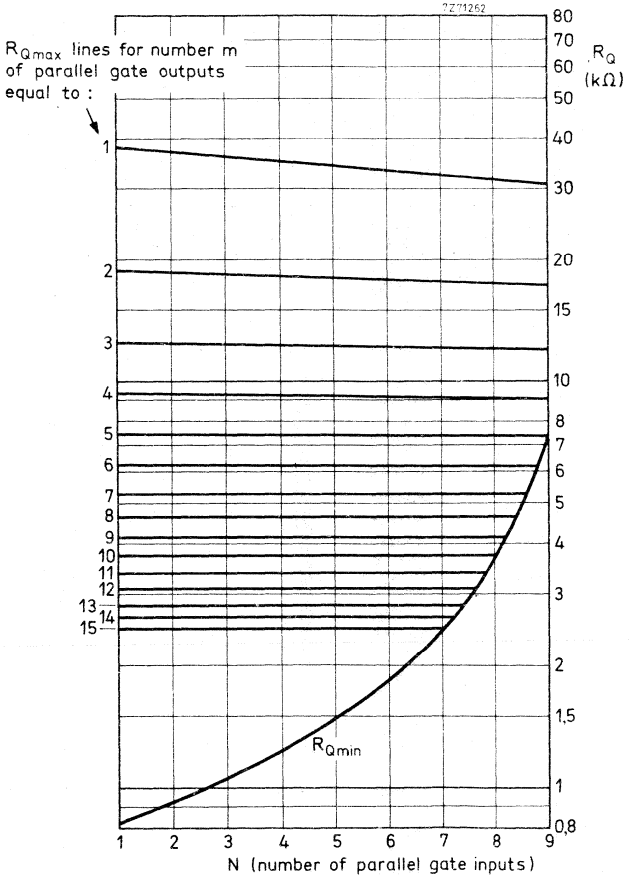
CHARACTERISTICS (continued)

Calculation of collector resistor R_Q

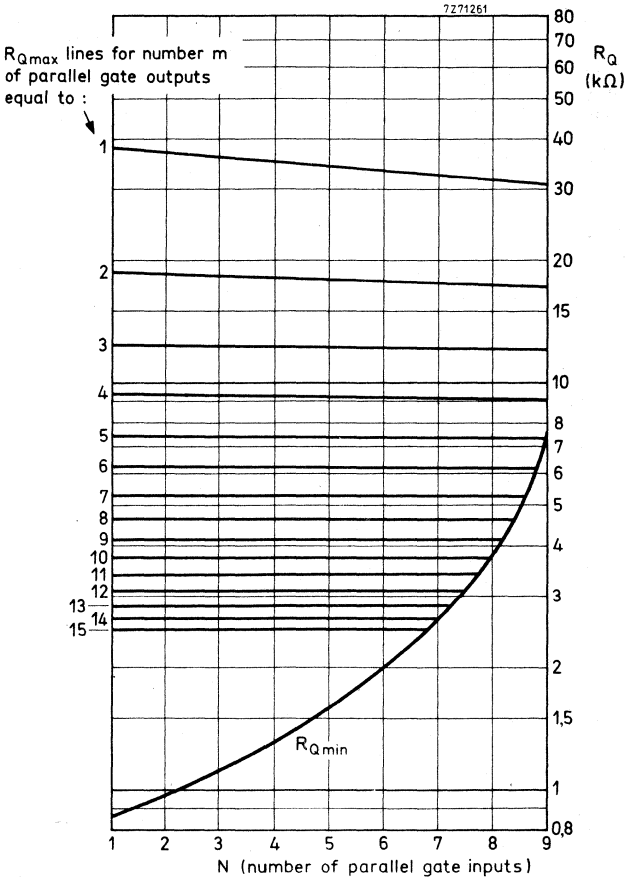
The collector resistor R_Q has to be calculated from voltages and input- and output currents of the gates.

$$R_{Qmax} = \frac{V_P - V_{QH} \quad (V)}{m \cdot I_{QH} + N \cdot I_{GH} \quad (\mu A)} \qquad R_{Qmin} = \frac{V_P - V_{QL} \quad (V)}{I_{QLmax} - N \cdot I_{GL} \quad (mA)}$$

m = number of interconnected outputs
N = number of used inputs
V_P = supply voltage of HNIL inputs
V_{QH} = output voltage HIGH of HNIL - circuit
V_{QL} = output voltage LOW of HNIL - circuit



R_Q as a function of m and N at V_P = 12 V (range I).

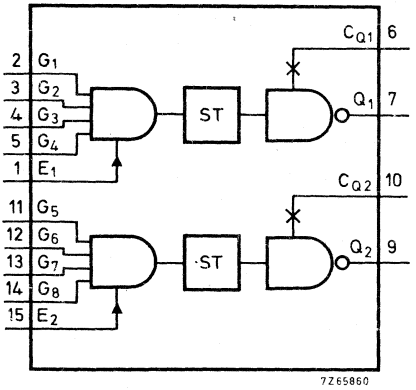


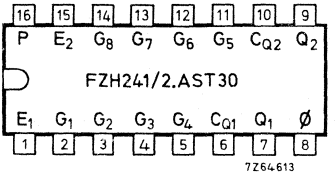
R_Q as a function of m and N at V_P = 15 V (range II).

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL 4-INPUT NAND SCHMITT TRIGGER

with slow-down capability and expandable inputs



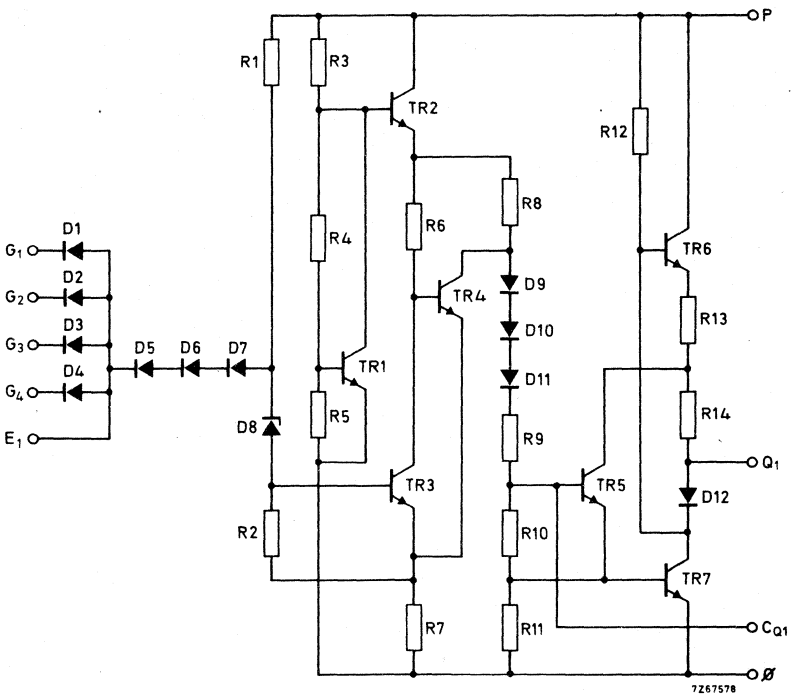


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out T_{amb} = 0 to +70 °C } LOW state	N_{aL}	max.	10	
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II: V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at T_{amb} = 25 °C (50% duty cycle) range I : V_P = 12 V	P_{av}	typ.	48	mW
range II: V_P = 15 V	P_{av}	typ.	72	mW

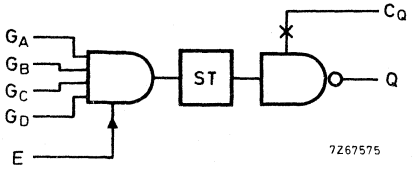
The FZH241/2.AST30 consists of two identical 4-input NAND SCHMITT triggers with slow-down capability and expandable inputs.
Each circuit functions as a 4-input NAND gate (without using the expandable input), but because of the SCHMITT action, the gate has different input threshold levels for positive- and negative-going signals. The hysteresis, which is the difference between the two threshold levels, is typically 900 mV.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot E}$$

FUNCTION TABLE

G_A	G_B	G_C	G_D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)	V_P	11,4 to 13,5		V
(range II)	V_P	13,5 to	17	V
Available d.c. fan-out; LOW state	N_{aL}	max.	10	
HIGH state	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current per gate: range I : output HIGH	I_{Pav}	typ.	4,0	mA
output LOW	I_{Pav}	typ.	3,8	mA
range II: output HIGH	I_{Pav}	typ.	4,5	mA
output LOW	I_{Pav}	typ.	5,0	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	85	mW
at range II; V_{Pmax}	P_{tot}	max.	105	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

[1]) Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ.[1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	8,0	–	–	V	11, 4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	5,0	V	11, 4 and 13, 5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	–	V	11, 4 and 13, 5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	11, 4	V_{GH} = 8,0 V; I_{QL} = 15 mA
Positive-going threshold voltage	V_{TP}	–	7,1	–	V	12	
Negative-going threshold voltage	V_{TN}	–	6,2	–	V	12	
Hysteresis [2]	V_H	–	0,9	–	V	12	
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V	11, 4	
LOW	M_L	2,8	5,0	–	V	11, 4	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	13, 5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	–	1,5	mA	13, 5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11, 4 and 13, 5	V_{GL} = 5,0 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	–	mA	11, 4	V_{GH} = 8,0 V; V_{QL} = 1,7 V
Output short-circuited [3]	$-I_{Qsc}$	9	15	25	mA	13, 5	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	4,0	6,3	mA	13, 5	V_G = 0 V
at V_{QL}	I_P	–	3,8	6,0	mA	13, 5	V_G = 13,5 V

1) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
2) $V_H = V_{TP} - V_{TN}$.
3) Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

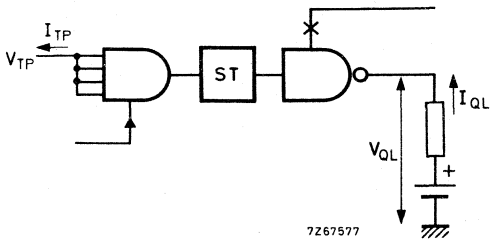
	Symbol	min.	typ.[1])	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	8,0	–	–	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	5,0	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,1	1,7	V	13,5	V_{GH} = 8,0 V; I_{QL} = 18 mA
Positive-going threshold voltage	V_{TP}	–	7,05	–	V	15	
Negative-going threshold voltage	V_{TN}	–	6,15	–	V	15	
Hysteresis [2])	V_H	–	0,9	–	V	15	
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	μA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	–	1,8	mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5 and 17	V_{GL} = 5,0 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{GH} = 8,0 V; V_{QL} = 1,7 V
Output short-circuited [3])	$-I_{Qsc}$	9	15	25	mA	17	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	4,5	7,3	mA	17	V_G = 0 V
at V_{QL}	I_P	–	5,0	8,0	mA	17	V_G = 17 V

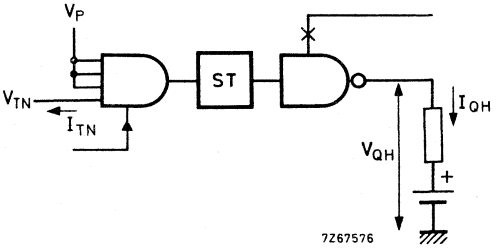
1) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.
2) $V_H = V_{TP} - V_{TN}$.
3) Short-circuit duration max. 1 s.

CHARACTERISTICS

D.C. test circuit for V_{TP}, V_{TN} and V_H

conditions: V_P = 12 V (range I); ϕ to earth;
V_P = 15 V (range II); T_{amb} = 25 °C

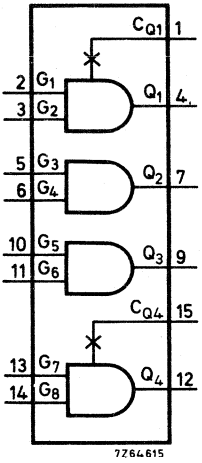


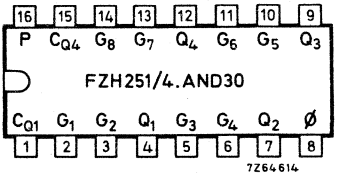


The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE 2–INPUT AND GATE

with slow-down capability



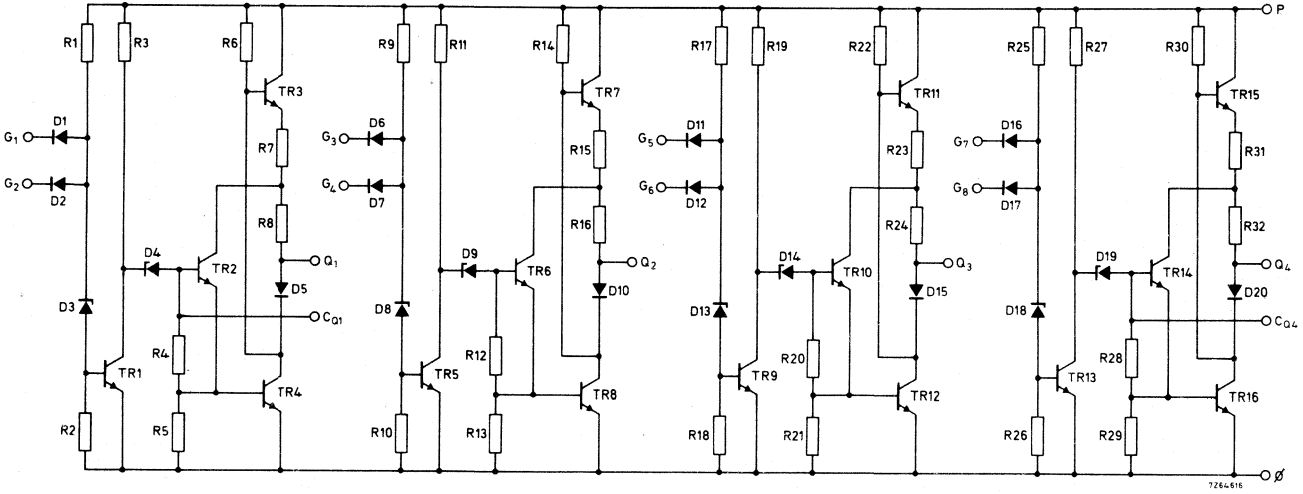


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay N = 1; C_L = 10 pF; T_{amb} = 25 °C; V_{pd} = 4,5 V	t_{pd}	typ.	260	ns
Available d.c. fan-out T_{amb} = 0 to +70 °C } LOW state	N_{aL}	max.	10	
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II: V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at T_{amb} = 25 °C				
(50 % duty cycle) range I : V_P = 12 V	P_{av}	typ.	24	mW
range II: V_P = 15 V	P_{av}	typ.	42,8	mW

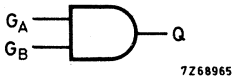
The FZH251/4.AND30 consists of four 2-input AND gates, two of which may be slowed down.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTIONS



Function table

G_A	G_B	Q
L	X	L
X	L	L
H	H	H

$Q = G_A . G_B$ (positive logic)

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)	V_P	11,4 to 13,5		V
(range II)	V_P	13,5 to 17		V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current per gate: range I; output HIGH	I_{Pav}	typ.	1,6	mA
output LOW	I_{Pav}	typ.	2,4	mA
range II; output HIGH	I_{Pav}	typ.	2,2	mA
output LOW	I_{Pav}	typ.	3,5	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	51,5	mW
at range II; V_{Pmax}	P_{tot}	max.	84	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

[1]) Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	11,4	$V_{QL} \leq 1,7$ V; $I_{QL} = 15$ mA
Input LOW	V_{GL}	–	–	4,5	V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH} = 0,1$ mA
Output HIGH	V_{QH}	10,0	11,3	–	V	11,4 and 13,5	$V_{GL} = 4,5$ V; $-I_{QH} = 0,1$ mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	$V_{GH} = 7,5$ V; $I_{QL} = 15$ mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	13,5	$V_{GH} = 13,5$ V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5	mA	13,5	$V_{GL} = 1,7$ V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4 and 13,5	$V_{GL} = 4,5$ V; $V_{QH} = 10$ V
Output LOW	I_{QL}	15	–	–	mA	11,4	$V_{GH} = 7,5$ V; $V_{QL} = 1,7$ V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	13,5	$V_G = 0$ V; $V_Q = 0$ V
Supply data							
Currents (per gate)							
at V_{QL}	I_P	–	3	4,5	mA	13,5	$V_G = 0$ V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	90	175	310	ns	12	$C_L = 10$ pF; N = 1; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V
rise time	t_{pdr}	200	340	570	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
[2]) Short-circuit duration max. 1 s.

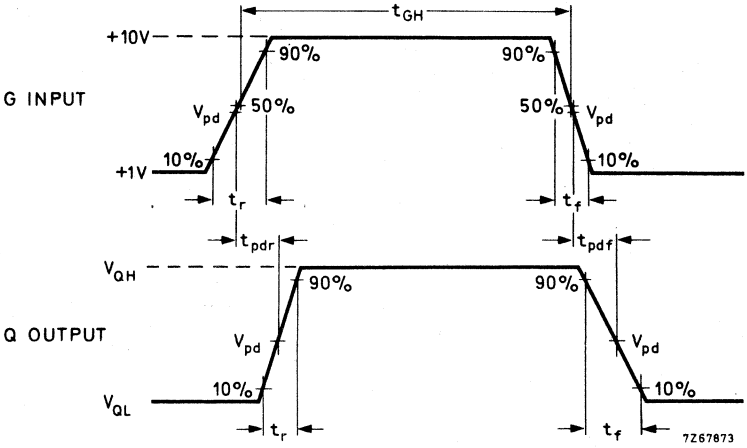
CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; $I_{QL} = 18$ mA
Input LOW	V_{GL}	–	–	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-i_{QH} = 0,1$ mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5 and 17	$V_{GL} = 4,5$ V; $-I_{QH} = 0,1$ mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	$V_{GH} = 7,5$ V; $I_{QL} = 18$ mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	μA	17	$V_{GH} = 17$ V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8	mA	17	$V_{GL} = 1,7$ V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5 and 17	$V_{GL} = 4,5$ V; $V_{QH} = 12$ V
Output LOW	I_{QL}	18	–	–	mA	13,5	$V_{GH} = 7,5$ V; $V_{QL} = 1,7$ V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	17	$V_G = 0$ V; $V_Q = 0$ V
Supply data							
Currents (per gate)							
at V_{QL}	I_P	–	3,7	6	mA	17	$V_G = 0$ V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	–	t.b.f.	–	ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	–	t.b.f.	–	ns	15	
output rise time	t_r	–	t.b.f.	–	ns	15	
output all time	t_f	–	t.b.f.	–	ns	15	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.
[2]) Short-circuit duration max. 1 s.

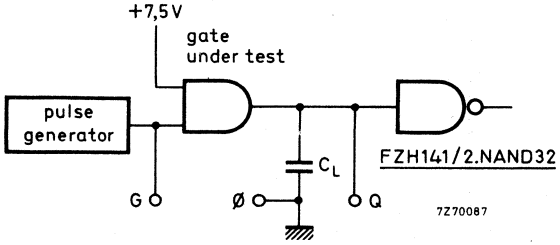
CHARACTERISTICS

Dynamic data



Pulse generator (G-input): t_r = 350 ns
t_f = 120 ns
t_{GH} = 1 µs

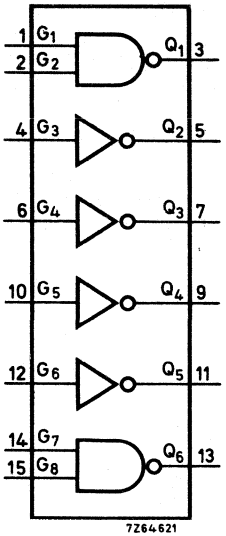
V_{pd} = + 4, 5 V



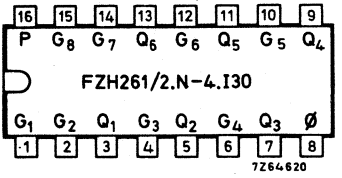
Measuring conditions: V_P = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C.

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.



DUAL NAND GATE/ QUADRUPLE INVERTER

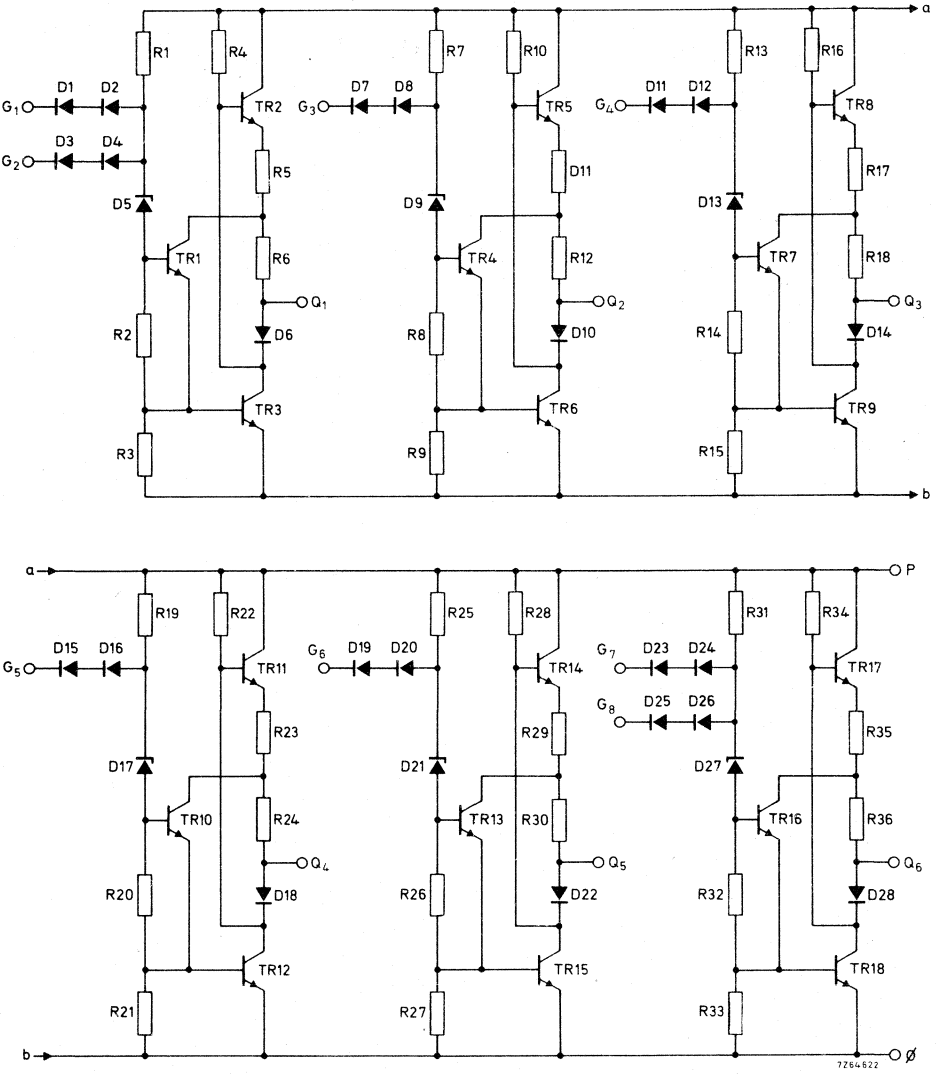


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	175	ns
Available d.c. fan-out $T_{amb} = 0$ to +70 °C } LOW state	N_{aL}	max.	10	
D.C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	16,2	mW
range II: $V_P = 15$ V	P_{av}	typ.	28,5	mW

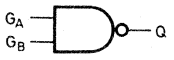
The FZH261/2.N-4.I30 consists of two 2-input NAND gates and four inverters, none of which have the slow-down facility.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



7Z55522

$Q = \overline{G_A . G_B}$ (positive logic)

Function table

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

7Z69007

$Q = \overline{G_C}$ (positive logic)

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C
Uniform system supply voltage (range I)	V_P		11,4 to 13,5	V
(range II)	V_P		13,5 to 17	V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min	2,8	V
	M_H	min	4,5	V
→ Supply current per gate; range I; output HIGH	I_{Pav}	typ.	1,0	mA
output LOW	I_{Pav}	typ.	1,7	mA
range II; output HIGH	I_{Pav}	typ.	1,4	mA
output LOW	I_{Pav}	typ.	2,4	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	34,3	mW
at range II; V_{Pmax}	P_{tot}	max.	56	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references: V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	11,4	$V_{QL} \leq 1,7$ V; $I_{QL} = 15$ mA
Input LOW	V_{GL}	–	–	4,5	V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH} = 0,1$ mA
Output HIGH	V_{QH}	10,0	11,3	–	V	11,4 and 13,5	$V_{GL} = 4,5$ V; $-I_{QH} = 0,1$ mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	$V_{GH} = 7,5$ V; $I_{QL} = 15$ mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	μA	13,5	$V_{GH} = 13,5$ V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5	mA	13,5	$V_{GL} = 1,7$ V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4 and 13,5	$V_{GL} = 4,5$ V; $V_{QH} = 10$ V
Output LOW	I_{QL}	15	–	–	mA	11,4	$V_{GH} = 7,5$ V; $V_{QL} = 1,7$ V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	13,5	$V_G = 0$ V; $V_Q = 0$ V
Supply data							
Currents (per gate)							
at V_{QL}	I_P	–	1,7	3	mA	13,5	$V_G = 13,5$ V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	90	175	310	ns	12	$C_L = 10$ pF; N = 1; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V
rise time	t_{pdr}	90	175	310	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

[2] Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

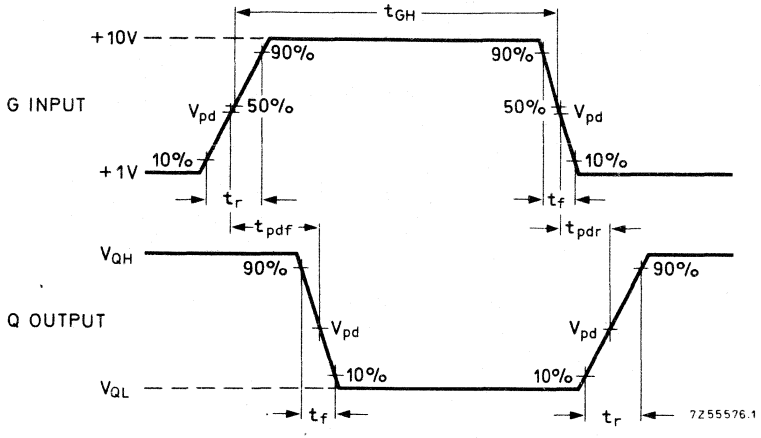
	Sym-bol	min.	typ. [1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8	mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	17	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QL}	I_P	–	2,4	4	mA	17	V_G = 17 V
Dynamic data							
Times							
Propagation delay fall time	t_{pdf}	–	t.b.f.	–	ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	–	t.b.f.	–	ns	15	
output rise time	t_r	–	t.b.f.	–	ns	15	
output fall time	t_f	–	t.b.f.	–	ns	15	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

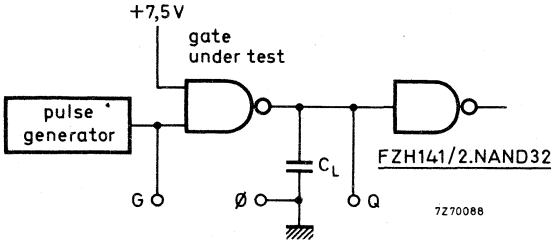
[2] Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = +4,5 V
t_f = 120 ns
t_{GH} = 1 µs

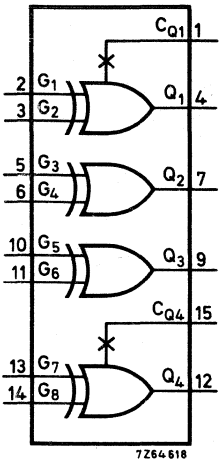


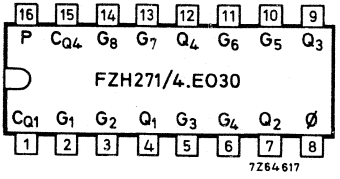
Measuring conditions: V_P = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE EXCLUSIVE-OR GATE
with slow-down capability



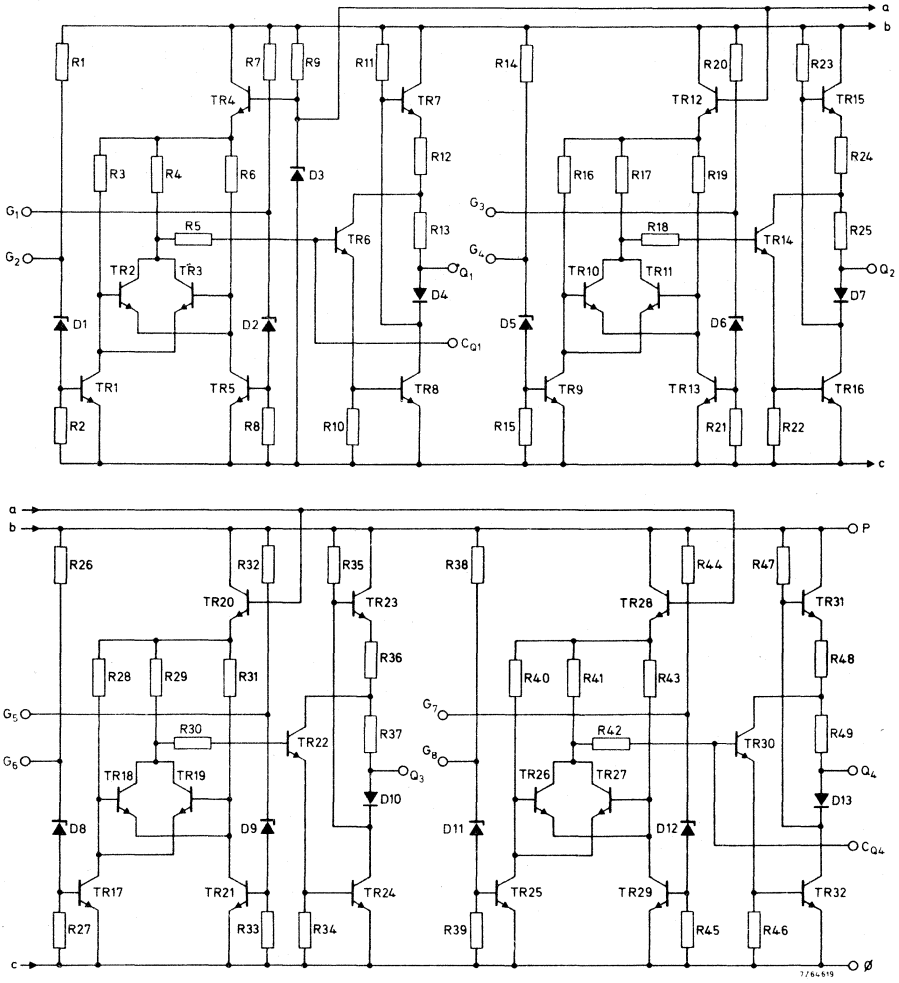


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay N = 1; C_L = 10 pF; T_{amb} = 25 °C; V_{pd} = 4,5 V	t_{pd}	typ.	260	ns
Available d.c. fan-out T_{amb} = 0 to +70 °C } LOW state	N_{aL}	max.	10	
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II: V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at T_{amb} = 25 °C				
(50% duty cycle) range I : V_P = 12 V	P_{av}	typ.	43,5	mW
range II: V_P = 15 V	P_{av}	typ.	66,8	mW

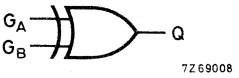
The FZH271/4.EO30 consists of four 2-input EXCLUSIVE-OR gates, two of which may be slowed down.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$Q = G_A.\overline{G}_B + \overline{G}_A.G_B$ (positive logic)

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

Function table

G_A	G_B	Q
L	L	L
H	L	H
L	H	H
H	H	L

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C
Uniform system supply voltage (range I)	V_P		11,4 to 13,5	V
(range II)	V_P		13,5 to 17	V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Suppy current per gate; range I ; output HIGH	I_{Pav}	typ.	3,45	mA
output LOW	I_{Pav}	typ.	3,8	mA
range II; output HIGH	I_{Pav}	typ.	4,1	mA
output LOW	I_{Pav}	typ.	4,8	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	76,8	mW
at range II; V_{Pmax}	P_{tot}	max.	114,8	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	11,4	$V_{QL} \leq 1,7$ V; $I_{QL} = 15$ mA
Input LOW	V_{GL}	–	–	4,5	V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH} = 0,1$ mA
Output HIGH	V_{QH}	10,0	11,3	–	V	11,4 and 13,5	$V_{GL} = 4,5$ V; $-I_{QH} = 0,1$ mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	$V_{GH} = 7,5$ V; $I_{QL} = 15$ mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	13,5	$V_{GH} = 13,5$ V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5	mA	13,5	$V_{GL} = 1,7$ V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4 and 13,5	$V_{GL} = 4,5$ V; $V_{QH} = 10$ V
Output LOW	I_{QL}	15	–	–	mA	11,4	$V_{GH} = 7,5$ V; $V_{QL} = 1,7$ V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	13,5	$V_G = 0$ V; $V_Q = 0$ V
Supply data							
Currents (per gate)							
at V_{QL}	I_P	–	3,8	6	mA	13,5	$V_G = 13,5$ V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	90	175	310	ns	12	$C_L = 10$ pF; N = 1; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V
rise time	t_{pdr}	200	340	570	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

[2] Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

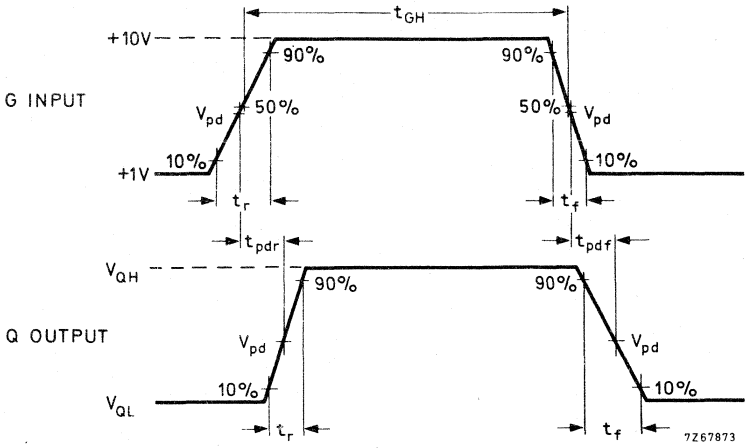
	Sym-bol	min.	typ. [1]	max.		Conditions and references: V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	μA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8	mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	17	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QL}	I_P	–	4,8	7,5	mA	17	V_G = 17 V
Dynamic data							
Times							
Propagation delay fall time	t_{pdf}	–	t.b.f.	–	ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
Propagation delay rise time	t_{pdr}	–	t.b.f.	–	ns	15	
output rise time	t_r	–	t.b.f.	–	ns	15	
output fall time	t_f	–	t.b.f.	–	ns	15	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

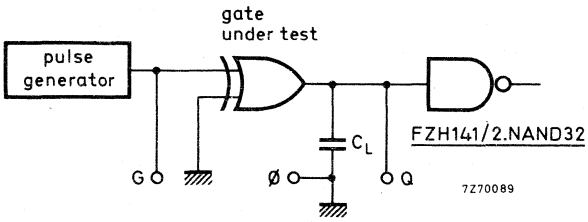
[2] Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = + 4,5 V
t_f = 120 ns
t_{GH} = 1 µs

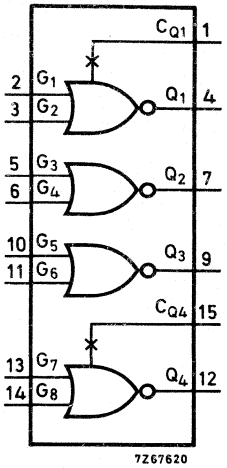


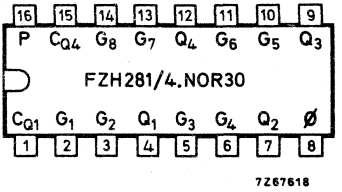
Measuring conditions: V_P = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE NOR GATE
with slow-down capability



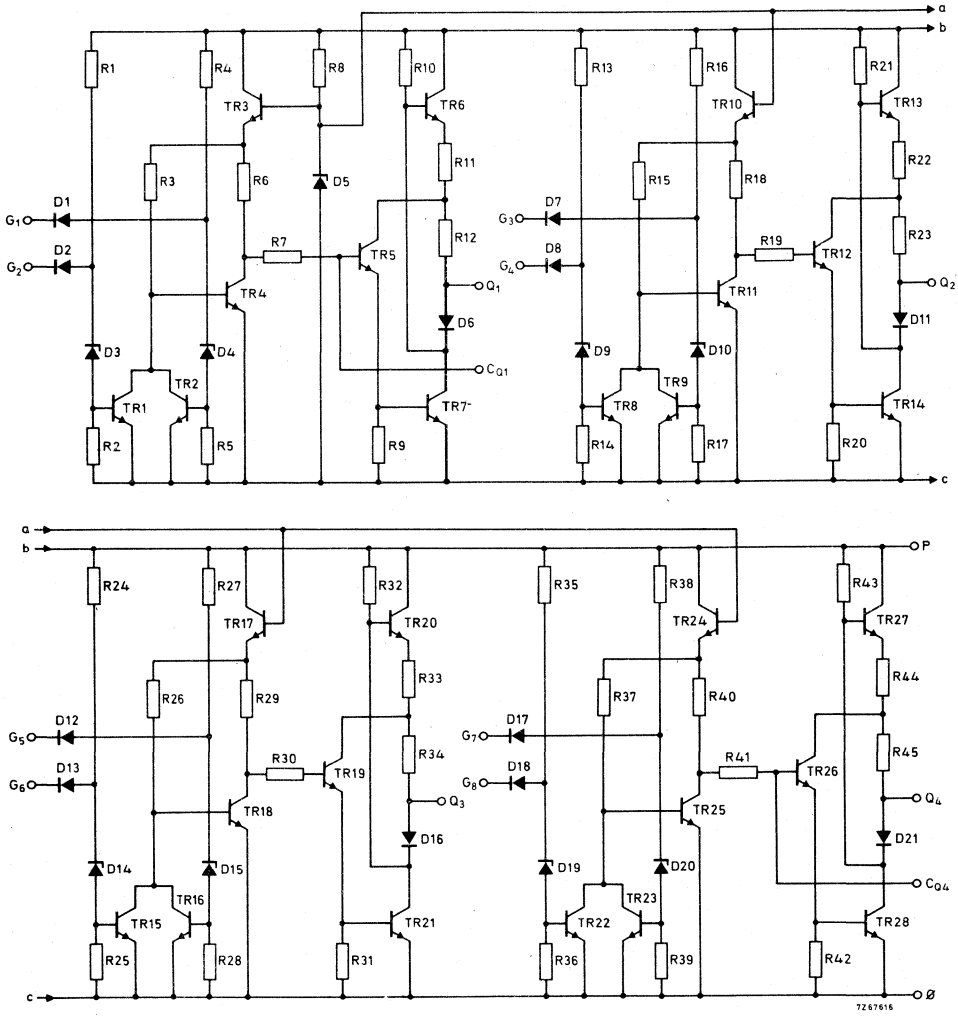


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	260	ns
Available d.c. fan-out, $T_{amb} = 0$ to +70 °C; LOW state	N_{aL}	max.	10	
D.C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	42	mW
range II: $V_P = 15$ V	P_{av}	typ.	63,8	mW

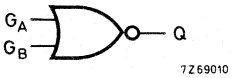
The FZH281/4.NOR30 consists of four 2-input NOR gates, two of which have the slow-down facility.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$Q = \overline{G_A + G_B}$ (positive logic)

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

Function table

G_A	G_B	Q
L	L	H
H	X	L
X	H	L

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C
Uniform system supply voltage (range I)	V_P		11,4 to 13,5	V
(range II)	V_P		13,5 to 17	V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current per gate; range I ; output HIGH	I_{Pav}	typ.	3,3	mA
output LOW	I_{Pav}	typ.	3,7	mA
range II; output HIGH	I_{Pav}	typ.	3,8	mA
output LOW	I_{Pav}	typ.	4,7	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	76,8	mW
at range II; V_{Pmax}	P_{tot}	max.	114,8	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references: V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4,5	V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	–	V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	V_{GH} = 7,5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5	mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	–	mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QL}	I_P	–	3,7	6	mA	13,5	V_G = 13,5 V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	200	340	570	ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	90	175	310	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

[2] Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

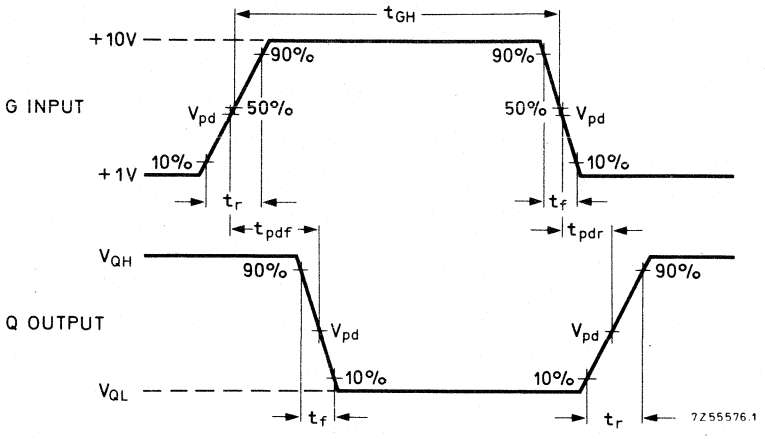
	Symbol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; $I_{QL} = 18$ mA
Input LOW	V_{GL}	–	–	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH} = 0,1$ mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5 and 17	$V_{GL} = 4,5$ V; $-I_{QH} = 0,1$ mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	$V_{GH} = 7,5$ V; $I_{QL} = 18$ mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	μA	17	$V_{GH} = 17$ V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8	mA	17	$V_{GL} = 1,7$ V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5 and 17	$V_{GL} = 4,5$ V; $V_{QH} = 12$ V
Output LOW	I_{QL}	18	–	–	mA	13,5	$V_{GH} = 7,5$ V; $V_{QL} = 1,7$ V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	17	$V_G = 0$ V; $V_Q = 0$ V
Supply data							
Currents (per gate)							
at V_{QL}	I_P	–	4,7	7,5	mA	17	$V_G = 17$ V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	–	t.b.f.	–	ns	15	$C_L = 10$ pF; N = 1; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V
rise time	t_{pdr}	–	t.b.f.	–	ns	15	
output rise time	t_r	–	t.b.f.	–	ns	15	
output fall time	t_f	–	t.b.f.	–	ns	15	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

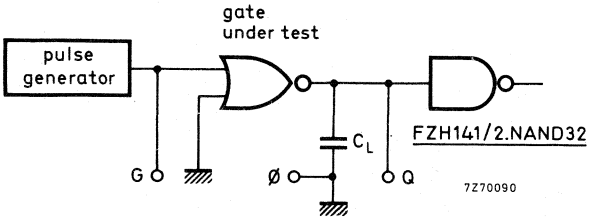
[2]) Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = +4,5 V
t_f = 120 ns
t_{GH} = 1 µs

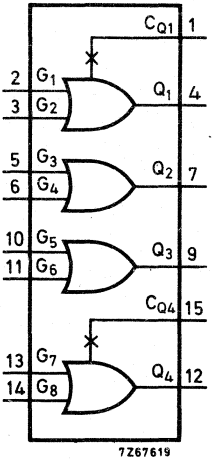


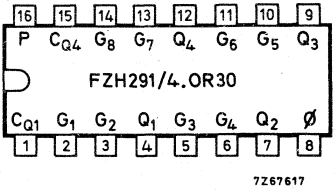
Measuring conditions: V_P = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE OR GATE
with slow-down capability



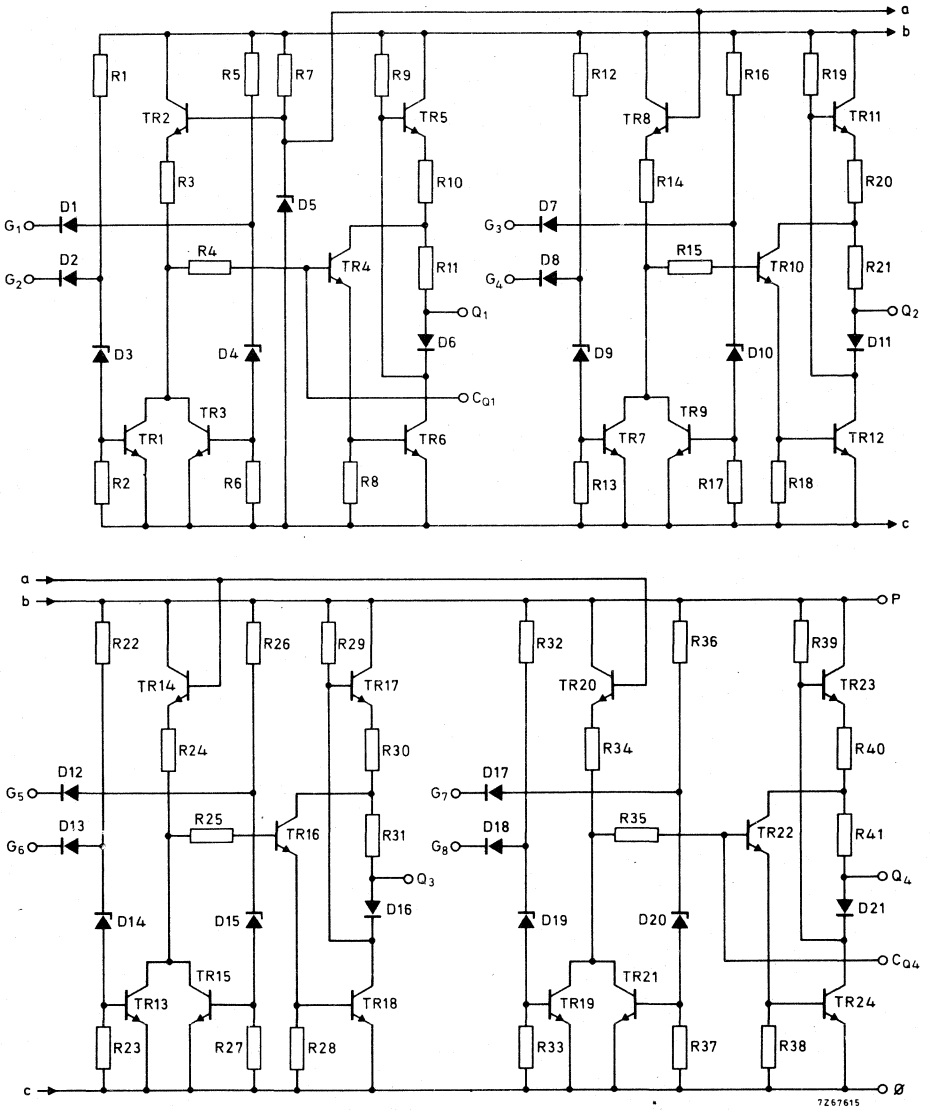


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	260	ns
Available d.c. fan-out, $T_{amb} = 0$ to +70 °C; LOW state	N_{aL}	max.	10	
D.C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	35,1	mW
range II: $V_P = 15$ V	P_{av}	typ.	54	mW

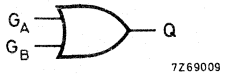
The FZH291/4.OR30 consists of four 2-input OR gates, two of which may be slowed down.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$Q = G_A + G_B$ (positive logic)

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

Function table

G_A	G_B	Q
L	L	L
H	X	H
X	H	H

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C
Uniform system supply voltage (range I)	V_P		11,4 to 13,5	V
(range II)	V_P		13,5 to 17	V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current per gate; range I ; output HIGH	I_{Pav}	typ.	2,25	mA
output LOW	I_{Pav}	typ.	3,6	mA
range II; output HIGH	I_{Pav}	typ.	2,6	mA
output LOW	I_{Pav}	typ.	4,6	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	64,1	mW
at range II; V_{Pmax}	P_{tot}	max.	104,1	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	11,4	$V_{QL} \leq 1,7$ V; $I_{QL} = 15$ mA
Input LOW	V_{GL}	–	–	4,5	V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH} = 0,1$ mA
Output HIGH	V_{QH}	10,0	11,3	–	V	11,4 and 13,5	$V_{GL} = 4,5$ V; $-I_{QH} = 0,1$ mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	$V_{GH} = 7,5$ V; $I_{QL} = 15$ mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	μA	13,5	$V_{GH} = 13,5$ V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5	mA	13,5	$V_{GL} = 1,7$ V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4 and 13,5	$V_{GL} = 4,5$ V; $V_{QH} = 10$ V
Output LOW	I_{QL}	15	–	–	mA	11,4	$V_{GH} = 7,5$ V; $V_{QL} = 1,7$ V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	13,5	$V_G = 0$ V; $V_Q = 0$ V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	3,6	5,8	mA	13,5	$V_G = 13,5$ V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	90	175	310	ns	12	$C_L = 10$ pF; N = 1; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V
rise time	t_{pdr}	200	340	570	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

[2] Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

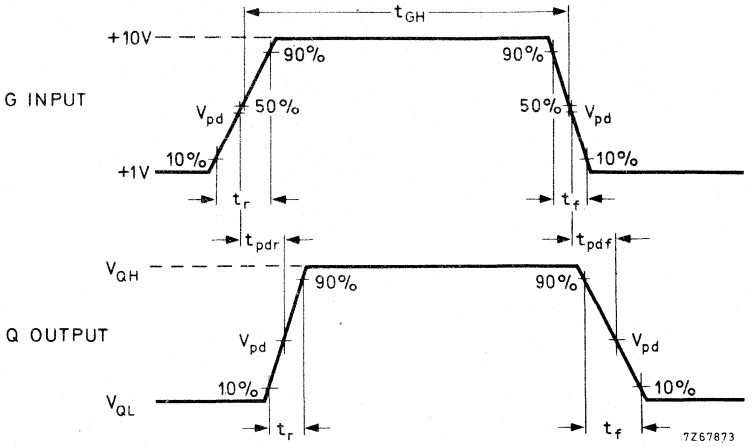
	Sym-bol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; $I_{QL} = 18$ mA
Input LOW	V_{GL}	–	–	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH} = 0,1$ mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5 and 17	$V_{GL} = 4,5$ V; $-I_{QH} = 0,1$ mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	$V_{GH} = 7,5$ V; $I_{QL} = 18$ mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	μA	17	$V_{GH} = 17$ V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8	mA	17	$V_{GL} = 1,7$ V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5 and 17	$V_{GL} = 4,5$ V; $V_{QH} = 12$ V
Output LOW	I_{QL}	18	–	–	mA	13,5	$V_{GH} = 7,5$ V; $V_{QL} = 1,7$ V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	17	$V_G = 0$ V; $V_Q = 0$ V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	4,6	7,3	mA	17	$V_G = 17$ V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	–	t.b.f.	–	ns	15	$C_L = 10$ pF; N = 1; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V
rise time	t_{pdr}	–	t.b.f.	–	ns	15	
output rise time	t_r	–	t.b.f.	–	ns	15	
output fall time	t_f	–	t.b.f.	–	ns	15	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

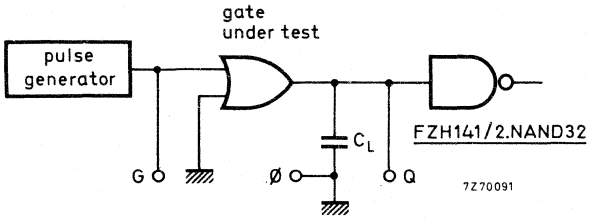
[2] Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = +4,5 V
t_f = 120 ns
t_{GH} = 1 µs



Measuring conditions: V_P = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C

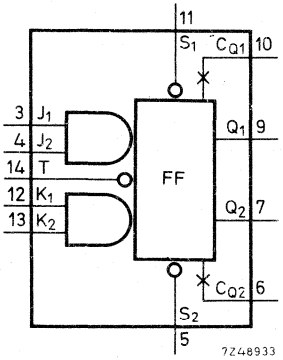
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

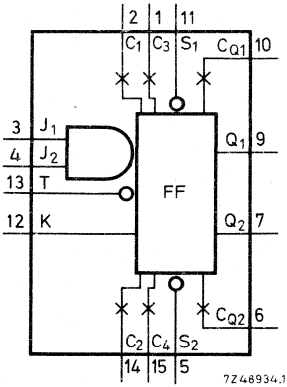
SINGLE JK MASTER-SLAVE FLIP-FLOPS

FZJ101/FF30: with slow-down capability on the slave

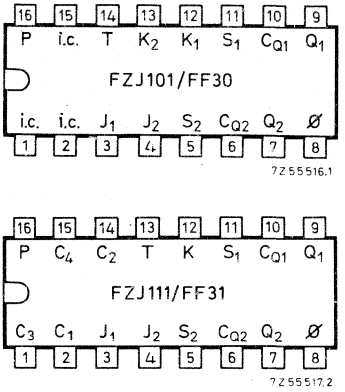
FZJ111/FF31: with slow-down capability on master and slave



FZJ101/FF30



FZJ111/FF31

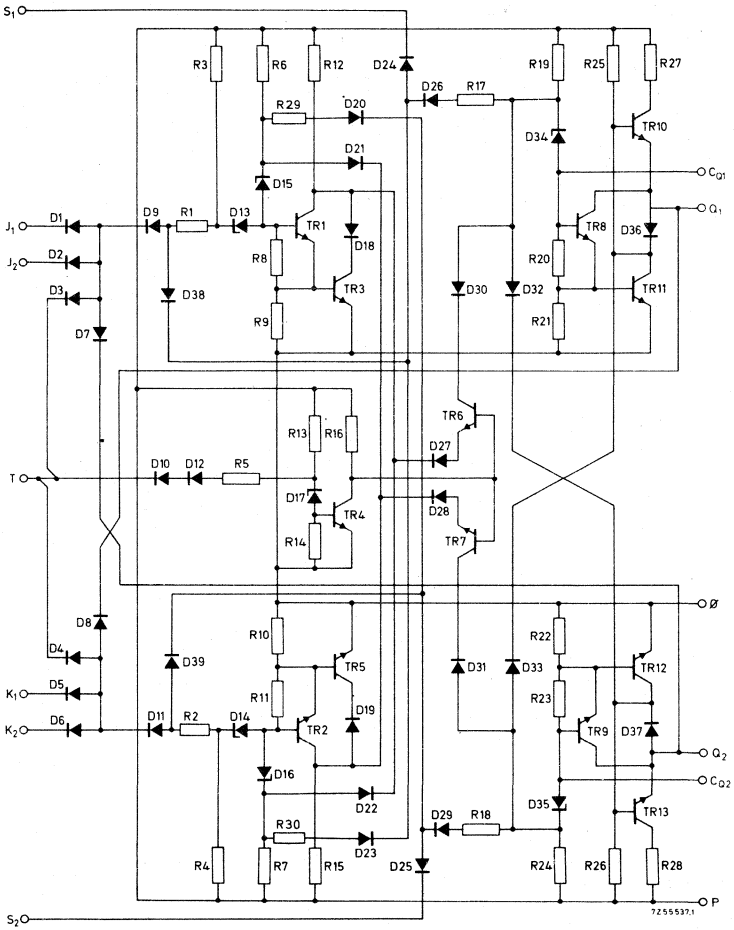


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out (T_{amb} = 0 to +70 °C) } LOW state	N_{aL}	max.	10	
Operating frequency at T_{amb} = 25 °C duty cycle 50%; range I/II	f_c	typ.	0,5	MHz
Average supply current at T_{amb} = 25 °C				
V_P = 13,5 V	I_{Pav}	typ.	8	mA
V_P = 17 V	I_{Pav}	typ.	11	mA
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II : V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V

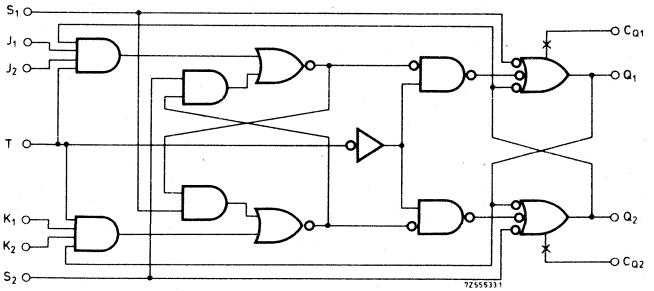
PACKAGE OUTLINE 16-lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM

FZJ101/FF30

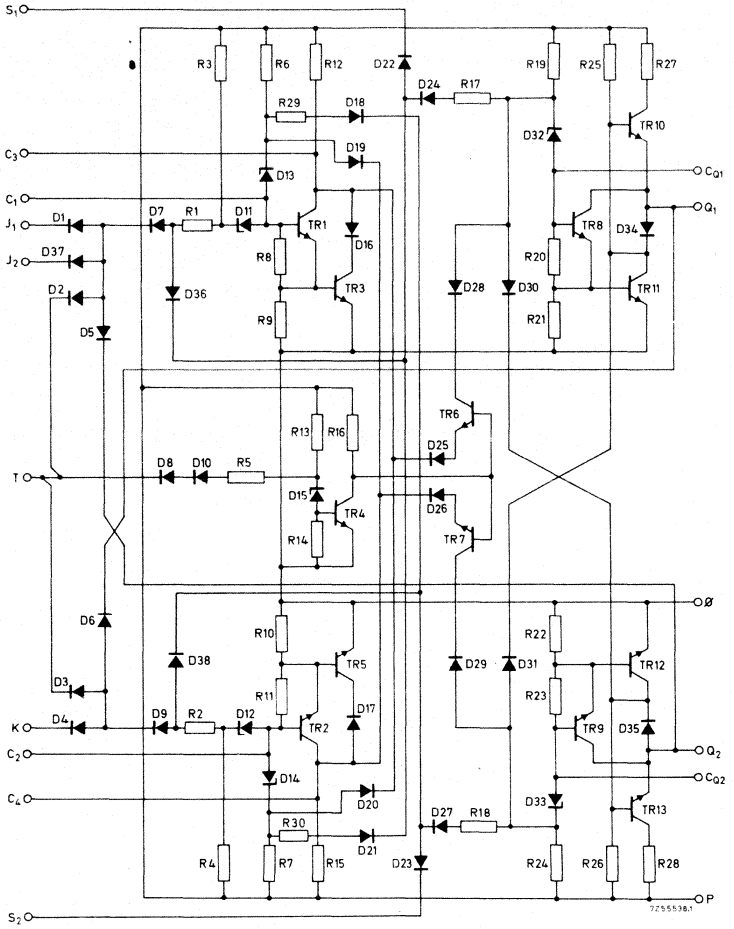


LOGIC DIAGRAM

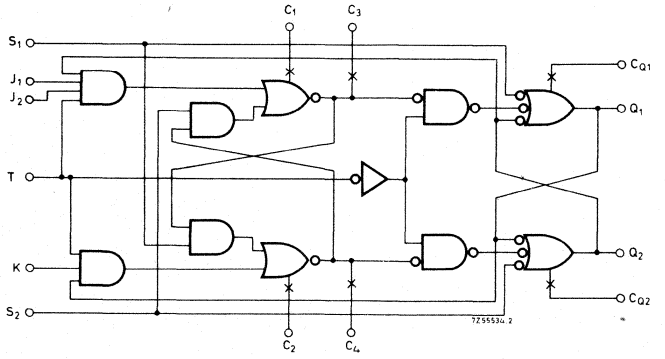


CIRCUIT DIAGRAM

FZJ111/FF31



LOGIC DIAGRAM



GENERAL DESCRIPTION

The FZJ101/FF30 consists of a single JK master-slave flip-flop with two J and K inputs and also has a slow-down capability on the slave of the flip-flop. So the reaction time of the slave to the negative-going clock-edge can be increased. This can be achieved by connecting external capacitors between the output terminals and their associated slow-down terminals.

The FZJ111/FF31 consists of a single JK master-slave flip-flop with two J inputs and one K input and has a slow-down capability both on the master and the slave of the flip-flop. For slowing down the slave see FZJ101/FF30.

The reaction time of the master to the positive-going clock-edge can be increased by connecting external capacitors between the slow-down terminals C_1, C_3 and C_2, C_4 respectively. Furthermore a minimum slope of the T-signal is required.

LOGIC FUNCTIONS

FZJ101/FF30

$J = J_1 \cdot J_2$

$K = K_1 \cdot K_2$

FZJ111/FF31

$J = J_1 \cdot J_2$

$K = K$

Function tables

t_n		t_{n+1}	
J	K	Q_1	Q_2
L	L	Q_{1n}	Q_{2n}
L	H	L	H
H	L	H	L
H	H	Q_{2n}	Q_{1n}
Q_2 is opposite Q_1			

The set inputs S_1 and S_2 override all the other inputs.

S_1	S_2	Q_1	Q_2
L	H	H	L
H	L	L	H
H	H	Q_1	Q_2 1)
L	L	H	H 2)

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

1) Q_2 is opposite Q_1

2) If S_1 and S_2 return to HIGH simultaneously the Q-states will be indeterminate.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	12	V
Input voltage	V_J, V_K, V_T	max.	18	V
Input current at V_P = 17 V	$-I_{IL}$	max.	25	mA 1)
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

1) All inputs except slow-down inputs.

NOTE

The slow-down terminals indicated by crosses are for slow-down purposes only; they are not to be connected to any other terminal.

RATINGS (continued)

Output short-circuit duration	t_{Qsc}	max.	1	s [1] ←
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	V
	$-I_{CQ}$	max.	10,0	V

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C
Uniform system supply voltage (range I)	V_P		11,4 to 13,5	V
(range II)	V_P		13,5 to 17	V
Available d.c. fan-out	N_{aL}	max.	10	
D.C. noise margin to all inputs: range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Average propagation delay time at V_{pd} = 4,5 V				
T → Q: at range I ; V_P = 12 V	t_{pd}	max.	645	ns
at range II; V_P = 15 V	t_{pd}	typ.	400	ns
S → Q: at range I ; V_P = 12 V	t_{pd}	max.	455	ns
at range II; V_P = 15 V	t_{pd}	typ.	265	ns
Maximum clock rate at T_{amb} = 25 °C duty cycle 50%; range I/II	f_c	typ.	0,5	MHz
		min.	0,2	MHz ←
Supply current at range I : V_P = 12 V	I_P	typ.	8	mA
range II : V_P = 15 V	I_P	typ.	11	mA
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

[1]) Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.	Conditions and references	
					V_P (V)	
Static data						
Voltages						
Input HIGH: J, K, T, S	V_{IH}	7,5	–	– V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW: J, K, S	V_{IL}	–	–	4,5 V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$=0,1mA
T	V_{TL}	–	–	4,0 V		
Output HIGH	V_{QH}	10	11,3	– V	11,4 and 13,5	V_{IL} = 4,5 V; $-I_{QH}$=0,1mA
Output LOW	V_{QL}	–	0,9	1,7 V	11,4	V_{IH} = 7,5 V; I_{QL} =15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	– V	11,4	
LOW	M_L	2,8	5,0	– V	11,4	
Currents						
Input HIGH: J, K, S	I_{IH}	–	–	1 µA	13,5	V_{IH} = 13,5 V (other inputs 0V)
T	I_{TH}	–	–	3 µA		
Input LOW: J, K	$-I_{IL}$	–	0,8	1,5 mA	13,5	$V_{JL}=V_{KL}=1,7$V
T	$-I_{TL}$	–	1,6	3,0 mA	13,5	V_{TL} = 1,7 V
S[2]	$-I_{SL}$	–	0,8	1,5 mA	13,5	V_{SL} = 1,7 V
Output HIGH	$-I_{QH}$	0,1	–	– mA	11,4 and 13,5	V_{QH} = 10 V
Output LOW	I_{QL}	15	–	– mA	11,4	V_{QL} = 1,7 V
Output short-circuited[3]	$-I_{Qsc}$	10	30	50 mA	13,5	V_I=0V; V_Q=0V
Supply data						
Supply current	I_P	–	8,0	– mA	13,5	

1) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
2) For dynamic: $-I_{SL}$ = 1,5 x specified values.
3) Short-circuited duration max. 1 s.

CHARACTERISTICS (continued)

Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references
Dynamic data						
Times						
Propagation delay:						
T → Q						
fall time	t_{pdf}	270	450	770	ns	
rise time	t_{pdr}	160	290	520	ns	
S → Q						
fall time	t_{pdf}	180	330	580	ns	
rise time	t_{pdr}	70	165	330	ns	
output rise time	t_r	200	340	570	ns	
output fall time	t_f	70	120	210	ns	C_L = 10 pF
Clock rate						N = 1
(duty cycle 50%)	f_c	0,2	0,5	–	MHz	T_{amb} = 25 °C
Input times						V_{pd} = 4,5 V
T input	t_{TH}	0,6	–	–	µs	
	t_{TL}	0,6	–	–	µs	
S input	t_{SL}	1,0	–	–	µs	
J or K input						
hold time	t_{hold}	0	–	–	ns	
set-up time	t_{su}	0	–	–	ns	
T input slope	$(-dV/dt)_{Tmin}$			1	V/µs	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH: J, K, T, S	V_{IH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW: J, K, S	V_{IL}	–	–	4,5	V	13,5 and 17	$V_{QH} \leq 12$ V; $-I_{QH}$ = 0,1 mA
T	V_{TL}	–	–	4,0	V	13,5 and 17	$V_{QH} \leq 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12	14,3	–	V	13,5 and 17	V_{IL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{IH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents							
Input HIGH: J, K, S	I_{IH}	–	–	1,0	μA	17	V_{IH} = 17 V; (other inputs 0 V)
T	I_{TH}	–	–	3,0	μA	17	V_{IH} = 17 V; (other inputs 0 V)
Input LOW: J, K	$-I_{IL}$	–	1,0	1,8	mA	17	$V_{JL} = V_{KL} = 1,7$ V
T	$-I_{TL}$	–	2,0	3,6	mA	17	V_{TL} = 1,7 V
S [2]	$-I_{SL}$	–	1,0	1,8	mA	17	V_{SL} = 1,7 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5 and 17	V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{QL} = 1,7 V
Output short-circuited	$-I_{Qsc}$ [3]	15	37	60	mA	17	V_I = 0 V; V_Q = 0 V
Supply data							
Supply current	I_P	–	11	–	mA	17	

[1] All typ. values under test conditions: T_{amb} = 25 °C and V_P = 15 V.
[2] For dynamic: $-I_{SL}$ = 1,5 x specified values.
[3] Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

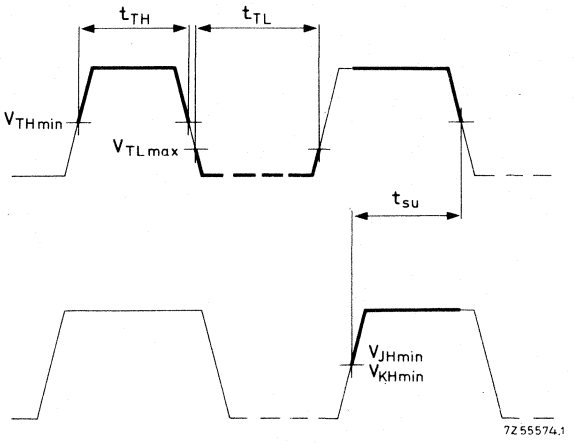
Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references
Dynamic data						
Times						
Propagation delay:						
T ⟶ Q						
fall time	t_{pdf}	–	470	–	ns	
rise time	t_{pdr}	–	330	–	ns	
S ⟶ Q						
fall time	t_{pdf}	–	340	–	ns	
rise time	t_{pdr}	–	195	–	ns	
output rise time	t_r	–	410	–	ns	
output fall time	t_f	–	75	–	ns	C_L = 10 pF
Clock rate						N = 1
(duty cycle 50%)	f_c	–	0,5	–	MHz	T_{amb} = 25 °C
Input times						V_{pd} = 4,5 V
T input	t_{TH}	0,6	–	–	µs	
	t_{TL}	0,6	–	–	µs	
S input	t_{SL}	1,0	–	–	µs	
J or K input						
hold time	t_{hold}	0	–	–	µs	
set-up time	t_{su}	0	–	–	µs	
T input slope	$(-dV/dt)_{Tmin}$			1	V/µs	

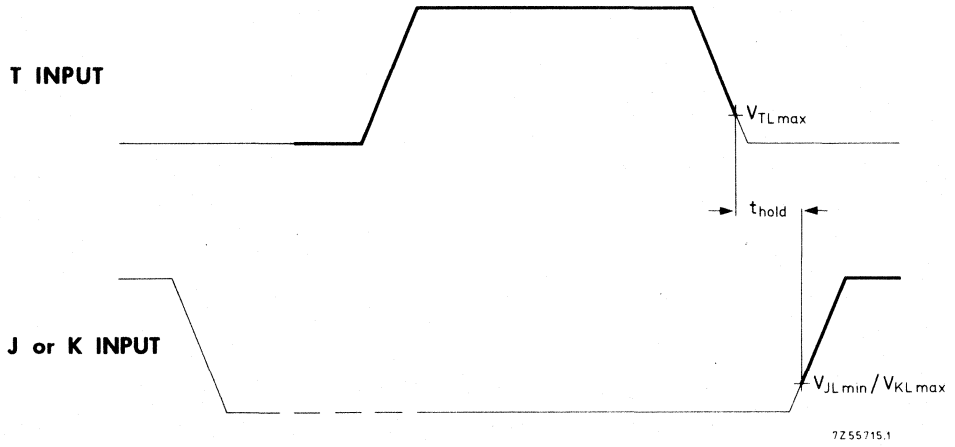
[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

CHARACTERISTICS (continued)

Dynamic data



Waveforms illustrating conditions for change of state



Waveforms illustrating conditions for no change of state

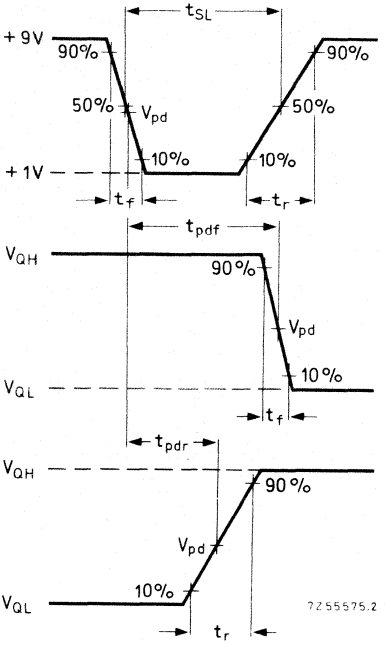
CHARACTERISTICS (continued)

Dynamic data

$S_2(S_1)$ INPUT

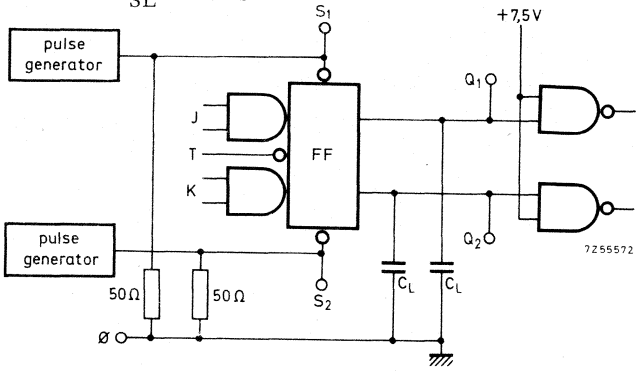
$Q_1(Q_2)$ OUTPUT

$Q_2(Q_1)$ OUTPUT



Pulse generator (S-input): t_r = 350 ns
t_f = 120 ns
t_{SL} = 700 ns

$V_{pd} = +4,5$ V

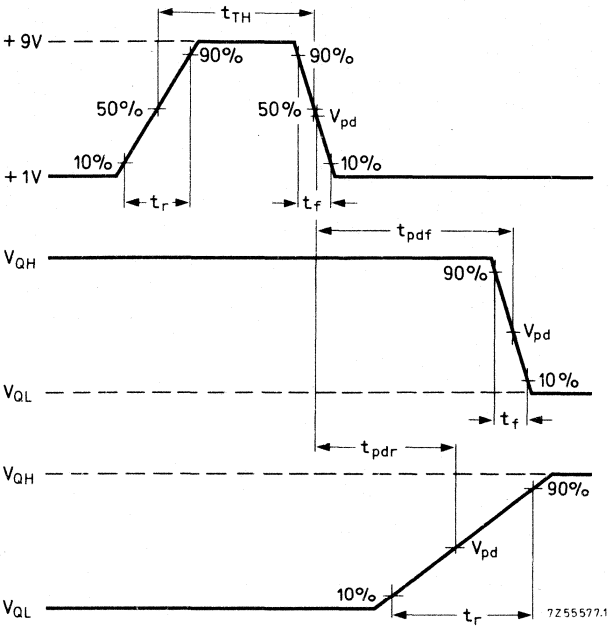


Measuring conditions: V_p = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
Slow-down terminals are not connected
All other inputs are floating.

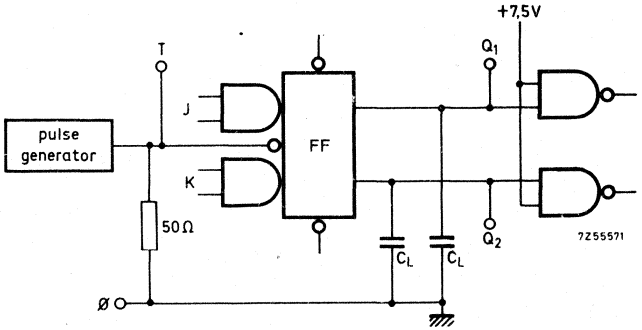
Waveforms illustrating conditions for set inputs. Set input signals are not supplied simultaneously.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (T-input): t_r = 350 ns V_{pd} = +4, 5 V
t_f = 120 ns
t_{TH} = 400 ns

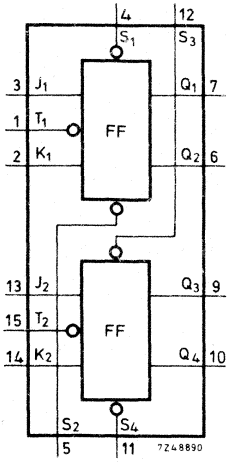


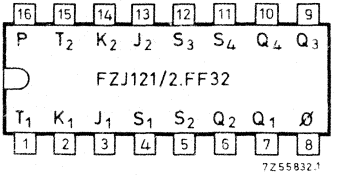
Measuring conditions: V_P = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
Slow-down terminals are not connected
All other inputs are floating.

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}.

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL JK MASTER-SLAVE FLIP-FLOP





QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out T_{amb} = 0 to +70 °C — LOW state	N_{aL}	max.	10	
Operating frequency at T_{amb} = 25 °C duty cycle 50%: range I/II	f_c	typ.	0,5	MHz
Average supply current at T_{amb} = 25 °C				
V_P = 13,5 V	I_{Pav}	typ.	15	mA
V_P = 17 V	I_{Pav}	typ.	20	mA
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II : V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V

PACKAGE OUTLINE 16-lead plastic dual in-line (see general section).

GENERAL DESCRIPTION

The FZJ121/2.FF32 comprises two independent JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, e.g. rise and fall times of all input signals including the trigger signals are immaterial.
The set and reset inputs (overriding any other input) are active at LOW level. There are no slow-down terminals.
Typical applications include counters and shift registers.

FUNCTION TABLES

t_n		t_{n+1}
J_1 J_2	K_1 K_2	Q_1 Q_3
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q_n}$
Q_2 is opposite Q_1 Q_4 is opposite Q_3		

S_1 S_3	S_2 S_4	Q_1 Q_3	Q_2 Q_4
L	H	H	L
H	L	L	H
H	H	$Q_1(Q_3)$	$Q_2(Q_4)$ 1)
L	L	X	X 2)

1) $Q_2(Q_4)$ is opposite $Q_1(Q_3)$
2) If S_1 (S_3) and S_2 (S_4) return to HIGH simultaneously the Q-states will be indeterminate.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_J, V_K, V_T	max.	18	V
Input current at V_P = 17 V	$-I_{IL}$	max.	25	mA
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s 1)

1) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0	to	+70	°C
Uniform system supply voltage (range I)	V_P	11,4	to	13,5	V
(range II)	V_P	13,5	to	17	V
Available d.c. fan-out	N_{aL}	max.		10	
D.C. noise margin to all inputs: range I at V_{Pmin}	M_L	min.		2,8	V
	M_H	min.		2,5	V
range II at V_{Pmin}	M_L	min.		2,8	V
	M_H	min.		4,5	V
Supply current at range I : V_P = 12 V	I_P	typ.		15	mA
range II : V_P = 15 V	I_P	typ.		20	mA
Thermal resistance from system to ambient	R_{th}	max.		150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH: T	V_{TH}	6,5	-	-	V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
J; K	V_{IH}	8,0	-	-	V	11,4	
S	V_{SH}	7,5	-	-	V	11,4	
Input LOW: T	V_{TL}	-	-	4,0	V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
J; K	V_{IL}	-	-	5,5	V		
S	V_{SL}	-	-	4,5	V		
Output HIGH	V_{QH}	10,0	11,3	-	V	11,4 and 13,5	$V_{IL} \leq 4,5$ V [2]; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	-	0,9	1,7	V	11,4	$V_{IH} \geq 7,5$ V [2]; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	-	V	11,4	
LOW	M_L	2,8	5,0	-	V	11,4	
Currents							
Input HIGH: T	I_{TH}	-	-	3	µA	13,5	V_{IH} = 13,5 V (other inputs 0V)
J; K; S	I_{IH}	-	-	1	µA		
Input LOW: T	$-I_{TL}$	-	1,6	3,0	mA	13,5	V_{IL} = 1,7 V
J; K; S [3]	$-I_{IL}$	-	0,8	1,5	mA	13,5	V_{IL} = 1,7 V
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4 and 13,5	V_{QH} = 10 V
Output LOW	I_{QL}	15	-	-	mA	11,4	V_{QL} = 1,7 V
Supply data							
Supply current	I_P	-	15	24	mA	13,5	

1) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
2) Measured to S_2 and S_1.
3) For dynamic: $-I_{SL}$ = 1,5 x specified values.

CHARACTERISTICS (continued)

Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references
Dynamic data						
Times						
Propagation delay:						
T ⟶ Q						
fall time	t_{pdf}	270	450	770	ns	
rise time	t_{pdr}	160	290	520	ns	
R or S ⟶ Q						
fall time	t_{pdf}	180	330	580	ns	
rise time	t_{pdr}	70	165	330	ns	
output fall time	t_f	70	120	210	ns	
output rise time	t_r	200	340	570	ns	C_L = 10 pF
Clock rate						N = 1
(duty cycle 50%)	f_c	0,2	0,5	–	MHz	T_{amb} = 25 °C
Input times						V_{pd} = 4,5 V
T input	t_{TH}	0,6	–	–	µs	
R input	t_{RL}	1,0	–	–	µs	
S input	t_{SL}	1,0	–	–	µs	
J or K input						
hold time	t_{hold}	0	–	–	ns	
set-up time	t_{su}	0	–	–	ns	
T input slope	$(-dV/dt)_{Tmin}$			1	V/µs	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ.[1]	max.		Conditions and references: V_P (V)	
Static data							
Voltages							
Input HIGH: T	V_{TH}	6,5	-	-	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
J; K	V_{IH}	8,0	-	-	V	13,5	
S	V_{SH}	7,5	-	-	V	13,5	
Input LOW: T	V_{TL}	-	-	4,0	V	11,4 and 13,5	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
J; K	V_{IL}	-	-	5,5	V		
S	V_{SL}	-	-	4,5	V		
Output HIGH	V_{QH}	12,0	14,3	-	V	11,4 and 13,5	$V_{IL} \leq 4,5$ V[2]; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	-	1,1	1,7	V	13,5	$V_{IH} \geq 7,5$ V[2]; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	-	V	13,5	
LOW	M_L	2,8	5,0	-	V	13,5	
Currents							
Input HIGH: T	I_{TH}	-	-	3,0	µA	17	V_{IH} = 17 V (other inputs 0V)
J; K; S	I_{IH}	-	-	1,0	µA		
Input LOW: T	$-I_{TL}$	-	2,0	3,6	mA	17	V_{IL} = 1,7 V
J; K; S[3]	$-I_{IL}$	-	1,0	1,8	mA	17	
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5 and 17	V_{QH} = 12 V
Output LOW	I_{QL}	18	-	-	mA	13,5	V_{QL} = 1,7 V
Supply data							
Supply current	I_P	-	20	32	mA	17	

1) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.
2) Measured to S_2 and S_1.
3) For dynamic: $-I_{SL}$ = 1,5 x specified values.

CHARACTERISTICS (continued)

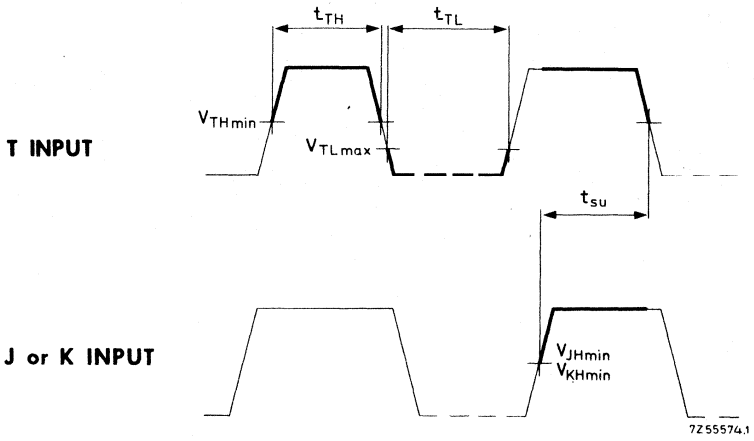
Test conditions at range II (V_p = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references
Dynamic data						
Times						
Propagation delay:						
T ⟶ Q						
fall time	t_{pdf}	–	470	–	ns	
rise time	t_{pdr}	–	330	–	ns	
R or S ⟶ Q						
fall time	t_{pdf}	–	340	–	ns	
rise time	t_{pdr}	–	195	–	ns	
output fall time	t_f	–	75	–	ns	
output rise time	t_r	–	410	–	ns	C_L = 10 pF
Clock rate						N = 1
(duty cycle 50%)	f_c	0,2	0,5	–	MHz	T_{amb} = 25 °C
Input times						V_{pd} = 4,5 V
T input	t_{TH}	0,6	–	–	µs	
R input	t_{RL}	0,6	–	–	µs	
S input	t_{SL}	1,0	–	–	µs	
J or K input						
hold time	t_{hold}	0	–	–	ns	
set-up time	t_{su}	0	–	–	ns	
T input slope	$(-dV/dt)_{Tmin}$			1	V/µs	

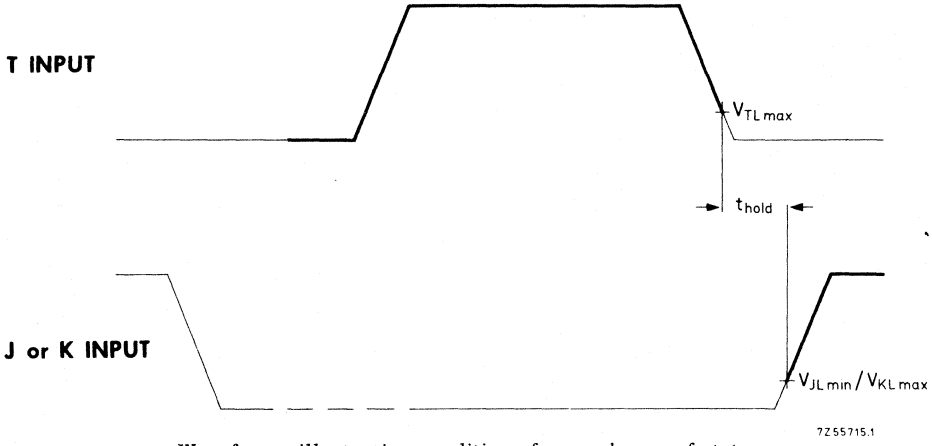
[1]) All typical values under test conditions: T_{amb} = 25 °C and V_p = 15 V.

CHARACTERISTICS (continued)

Dynamic data



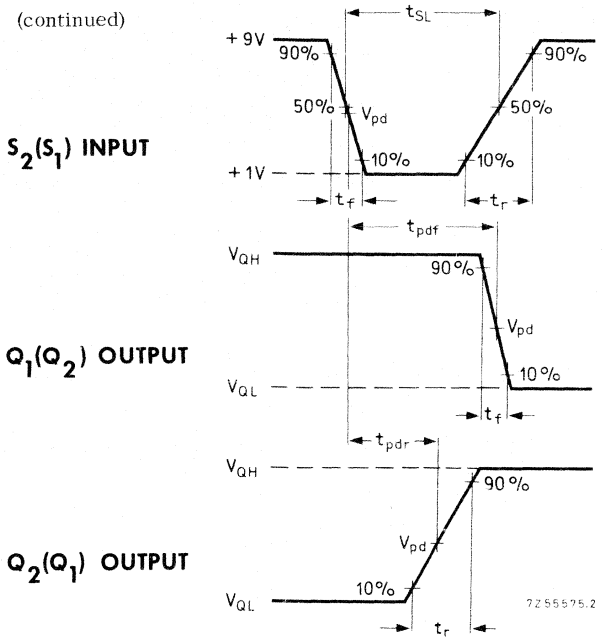
Waveforms illustrating conditions for change of state



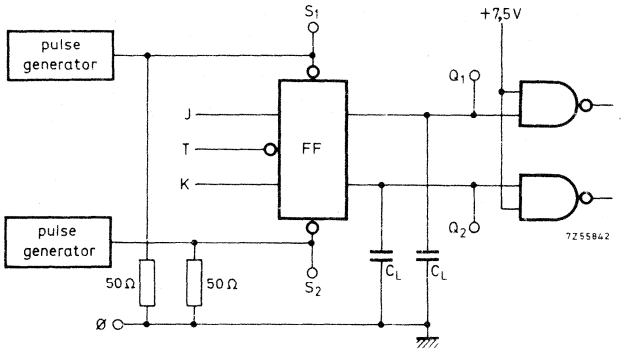
Waveforms illustrating conditions for no change of state

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (S-input): t_r = 350 ns; t_f = 120 ns; t_{SL} = 700 ns; V_{pd} = +4,5 V

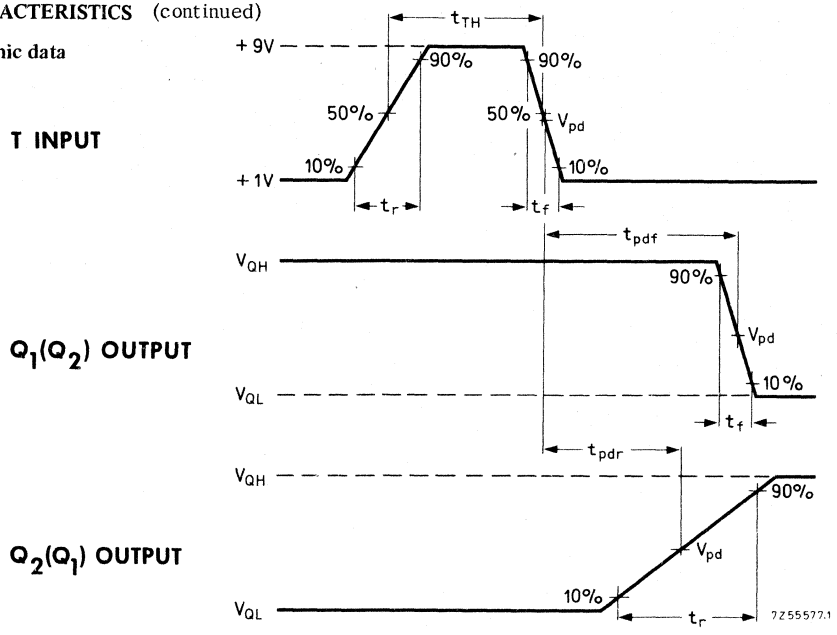


Measuring conditions: V_P = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
All other inputs are floating.

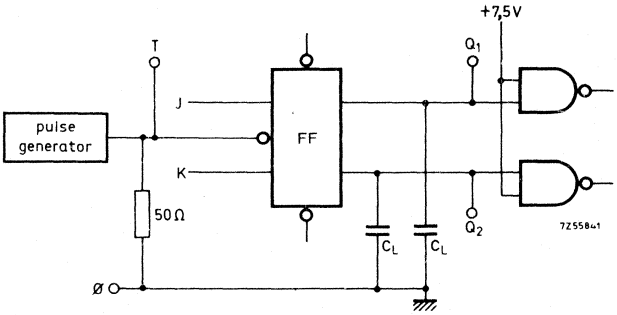
Waveforms illustrating conditions for set inputs. Set input signals are not supplied simultaneously.

CHARACTERISTICS (continued)

Dynamic data



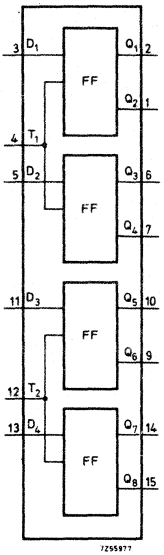
Pulse generator (T-input): t_r = 350 ns; t_f = 120 ns; t_{TH} = 400 ns; V_{pd} = +4,5 V



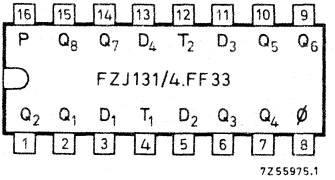
Measuring conditions: V_P = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
All other inputs are floating.

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}.

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.



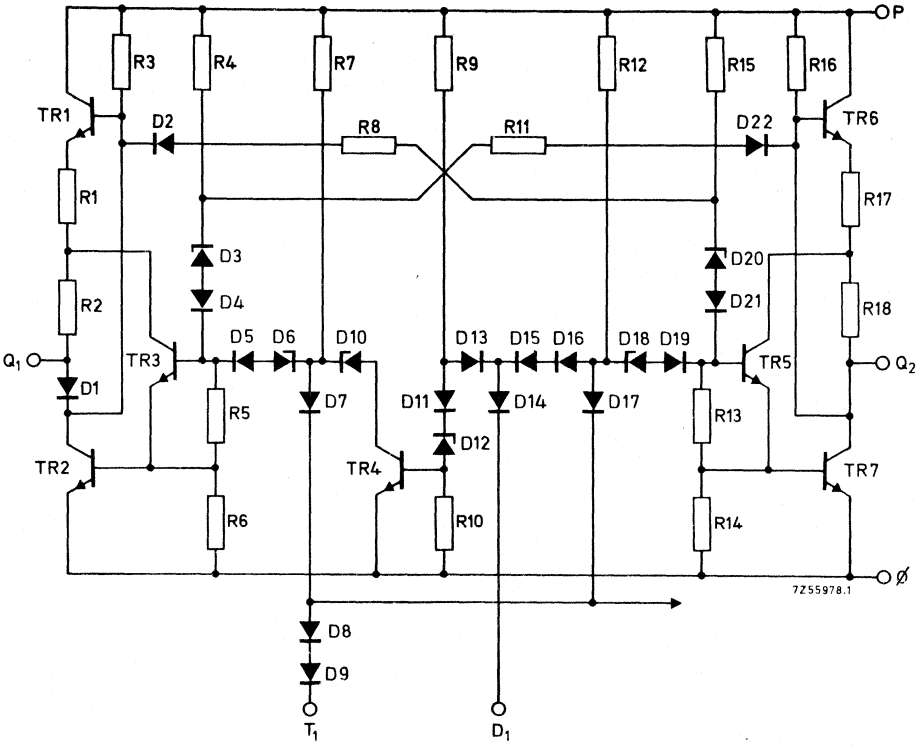
QUADRUPLE D-TYPE LATCH FLIP-FLOP



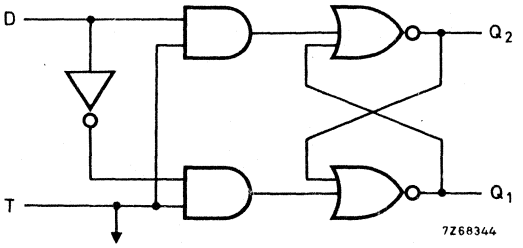
QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out T_{amb} = 0 to +70 °C — LOW state	N_{aL}	max.	10	
Average supply current at T_{amb} = 25 °C				
V_P = 13,5 V	I_{Pav}	typ.	22	mA
V_P = 17 V	I_{Pav}	typ.	28	mA
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II : V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V
Average power consumption				
(50% duty cycle) range I : V_P = 12 V	P_{av}	typ.	264	mW
range II : V_P = 15 V	P_{av}	typ.	420	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC DIAGRAM



LOGIC FUNCTIONS

The FZJ131/4.FF33 comprises four D-type latch flip-flops. Information present at a data input D, is transferred to Q as long as T is HIGH.
When T is LOW, D does not affect Q.

Function table

input		output
T	D (t_n)	Q ($t_n + 1$)
L	L	Q_n
L	H	Q_n
H	L	L
H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

t_n = bit-time before trigger pulse
t_{n+1} = bit-time after trigger pulse

RATING Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_D, V_T	max.	18	V
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C
Uniform system supply voltage (range I)	V_P		11,4 to 13,5	V
(range II)	V_P		13,5 to 17	V
Available d.c. fan-out	N_{aL}	max.	10	
D.C. noise margin to all inputs: range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Power consumption (50% duty cycle) at range I : V_{Pmax}	P_{av}	max.	432	mW
at range II : V_{Pmax}	P_{av}	max.	720	mW
Supply surrent at range I : V_P = 12 V	I_P	max.	32	mA
range II : V_P = 15 V	I_P	max.	42	mA
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

1) Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ.[1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH: D, T	V_{IH}	7,5	–	–	V		
Input LOW: D, T	V_{IL}	–	–	4,5	V		
Output HIGH	V_{QH}	10	11,3	–	V	11,4	V_I = 7,5 V $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	V_{TH} = 7,5 V V_{DL} = 4,5 V I_{QL} = 15 mA
D.C. noise margin							
HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents							
Input HIGH: D, T	I_{IH}	–	–	1	µA	13,5	V_{IH} = 13,5 V other inputs 0 V
Input LOW: D	$-I_{DL}$	–	–	3	mA	13,5	V_{DL} = 1,7 V
T	$-I_{TL}$	–	–	6	mA	13,5	V_{TL} = 1,7 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4	V_{QH} = 10 V
Output LOW	I_{QL}	15	–	–	mA	11,4	V_{QL} = 1,7 V
Output short-circuited	$-I_{Qsc}$	9	15	25	mA	13,5	V_I = 0; V_Q = 0
Supply data							
Supply current	I_P	–	22	32	mA	13,5	V_I = 0

1) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		conditions and references
Dynamic data						
Times						
Propagation delay:						
$T_1 \longrightarrow Q_1$						
fall time	t_{pdf}	70	120	210	ns	
rise time	t_{pdr}	90	160	310	ns	
$T_1 \longrightarrow Q_2$						
fall time	t_{pdf}	70	120	210	ns	
rise time	t_{pdr}	90	150	310	ns	
$D_1 \longrightarrow Q_1$						
fall time	t_{pdf}	30	70	150	ns	
rise time	t_{pdr}	90	175	310	ns	
$D_1 \longrightarrow Q_2$						
fall time	t_{pdf}	70	130	290	ns	
rise time	t_{pdr}	30	70	150	ns	C_L = 10 pF N = 1
output fall time	t_f	15	35	60	ns	T_{amb} = 25 °C
output rise time	t_r	50	90	170	ns	V_{pd} = 4,5 V
Clock rate						
(duty cycle 50%)	f_c	0,5	-	-	MHz	
D input						
hold time	t_{holdH}	150	-	-	ns	
	t_{holdL}	50	-	-	ns	
set-up time	t_{suH}	300	-	-	ns	
	t_{suL}	500	-	-	ns	
T input	$(-dV/dt)_{Tmin}$			1	V/µs	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH: D, T	V_{IH}	7,5	–	–	V		
Input LOW: D, T	V_{IL}	–	–	4,5	V		
Output HIGH	V_{QH}	12	14,3	–	V	13,5	V_I = 7,5 V $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{TH} = 7,5 V V_{DL} = 4,5 V I_{QL} = 18 mA
D.C. noise margin							
HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents							
Input HIGH: D, T	I_{IH}	–	–	1,0	µA	17	V_{IH} = 17 V (other inputs 0 V)
Input LOW: D	$-I_{DL}$	–	–	3,6	mA	17	V_{DL} = 1,7 V
T	$-I_{TL}$	–	–	7,2	mA	17	V_{TL} = 1,7 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5	V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{QL} = 1,7 V
Output short-circuited	$-I_{Qsc}$	9	15	25	mA	17	V_I = 0; V_Q = 0
Supply data							
Supply current	I_P	-	28	42	mA	17	V_I = 0

1) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

CHARACTERISTICS (continued)

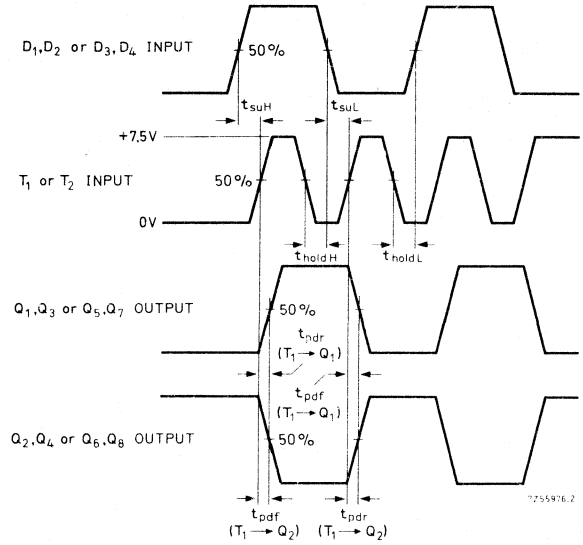
Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

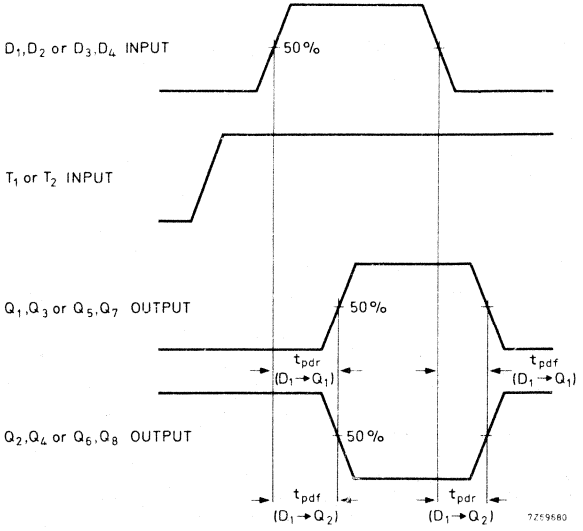
	Symbol	min.	typ. [1]	max	conditions and references
Dynamic data					
Times					
Propagation delay:					
$T_1 \rightarrow Q_1$					
fall time	t_{pdf}				
rise time	t_{pdr}				
$T_1 \rightarrow Q_2$					
fall time	t_{pdf}				
rise time	t_{pdr}				
$D_1 \rightarrow Q_1$					
fall time	t_{pdf}				
rise time	t_{pdr}				
$D_1 \rightarrow Q_2$					
fall time	t_{pdf}				C_L = 10 pF N = 1 T_{amb} = 25 °C V_{pd} = 4,5 V
rise time	t_{pdr}		t.b.f.		
output fall time	t_f				
output rise time	t_r				
Clock rate (duty cycle 50%)	f_c				
D input hold time					
set-up time					
T input slope	$(-dV/dt)_{Tmin}$	–	–	1 V/µs	

[1]) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

CHARACTERISTICS (continued)

Dynamic data

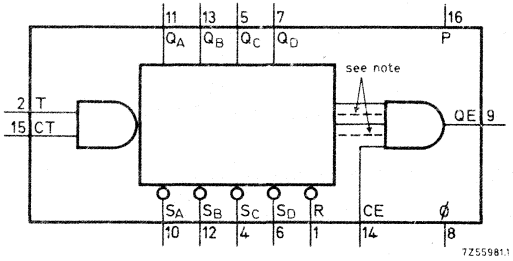


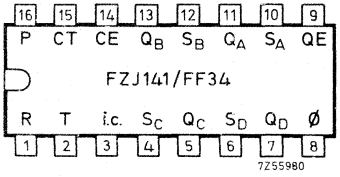


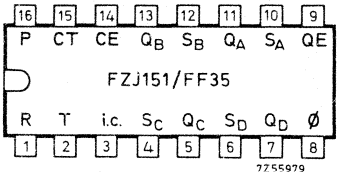
Waveforms illustrating measurement of t_{pdr} and t_{pdf} (T → Q); (D → Q)

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

SINGLE SYNCHRONOUS DECIMAL COUNTER
SINGLE SYNCHRONOUS 4-BIT BINARY COUNTER







Note

FZJ141/FF34: without connections indicated by dotted line
FZJ151/FF35: with connections indicated by dotted line

QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out T_{amb} = 0 to +70 °C } LOW state	N_{aL}	max.	10	
Operating frequency at T_{amb} = 25 °C duty cycle 50%: range I/II	f_c	max.	1,5	MHz
Average supply current at T_{amb} = 25 °C				
V_P = 13,5 V at V_{QL}	I_{Pav}	typ.	20	mA
V_P = 17 V at V_{QL}	I_{Pav}	typ.	23	mA
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II : V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

GENERAL DESCRIPTION

The FZJ141/FF34 and FZJ151/FF35 are synchronous counters consisting of 4 master-slave flip-flops.
The FZJ141/FF34 is a decimal counter with common T and R input and a set (S) input for each bit. The condition input (CE) and output (QE) are for coupling these circuits.
The FZJ151/FF35 is a 4-bit binary counter with a common T and R input and a set input per bit. The direct reset inhibits the count and simultaneously all flip-flops return to LOW. The output information of each flip-flop of both circuits changes when T goes from HIGH to LOW.

LOGIC FUNCTIONS

Count condition: $S_A = S_B = S_C = S_D = CT = CE = R = HIGH$

FZJ141/FF34

count	outputs				
	Q_A	Q_B	Q_C	Q_D	QE
0	L	L	L	L	L
1	H	L	L	L	L
2	L	H	L	L	L
3	H	H	L	L	L
4	L	L	H	L	L
5	H	L	H	L	L
6	L	H	H	L	L
7	H	H	H	L	L
8	L	L	L	H	L
9	H	L	L	H	H

FZJ151/FF35

count	outputs				
	Q_A	Q_B	Q_C	Q_D	QE
0	L	L	L	L	L
1	H	L	L	L	L
2	L	H	L	L	L
3	H	H	L	L	L
4	L	L	H	L	L
5	H	L	H	L	L
6	L	H	H	L	L
7	H	H	H	L	L
8	L	L	L	H	L
9	H	L	L	H	L
10	L	H	L	H	L
11	H	H	L	H	L
12	L	L	H	H	L
13	H	L	H	H	L
14	L	H	H	H	L
15	H	H	H	H	H

Pin description

CT = condition enable trigger at input T
CE = condition enable for output QE
QE = output enable

Set and reset conditions

inputs					outputs			
R	S_A	S_B	S_C	S_D	Q_A	Q_B	Q_C	Q_D
L	H	H	H	H	L	L	L	L
L	L	X	X	X	H	X	X	X
L	X	L	X	X	X	H	X	X
L	X	X	L	X	X	X	H	X
L	X	X	X	L	X	X	X	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

All set and reset inputs, when LOW, override the count input signal and set the flip-flops corresponding to the table at the left.
Set and reset terminals may not be left floating but must be connected to the supply voltage V_P.

LOGIC FUNCTIONS (continued)

Enable conditions

input CT	
L	no count
H	count

input CE	enable output QE
L	L
H	X *)

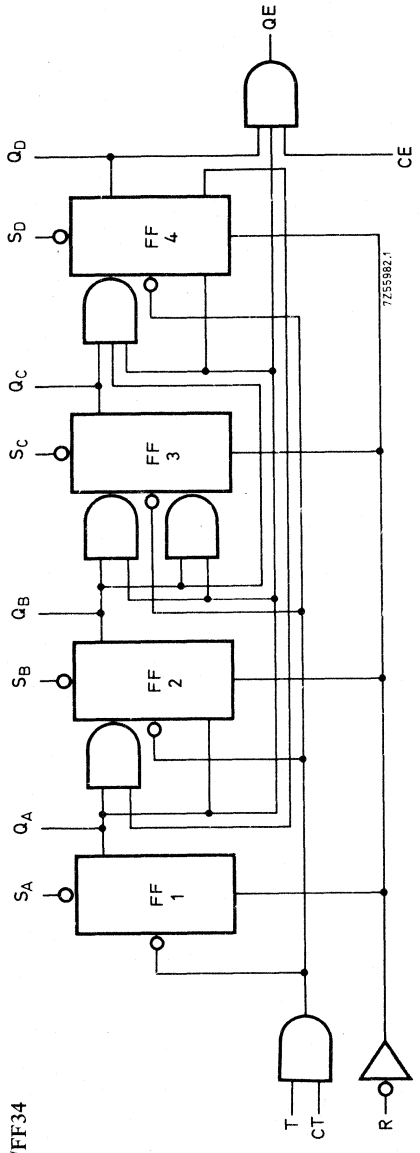
*) Depends on logic state of other inputs of the final gate.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

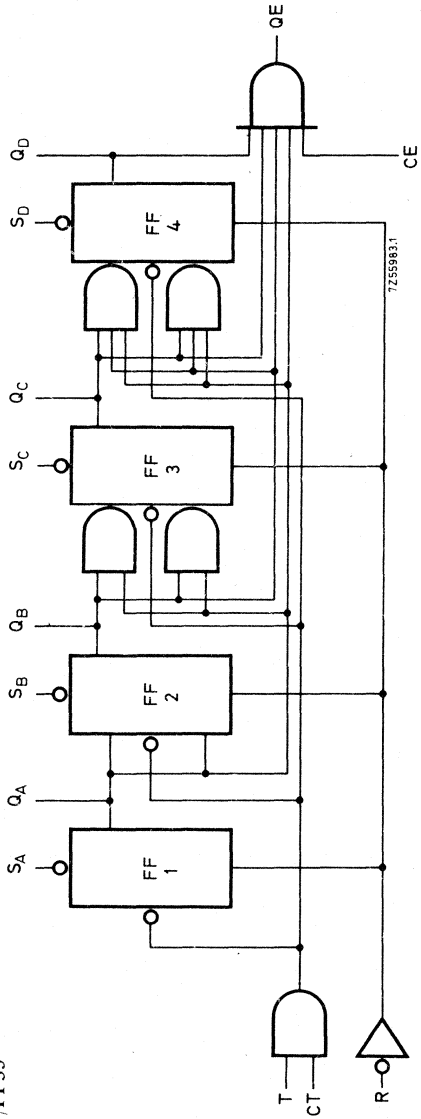
Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_I	max.	18	V
Input current at V_P = 17 V	$-I_{IL}$	max.	25	mA
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

LOGIC DIAGRAMS

FZJ141/FF34



FZJ151/FF35



SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to	+70	°C
Uniform system supply voltage (range I)	V_P	11,4 to	13,5	V
(range II)	V_P	13,5 to	17	V
Available d.c. fan-out	N_{aL}	max.	10	
D.C. noise margin to all inputs: range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Clock rate at T_{amb} = 25 °C duty cycle 50%; range I/II	f_c	min.	0,5	MHz
	f_c	typ.	1,5	MHz
Supply current at range I : V_P = 12 V				
at V_{QH}	I_P	typ.	12	mA
at V_{QL}	I_P	typ.	20	mA
at range II : V_P = 15 V				
at V_{QH}	I_P	typ.	15	mA
at V_{QL}	I_P	typ.	23	mA
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{IH}	7,5	–	–	V	11,4	
Input LOW	V_{IL}	–	–	4,5	V	13,5	
Output HIGH	V_{QH}	10	11,3	–	V	11,4	V_{IL} = 4,5 V $-I_Q$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	V_{IH} = 7,5 V I_Q = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents							
Input HIGH	I_{IH}	–	–	1	µA	13,5	V_{IH} = 13,5 V
Input LOW	$-I_{IL}$	–	0,8	1,5	mA	13,5	V_{IL} = 1,7 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4 and 13,5	V_{QH} = 10 V
Output LOW	I_{QL}	15	–	–	mA	11,4	V_{QL} = 1,7 V
Output short-circuited	$-I_{Qsc}$	9	15	25	mA	13,5	V_I = 0; V_Q = 0
Supply data							
Supply current at V_{QH}	I_P	–	12	–	mA	13,5	V_I = 13,5 V
at V_{QL}	I_P	–	20	–	mA	13,5	V_R = 0 V other inputs 13,5 V

1) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range I (V_P = 12 V)

	Symbol	min.	typ. [1]	max.		Conditions and references
Dynamic data						
Times						
Propagation delay: T → Q_A; Q_B; Q_C; Q_D						
fall time	t_{pdf}	90	200	450	ns	V_{pd} = 4,5 V; N = 1; C_L = 10 pF; T_{amb} = 25 °C
rise time	t_{pdr}	90	200	450	ns	
T → QE						
fall time	t_{pdf}	150	300	500	ns	
rise time	t_{pdr}	200	400	700	ns	
CE → QE						
fall time	t_{pdf}	25	60	200	ns	
rise time	t_{pdr}	90	200	450	ns	
R → Q_A; Q_B; Q_C; Q_D						
fall time	t_{pdf}	70	150	310	ns	
S_A → Q_A; S_B → Q_B; S_C → Q_C; S_D → Q_D						
rise time	t_{pdr}	30	120	210	ns	
Clock pulse duration	t_T	0,5	–	–	µs	V_{pd} = 4,5 V; N = 1
Clock rate	f_c	0,5	–	–	MHz	duty cycle 50%
Reset pulse duration	t_{RL}	0,5	–	–	µs	V_{pd} = 4,5 V; N = 1; T_{amb} = 25 °C
Reset recovery time (T input)	t_{Rrec}	–	–	2	µs	
Reset pulse duration during set operation	t_{RLS}	1	–	–	µs	
Set inputs (S_A; S_B; S_C; S_D) set-up time	t_{su}	1	–	–	µs	
Set inputs (S_A; S_B; S_C; S_D) hold time	t_{hold}	1	–	–	µs	
Output fall time (at Q)	t_f	5	20	60	ns	
Output rise time (at Q)	t_r	90	250	450	ns	
Output fall time (at QE)	t_f	30	60	210	ns	
Output rise time (at QE)	t_r	70	140	310	ns	
T input slope	$(-dV/dt)_{Tmin}$			1	V/µs	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{IH}	7,5	–	–	V	13,5	
Input LOW	V_{IL}	–	–	4,5	V	17,0	
Output HIGH	V_{QH}	12	14,3	–	V	13,5	V_{IL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1	1,7	V	13,5	V_{IH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8	–	V	13,5	
LOW	M_L	2,8	5	–	V	13,5	
Currents							
Input HIGH	I_{IH}	–	–	1	µA	17,0	V_I = 17,0 V
Input LOW	$-I_{IL}$	–	1,0	1,8	mA	17,0	V_I = 1,7 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5	V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{QL} = 1,7 V
Output short-circuited	$-I_{Qsc}$	9	15	25	mA	17,0	V_I = 0; V_Q = 0
Supply data							
Supply current at V_{QH}	I_P	–	15	23	mA	17,0	V_I = 17,0 V
at V_{QL}	I_P	–	23	36,5	mA	17,0	V_R = 0 V; other inputs 17,0 V

1) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

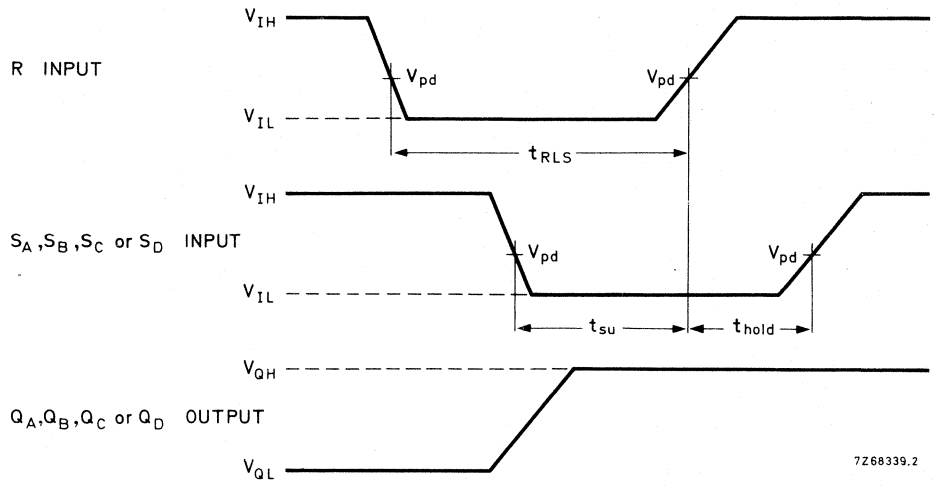
CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min. typ. [1] max.		Conditions and references
Dynamic data				
Times				
Propagation delay:				
T → Q				
fall time	t_{pdf}		ns	
rise time	t_{pdr}		ns	
T → QE				
fall time	t_{pdf}		ns	
rise time	t_{pdr}		ns	
C_E → QE				
fall time	t_{pdf}		ns	
rise time	t_{pdr}		ns	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
R → Q				
fall time	t_{pdf}	t.b.f.	ns	
S_A → Q_A, S_B → Q_B				
rise time	t_{pdr}		ns	
S_C → Q_C, S_D → Q_D				
fall time	t_{pdf}		ns	
output fall time / output rise time } at Q	t_f / t_r		ns	
output fall time / output rise time } at QE				
T input slope	$(-dV/dt)_{Tmin}$	1	V/µs	

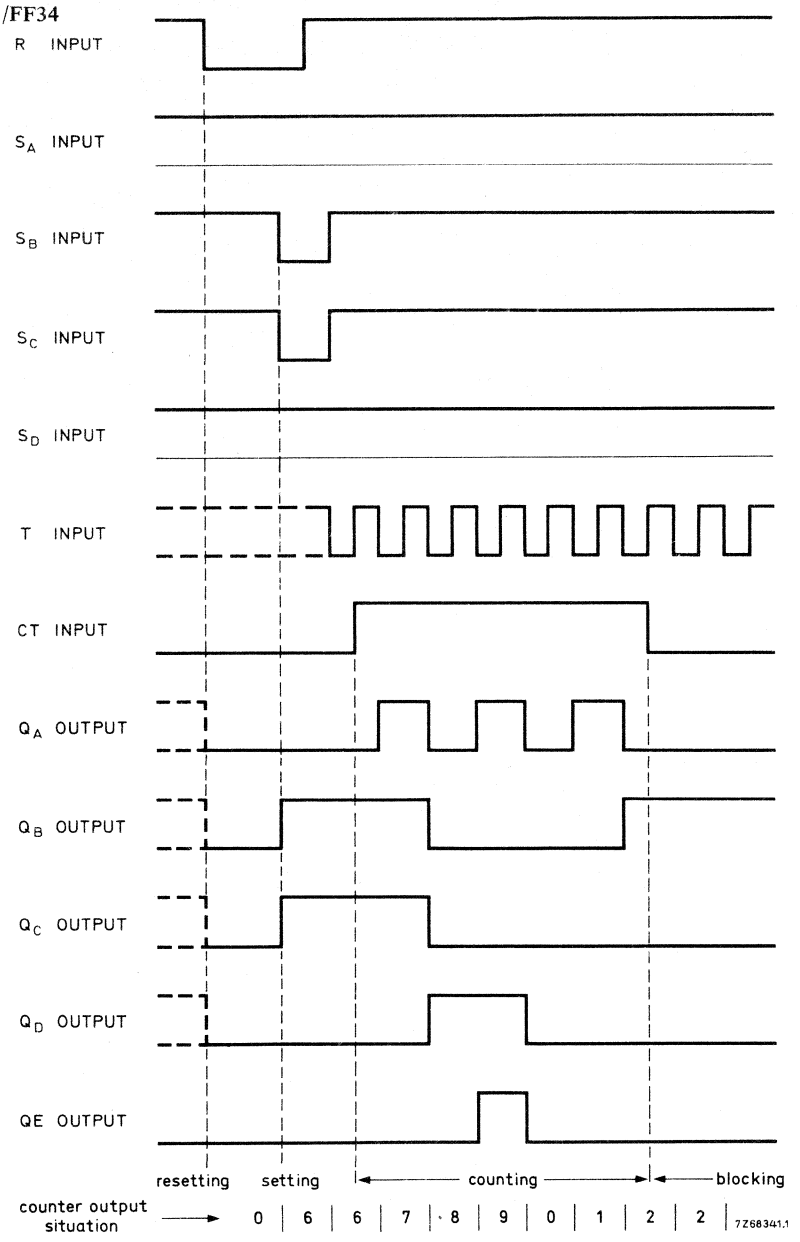
[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

CHARACTERISTIC (*continued*)



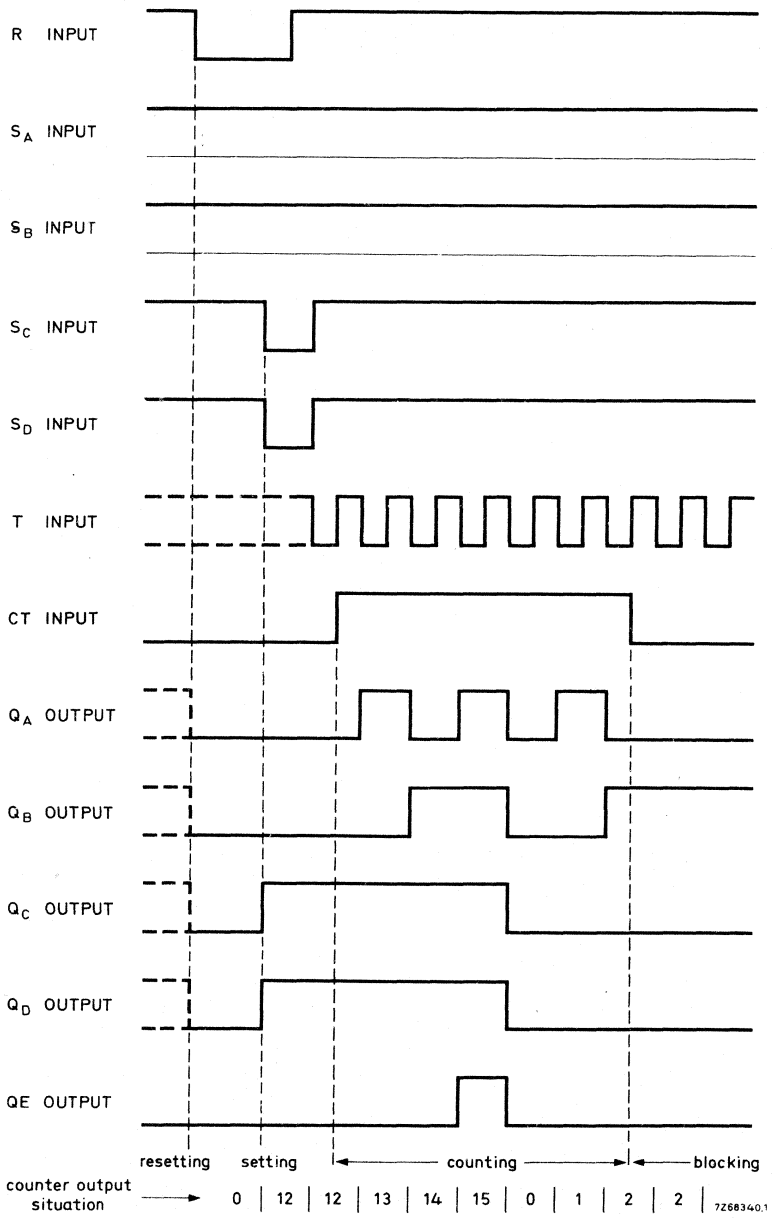
CHARACTERISTICS (continued)

FZJ141/FF34



CHARACTERISTICS (continued)

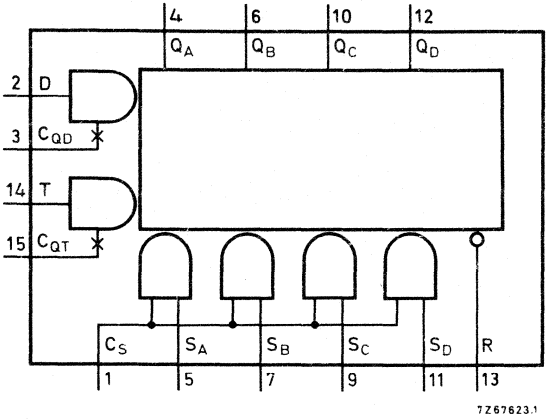
FZJ151/FF35

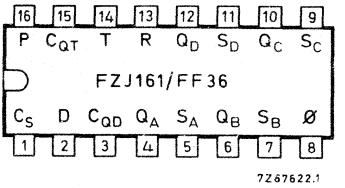


The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

SINGLE SYNCHRONOUS 4-BIT SHIFT REGISTER

with slow-down capability





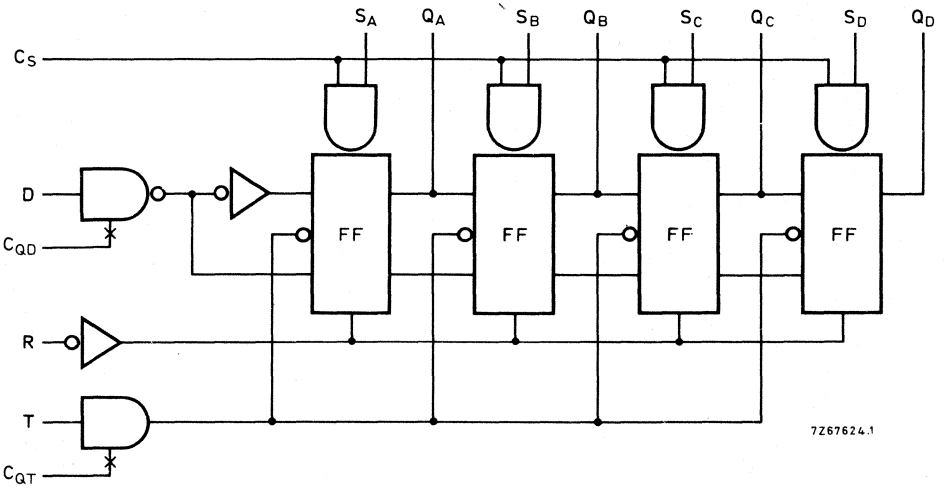
QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}	0 to +70		°C
Available d.c. fan-out T_{amb} = 0 to +70 °C — LOW state	N_{aL}	max.	10	
Average supply current at T_{amb} = 25 °C				
V_P = 13,5 V	I_{Pav}	typ.	21	mA
V_P = 17 V	I_{Pav}	typ.	26	mA
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II : V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V
Average power consumption (50% duty cycle) range I : V_P = 12 V	P_{av}	typ.	180	mW
range II : V_P = 15 V	P_{av}	typ.	390	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

GENERAL DESCRIPTION

The FZJ161/FF36 consists of a synchronous 4-bit shift register with serial or parallel inputs and serial or parallel outputs.
It is used as serial to parallel or parallel to serial converter, register and memory.
The device has slow-down inputs (C_{QD} and C_{QT}).

LOGIC DIAGRAM



Pin description

C_S = condition set input
D = data input
C_{QD} = slow-down data input
R = reset input
T = trigger input
C_{QT} = slow-down trigger input
S = set input
Q = output

FUNCTION TABLE

inputs						outputs			
C_S	R	S_A	S_B	S_C	S_D	Q_A	Q_B	Q_C	Q_D
L	L	X	X	X	X	L	L	L	L
H	L	H	L	H	H	H	L	H	H
L	H	X	X	X	X	shift			

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_I	max.	18	V
Input current at V_P = 17 V	$-I_{IL}$	max.	25	mA
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to	+70	°C
Uniform system supply voltage (range I)	V_P	11,4 to	13,5	V
(range II)	V_P	13,5 to	17	V
Available d.c. fan-out	N_{aL}	max.	10	
D.C. noise margin to all inputs: range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Power consumption (50 % duty cycle) at range I : V_{Pmax}	P_{av}	max.	340	mW
at range II : V_{Pmax}	P_{av}	max.	715	mW
Supply current at range I : V_P = 12 V	I_P	max.	33	mA
range II : V_P = 15 V	I_P	max.	42	mA
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

[1] Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.	Conditions and references: V_P (V)	Conditions and references:
Static data						
Voltages						
Input HIGH	V_{IH}	7,5	–	– V	11,4	
Input LOW	V_{IL}	–	–	4,5 V	11,4 and 13,5	
Output HIGH	V_{QH}	10	11,3	– V	11,4	V_{IL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7 V	11,4	V_{IH} = 7,5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	– V	11,4	
LOW	M_L	2,8	5,0	– V	11,4	
Currents						
Input HIGH	I_{IH}	–	–	1 µA	13,5	V_{IH} = 13,5 V
Input LOW						
C_S-input	$-I_{CSL}$	–	–	6 mA	13,5	V_{IL} = 1,7 V
other inputs	$-I_{IL}$	–	–	1,5 mA	13,5	V_{IL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25 mA	13,5	V_I = 0; V_Q = 0
Supply data						
Supply current	I_P	–	21	33 mA	13,5	V_I = 0

1) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
2) Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C.

	Symbol	min.	typ. [1]	max.		Conditions and references
Dynamic data						
Times						
Propagation delay:						
T → Q						
fall time	t_{pdf}	90	140	450	ns	
rise time	t_{pdr}	90	140	450	ns	
R → Q						
fall time	t_{pdf}	0,6	0,85	1,3	µs	V_{pd} = 4,5 V
$C_S \rightarrow Q, S_A \rightarrow Q_A, S_B \rightarrow Q_B, S_C \rightarrow Q_C, S_D \rightarrow Q_D$						N = 1
fall time	t_{pdf}	90	140	450	ns	C_L = 10 pF
rise time	t_{pdr}	100	240	500	ns	T_{amb} = 25 °C
output fall time	t_f	5	20	60	ns	
output rise time	t_r	70	150	290	ns	
Clock pulse duration	t_T	0,5	–	–	µs	V_{pd} = 4,5 V; N = 1
Clock rate	f_c	0,5	1,5	–	MHz	duty cycle 50%
Reset pulse duration	t_{RL}	0,5	–	–	µs	
Reset pulse duration during set operation	t_{RLS}	1	–	–	µs	
Set-up times at						V_{pd} = 4,5 V
S_A; S_B; S_C; S_D; C_S	t_{su}	1	–	–	µs	N = 1
D	t_{su}	0	–	–	µs	T_{amb} = 25 °C
Hold times at						
S_A; S_B; S_C; S_D; C_S	t_{hold}	1	–	–	µs	
D	t_{hold}	0,5	–	–	µs	
T input slope	$(-dV/dt)_{Tmin}$			1	V/µs	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.	Conditions and references: V_P (V)	Conditions and references:
Static data						
Voltages						
Input HIGH	V_{IH}	7,5	–	– V	13,5	
Input LOW	V_{IL}	–	–	4,5 V	13,5 and 17,0	
Output HIGH	V_{QH}	12,0	14,3	– V	13,5	V_{IL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7 V	13,5	V_{IH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	– V	13,5	
LOW	M_L	2,8	5,0	– V	13,5	
Currents						
Input HIGH	I_{IH}	–	–	1 µA	17,0	V_I = 17,0 V
Input LOW						
C_S-input	$-I_{CSL}$	–	–	7,2 mA	17,0	V_I = 1,7 V
other inputs	$-I_{IL}$	–	–	1,8 mA	17,0	V_I = 1,7 V
Output short-circuited [2]	I_{Qsc}	9	15	25 mA	17,0	V_I = 0; V_Q = 0
Supply data						
Supply current	I_P	–	26	42 mA	17,0	V_I = 0

[1] All typ. values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

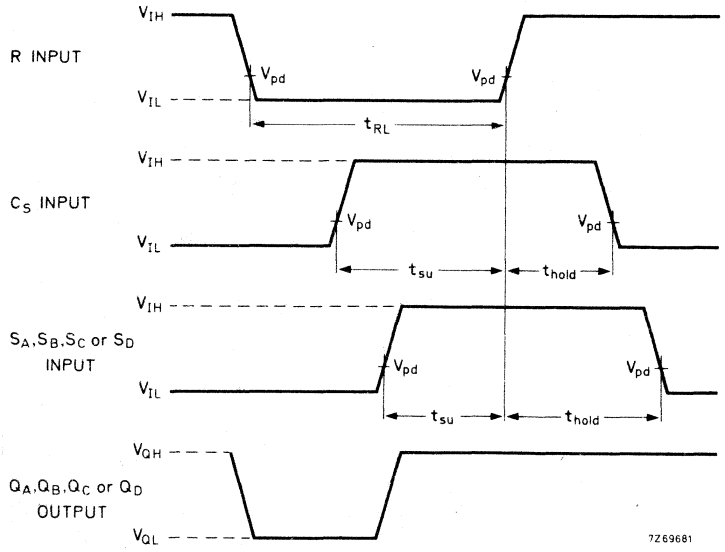
[2] Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.	Conditions and references
Dynamic data					
Times					
Propagation delay:					
T → Q					
fall time	t_{pdf}			ns	C_L = 10 pF N = 1 T_{amb} = 25 °C V_{pd} = 4,5 V
rise time	t_{pdr}			ns	
R → Q					
fall time	t_{pdf}			µs	
$C_S \rightarrow Q, S_A \rightarrow Q_A, S_B \rightarrow Q_B, S_C \rightarrow Q_C, S_D \rightarrow Q_D$			t.b.f.		
rise time	t_{pdr}			ns	
fall time	t_{pdf}			ns	
output fall time	t_f			ns	
output rise time	t_r			ns	
T input slope	$(-dV/dt)_{Tmin}$	1		V/µs	

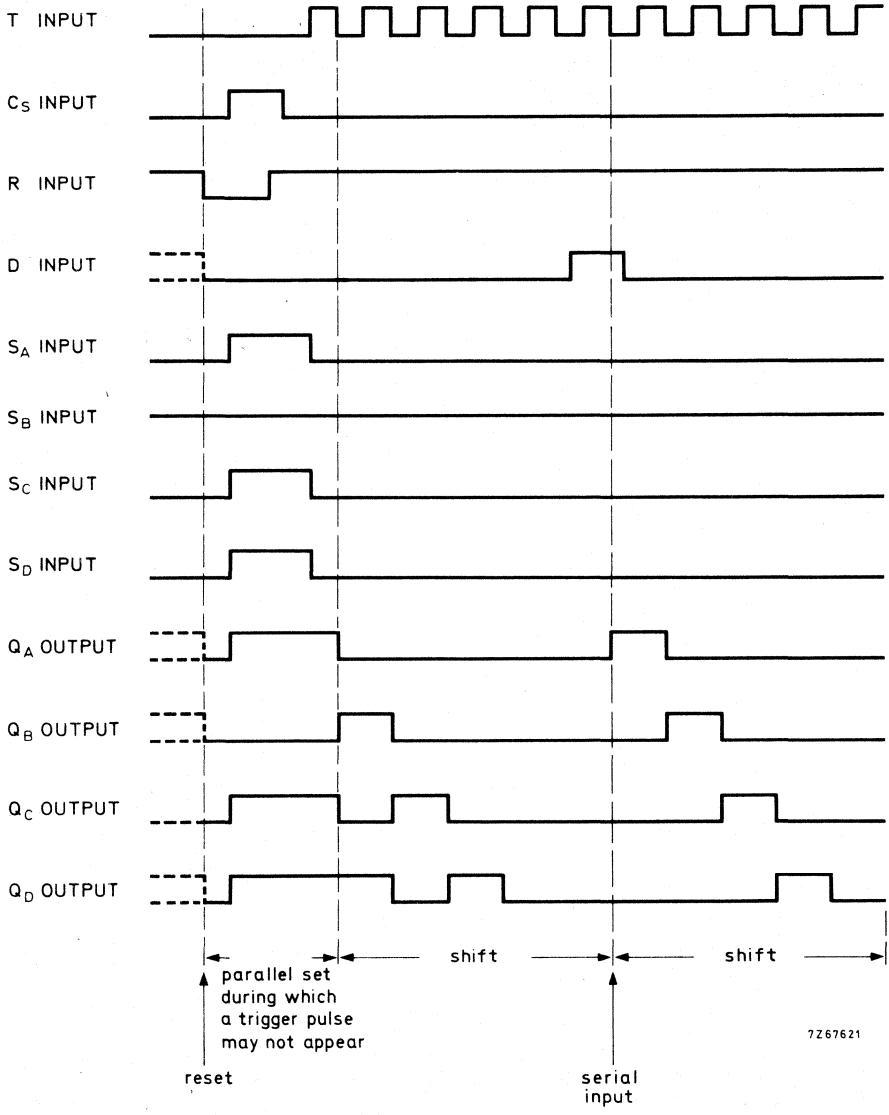
Waveforms for set operation



[1] All typical values under test conditions: T_{amb} = 25 °C and Vp = 15 V.

CHARACTERISTICS (continued)

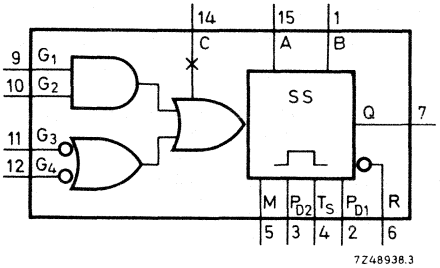
Dynamic data

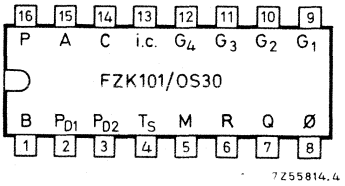


The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

MONOSTABLE MULTIVIBRATOR

with slow-down capability

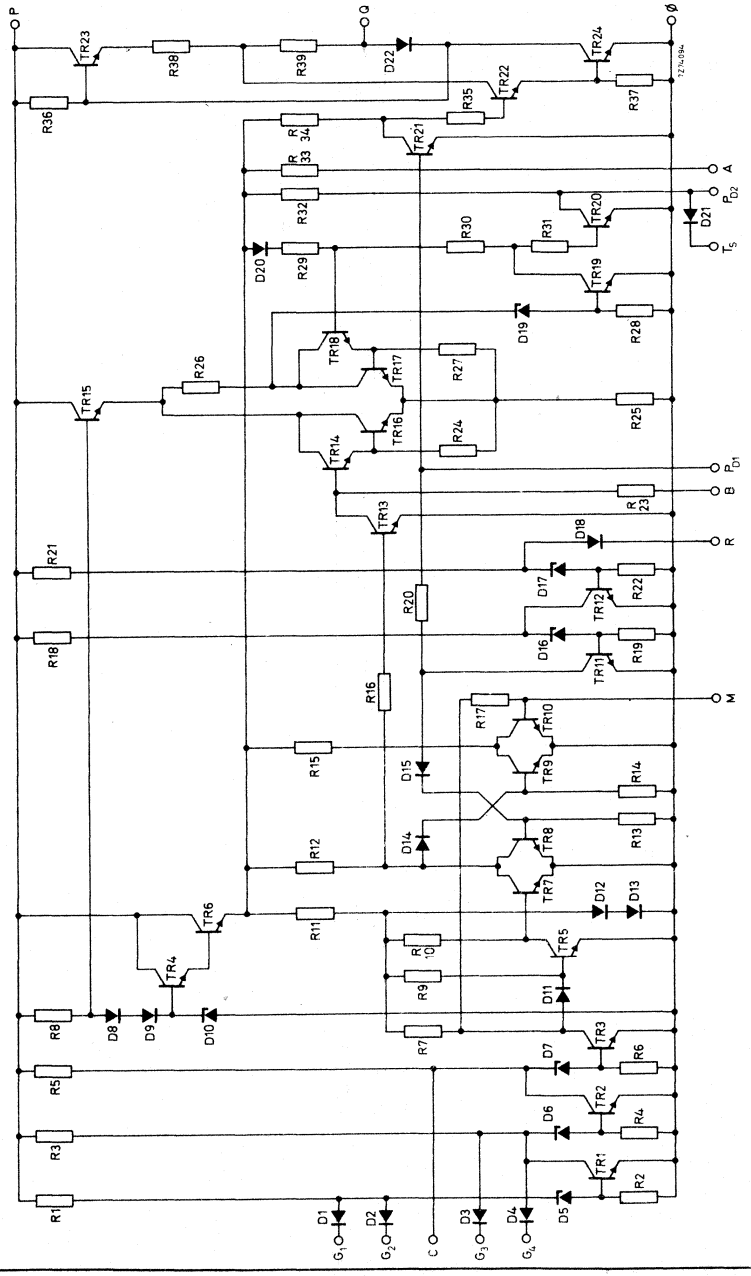




QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay: T_{amb} = 25 °C; V_{pd} = 4,5 V (ranges I and II)	t_{pdr}	typ.	270	ns
Available d.c. fan-out: LOW state	N_{aL}	max.	10	
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	M_L=M_H	typ.	5	V
	M_L	typ.	5	V
range II : VP = 15 V	M_H	typ.	8	V
Average power consumption				
(50% duty cycle) range I : V_P = 12 V	P_{av}	typ.	145	mW
range II: V_P = 15 V	P_{av}	typ.	180	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



GENERAL DESCRIPTION

The FZK101/OS30 has the following electrical functions and properties.

If the FZK101/OS30 is used as :

a. Monostable multivibrator: P_{D2}, and M have to be interconnected
b. Pulse delaying circuit : P_{D1} and P_{D2} have to be interconnected
c. Pulse shortening circuit : T_S and M have to be interconnected.

The output-pulse duration and pulse-delaying duration depend upon a resistor R_t which is externally connected between A and B and a capacitor C_t between B and ϕ. Output pulse durations and propagation delay are very stable with temperature and supply voltage changes.
The LOW state of output Q can be obtained by a LOW signal at input R.
The noise immunity of the G-inputs will be increased by connecting a capacitor (max. 500 pF) between slow-down terminal C and ϕ.
To the terminals P_{D1}, P_{D2}, T_S and M no voltages or currents may be applied.
External interconnections between these terminals have to be as short as possible.
If input signals are applied to the inputs G_3 and G_4, inputs G_1 and/or G_2 have to be LOW.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	18	V	
Output voltage	V_Q	max.	V_P		
Input voltage	V_G	max.	18	V	
Voltage difference between any two inputs		max.	18	V	
Storage temperature	T_{stg}	−65 to +150		°C	
Operating ambient temperature	T_{amb}	0 to +70		°C	
Slow-down input voltage	$+V_C$	max.	0,6	V	
	$-V_C$	max.	1,0	V	
Slow-down input current	$+I_C$	max.	2,0	mA	
	$-I_C$	max.	10,0	mA	
Output short-circuit duration	t_{Qsc}	max.	1	s	1)

1) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0	to	+70	°C
Uniform system supply voltage (range I)	V_P	11,4	to	13,5	V
(range II)	V_P	13,5	to	17	V
D.C. noise margin; range I at V_{Pmin}	M_L	min.		2,8	V
	M_H	min.		2,5	V
range II at V_{Pmin}	M_L	min.		2,8	V
	M_H	min.		4,5	V
Supply current at range I; output HIGH	I_{Pav}	typ.		12	mA
output LOW	I_{Pav}	typ.		13	mA
at range II; output HIGH	I_{Pav}	typ.		14	mA
output LOW	I_{Pav}	typ.		15	mA
Power consumption (50% duty cycle) at range I = V_{Pmax}	P_{av}	max.		257	mW
at range II = V_{Pmax}	P_{av}	max.		391	mW
Slow-down capacitor	C_M	max.		500	pF
Thermal resistance from system to ambient	R_{th}	max.		150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1])	max.	Conditions and references: V_P (V)	Conditions and references
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4,5 V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	– V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7 V	11,4	V_{GH} = 7,5 V; I_{QL} = 15 mA
D.C.noise margin: HIGH	M_H	2,5	5,0	– V	11,4	
LOW	M_L	2,8	5,0	– V	11,4	
Currents (per input)						
Input HIGH	I_{GH}	–	–	1,0 µA	13,5	V_G = 13,5 V (other inputs 0 V)
Input LOW	$-I_{GL}$	–	0,8	1,5 mA	13,5	V_{GL} = 1,7 V other inputs 13,5V
Output HIGH	$-I_{QH}$	–	–	0,1 mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	– mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited	$-I_{Qsc}$	10	30	50 mA	13,5	V_G= 0 V; V_Q= 0 V
Supply data						
Currents						
at V_{GL}	I_P	–	13,0	18,5 mA	13,5	
at V_{GH}	I_P	–	12,0	17,0 mA	13,5	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	symbol	min.	typ. [1]	max.		conditions and references
Dynamic data						
Times						
Propagation delay:						
G → Q						
fall time	t_{pdf}	110	180	450	ns	C_L = 10 pF
rise time	t_{pdr}	220	270	740	ns	N = 1
R → Q						
fall time	t_{pdf}	150	300	550	ns	T_{amb} = 25 °C
Output fall time	t_f	30	80	150	ns	V_{pd} = 4,5 V
Output rise time	t_r	50	100	200	ns	
Input pulse duration	t_{GH}	0,5	-	-	µs	
Reset pulse duration	t_{RL}	0,5	-	-	µs	
Recovery time	t_{rec}		$(C_o + C_t) \times 10^3$		s/F	C_o = 10 pF
Set-up time						between B and ϕ
at G_1, G_2	t_{su}	0	-	-	µs	
at G_3, G_4	t_{su}	0,5	-	-	µs	
Output pulse duration	t_{QH}	400			ns	V_P = 11,4 V
Output pulse duration	t_{QHmin}	650	700	780	ns	R_t = 0,5 kΩ, C_t = 2 nF
Capacitor	C_t	0	-	∞	µF	
Resistor	R_t	5	-	500	k Ω	see note 2
Input slope, G_1, G_2	$(-dV/dt)_{Tmin}$	0,1			V/µs	
G_3, G_4		1			V/µs	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
[2]) For higher accuracy R_t = 40 to 200 kΩ.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per input)							
Input HIGH	I_{GH}	–	–	1,0	µA	17	V_G = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8	mA	17	V_{GL} = 1,7 V; other inputs 17V
Output HIGH	$-I_{QH}$	–	–	0,1	mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited	$-I_{Qsc}$	15	37	50	mA	17	V_G = 0 V; V_Q = 0V
Supply data							
Currents							
at V_{GH}	I_P	–	14,0	20,0	mA	17	
at V_{GL}	I_P	–	15,0	21,5	mA	17	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	symbol	min.	typ. [1]	max.		conditions and references
Dynamic data						
Times						
Propagation delay:						
G ⟶ Q						
fall time	t_{pdf}		t.b.f.		ns	C_L = 10 pF
rise time	t_{pdr}				ns	N = 1
R ⟶ Q						
fall time	t_{pdf}				ns	T_{amb} = 25 °C
Output fall time	t_f				ns	V_{pd} = 4,5 V
Output rise time	t_r				ns	
Input pulse duration	t_{GH}	0,5	–	–	µs	
Reset pulse duration	t_{RL}	0,5	–	–	µs	
Recovery time	t_{rec}		$(C_o + C_t) \times 10^3$		s/F	C_o = 10 pF
Set-up time						between B and ϕ
at G_1, G_2	t_{su}	0	–	–	µs	
at G_3, G_4	t_{su}	0,5	–	–	µs	
Output pulse duration	t_{QHmin}	400	700		ns	V_P = 13,5 V
Output pulse duration	t_{QH}	650	700	780	ns	R_t = 0,5 kΩ
Capacitor	C_t	0	–	∞	µF	C_t = 2 nF
Resistor	R_t	5	–	500	kΩ	see note 2
Input slope, G_1, G_2	$(-dV/dt)_{Tmin}$	0,1			V/µs	
G_3, G_4		1			V/µs	

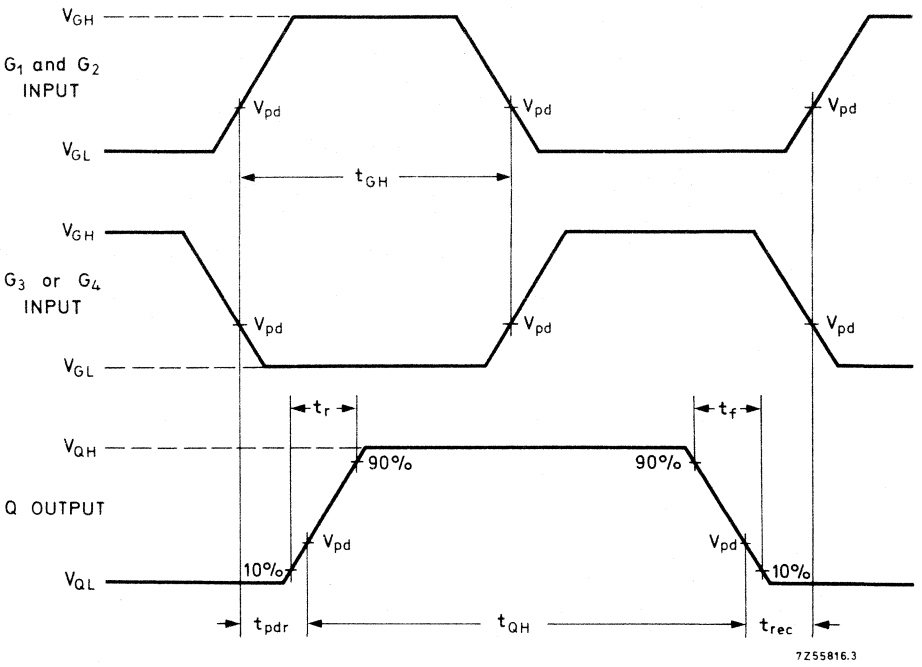
[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

[2]) For higher accuracy R_t = 40 to 200 kΩ.

CHARACTERISTICS (continued)

Dynamic data

FZK101/OS30 used as monostable multivibrator

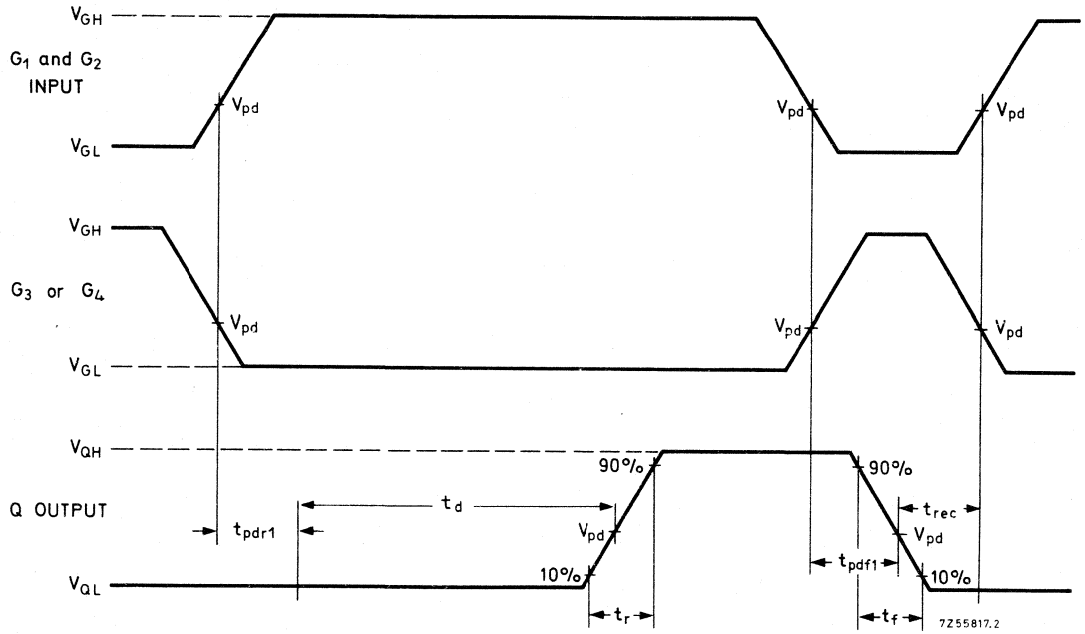


Conditions: P_{D2} and M interconnected
$t_{QH} = 0,7 \times R_t \ (C_o + C_t)$

CHARACTERISTICS (continued)

Dynamic data

FZK101/OS30 used as pulse delayed circuit

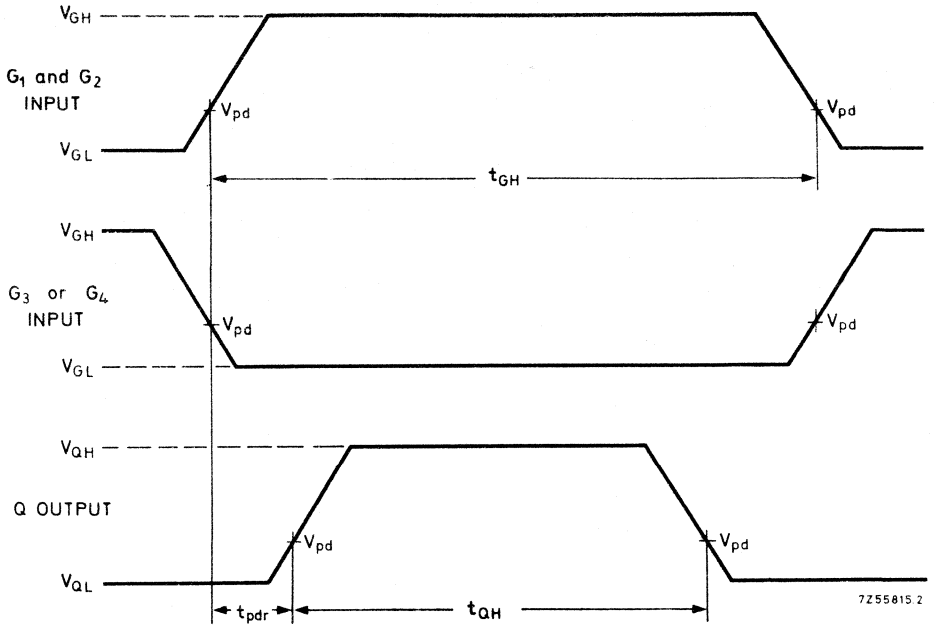


Conditions: P_{D1} and P_{D2} interconnected
$t_d = 0,7 \times R_t \ (C_o + C_t)$

CHARACTERISTICS (continued)

Dynamic data

FZK101/OS30 used as pulse shortened circuit



Conditions: T_S and M interconnected

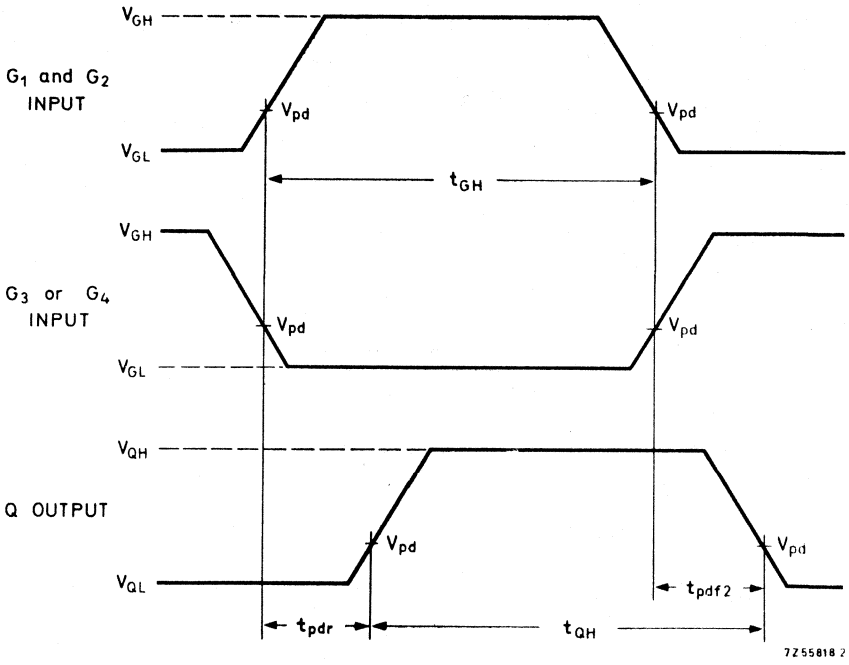
$t_{GH} > 0,7 \times R_t (C_o + C_t)$

$t_{QH} = 0,7 \times R_t (C_o + C_t)$

CHARACTERISTICS (continued)

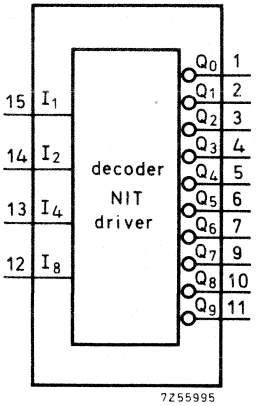
Dynamic data

FZK101/OS30 used as pulse shortened circuit

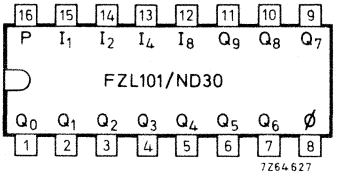


Conditions: T_S and M interconnected
$t_{GH} \leq 0,7 \times R_t (C_o + C_t)$
$t_{QH} = t_{GH}$

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.



SINGLE BCD-DECIMAL DECODER N.I.T.[1] DRIVER



QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Output current (per output):				
output transistor in off-state	I_Q	max.	2	mA
output transistor in on-state	I_Q	max.	20	mA
Output voltage at any output (output transistor in cut-off)	V_Q	max.	80	V
Average supply current at T_{amb} = 25 °C				
V_P = 13,5 V	I_{Pav}	typ.	17	mA
V_P = 17 V	I_{Pav}	typ.	18	mA
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	M_L	typ.	5,5	V
	M_H	typ.	4,5	V
range II : V_P = 15 V	M_L	typ.	5,5	V
	M_H	typ.	7,5	V
Average power consumption				
(50% duty cycle) range I : V_P = 12 V	P_{av}	typ.	205	mW
range II : V_P = 15 V	P_{av}	typ.	270	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

[1]) N.I.T. = numerical indicator tube.

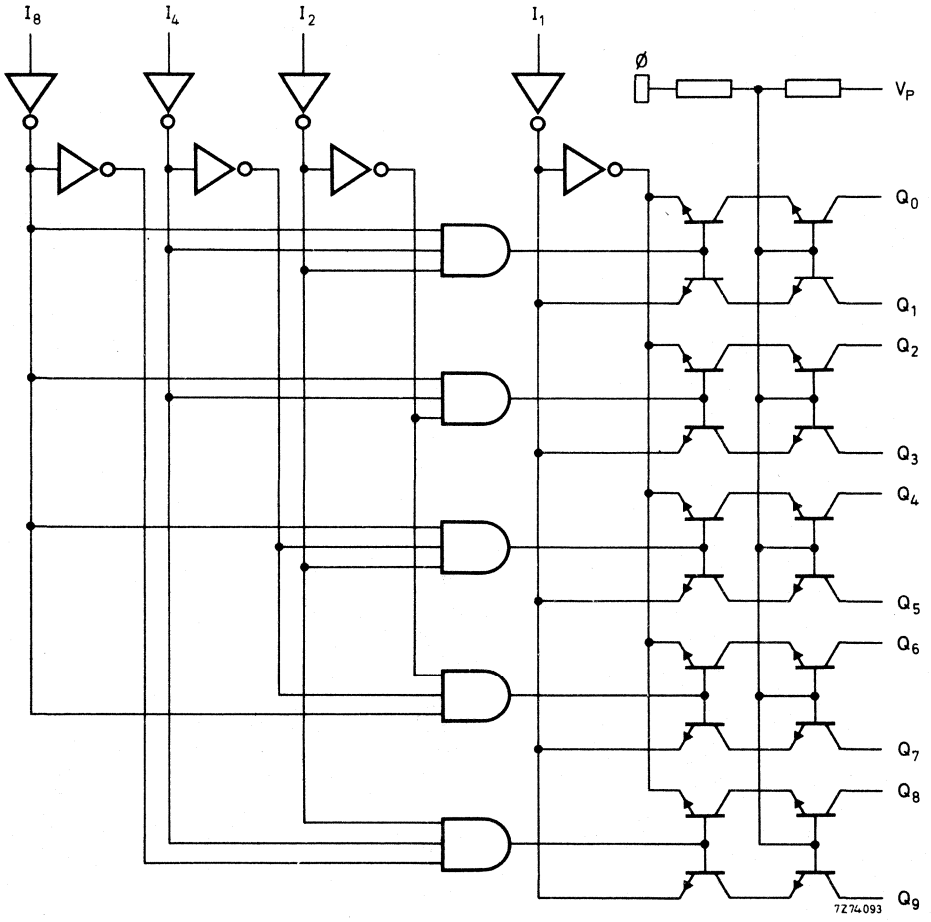
GENERAL DESCRIPTION

The FZL101/ND30 is a BCD (1-2-4-8 code) to decimal decoder incorporating high voltage output transistors for driving numerical indicator tubes.

Note

When used as HNIL decoder for every output a 10 kΩ resistor, connected to V_P, is required. At the outputs hazard pulses can appear during transition stages.

LOGIC DIAGRAM



FUNCTION TABLE

inputs				outputs (on-state = L)									
I_1	I_2	I_4	I_8	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage (at any output)	V_Q	max.	80	V
Input voltage	V_I	max.	18	V
Current into any output (off-state)	I_Q	max.	2	mA
Current into any output (on-state)	I_Q	max.	20	mA
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)	V_P	11,4 to 13,5		V
(range II)	V_P	13,5 to 17		V
D.C. noise margin to all inputs: range I at V_{Pmin}	M_L	min.	3,3	V
	M_H	min.	2,0	V
range II at V_{Pmin}	M_L	min.	3,3	V
	M_H	min.	4,0	V
Power consumption (50% duty cycle) at range I : V_{Pmax}	P_{av}	max.	340	mW
at range II : V_{Pmax}	P_{av}	max.	460	mW
Supply current at range I : V_P = 12 V	I_P	max.	25	mA
range II : V_P = 15 V	I_P	max.	27	mA
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ.[1])	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{IH}	8,0	–	–	V		
Input LOW	V_{IL}	–	–	5,0	V		
Output HIGH	V_{QH}	80	–	–	V	13,5	$-I_{QH}$ = 1 mA
Output LOW	V_{QL}	–	–	2,5	V	11,4	I_{QL} = 9 mA
D.C. noise margin							
HIGH	M_H	2,0	4,5	–	V	11,4	
LOW	M_L	3,3	5,5	–	V	11,4	
Currents							
Input HIGH	I_{IH}	–	–	1,0	µA	13,5	V_{IH} = 13,5 V
Input LOW	$-I_{IL}$	–	0,8	1,5	mA	13,5	V_{IL} = 0 V
Output HIGH:							
input combination 0 to 9	$-I_{QH}$	–	–	50	µA	13,5	V_{QH} = 70 V
input combination 10 to 15	$-I_{QH}$	–	–	5	µA	13,5	V_{QH} = 60 V
Supply data							
Supply current	I_P	–	17	25	mA	13,5	input voltage at I_1, I_4, I_8 = 0 V and at I_2 = 13,5 V

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C.

	Symbol	min.	typ. [1]	max.		Conditions and references
Dynamic data						
Times						
Propagation delay:						
$I_2 \longrightarrow Q_2$						
fall time	t_{pdf}	60	150	280	ns	C_L = 10 pF
rise time	t_{pdr}	30	70	210	ns	N = 1
$I_2 \longrightarrow Q_0$						T_{amb} = 25 °C
fall time	t_{pdf}	30	70	210	ns	V_L = 12 V
rise time	t_{pdr}	60	150	280	ns	R_L = 1 kΩ

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{IH}	8,0	–	–	V		
Input LOW	V_{IL}	–	–	5,0	V		
Output HIGH	V_{QH}	80	–	–	V	17,0	$-I_{QH}$ = 1 mA
Output LOW	V_{QL}	–	–	2,5	V	13,5	I_{QL} = 9 mA
D.C. noise margin							
HIGH	M_H	4,0	7,5	–	V	13,5	
LOW	M_L	3,3	5,5	–	V	13,5	
Currents							
Input HIGH	I_{IH}	–	–	1,0	µA	17,0	V_I = 17,0 V
Input LOW	$-I_{IL}$	–	1,0	1,8	mA	17,0	V_I = 0 V
Output HIGH: input combination 0 to 9	$-I_{QH}$	–	–	50	µA	17,0	V_{QH} = 70 V
Output HIGH: input combination 10 to 15	$-I_{QH}$	–	–	5	µA	17,0	V_{QH} = 60 V
Supply data							
Supply current	I_P	–	18	27	mA	17,0	input voltage at I_1, I_4, I_8 = 0 V and at I_2 = 13,5 V

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

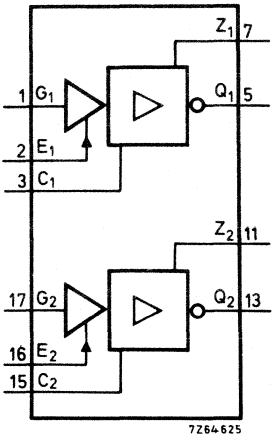
CHARACTERISTICS (continued)

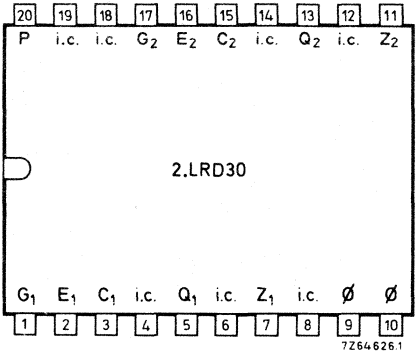
	Symbol	min. typ. [1] max.	Conditions and references
Dynamic data			
Propagation delay:			
$I_2 \longrightarrow Q_2$			
fall time	t_{pdf}	t.b.f.	
rise time	t_{pdr}		
$I_2 \longrightarrow Q_0$			
fall time	t_{pdf}		
rise time	t_{pdr}		

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL LAMP/RELAY DRIVER





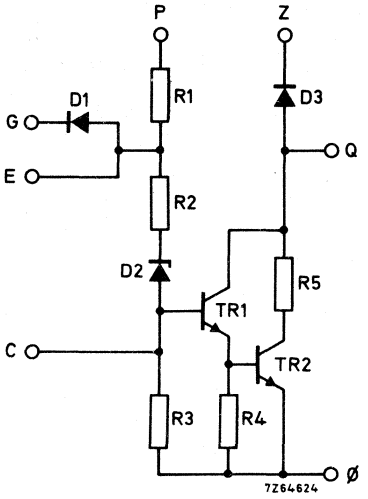
QUICK REFERENCE DATA				
Supply voltage	V_P		11,4 to 17,0	V
when loaded	V_{Pload}	max.	30	V
Operating ambient temperature	T_{amb}		−30 to + 75	°C
Output current (d.c.) T_{amb} = − 35 to +75 °C; V_{Pload} = 30 V	I_{QL}	max.	200	mA
Non-repetitive peak output current t_{max} = 20 ms	I_{QLM}	max.	400	mA
D.C. noise margin at T_{amb} = 25 °C	M_L	typ.	6	V
	M_H	typ.	7	V
Average power consumption T_{amb} = 25 °C; V_P = 15 V; Q = unloaded	P_{av}	typ.	40	mW

Note

Necessary input drive equal to 3 gate loads.

PACKAGE OUTLINE 20 lead dual in-line (see general section).

CIRCUIT DIAGRAM



GENERAL DESCRIPTION

The 2.LRD30 is a dual driver for output currents up to 200 mA at a supply voltage of maximum 30 V; it is used for driving lamps and relays.
The number of gate inputs can be extended by connecting up to 15 Si diodes to the expander terminal E (connect anodes of diodes to E) *).
With inductive loads the built-in clamping diode D3 must be used. This is done by connecting terminal Z to the load supply voltage, to protect the output transistor against damage caused by high inductive voltages.
To improve the a.c. noise immunity by increasing the propagation delay time, a capacitor has to be connected between terminals C and ϕ.
With a resistive load, the capacitor is connected between C and Q.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Supply voltage	V_P	max.	20 V
when loaded	V_{Pload}	max.	30 V
Output voltage	V_{QH}	max.	30 V
Input voltage	V_{GH}	max.	30 V
Negative input voltage	$-V_G$	max.	4 V
Storage temperature	T_{stg}		−30 to + 85 °C
Operating ambient temperature	T_{amb}		−30 to + 75 °C

*) Diode leads should be kept as short as possible.

CHARACTERISTICS

Test conditions: T_{amb} = −30 to +70 °C

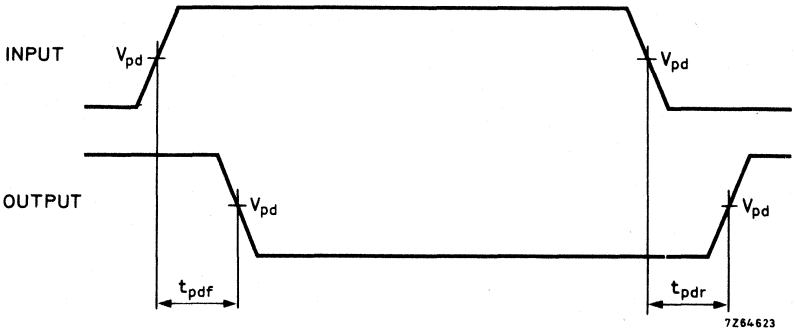
	symbol	min.	typ.[1])	max.		Conditions and references: V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	8,0	–	–	V	11,4 and 17,0	V_Q = LOW
Input LOW	V_{GL}	–	–	4,5	V	11,4 and 17,0	I_Q = 0,5 mA
Output LOW	V_{QL}	–	0,9	1,3	V	11,4	$V_{GH} \geq 8,0$ V; I_Q = 200 mA
D.C. noise margin: HIGH	M_H	2,0	7	–	V	11,4	
LOW	M_L	2,8	6	–	V	11,4 and 17,0	
Currents							
Input HIGH	I_{GH}	–	0,1	10	μA	11,4 and 17,0	V_G = 17,0 V
Input LOW	$-I_{GL}$	–	–	5,4	mA	17,0	V_{GL} = 1,7 V
Output HIGH	I_{QH}	–	–	0,5	mA	11,4 and 17,0	$V_{GL} \leq 4,5$ V; V_{Pload} = 30 V
Output LOW	I_{QL}	–	–	200	mA	11,4 and 17,0	$V_G \geq 8,0$ V
Non-repetitive peak value; t_{max} = 20 ms	I_{QLM}	–	–	400	mA	11,4 and 17,0	$V_{GH} \geq 8,0$ V
Supply data							
Currents							
at V_{QH}	I_P	–	4,2	4,9	mA	17,0	V_G = 1,7 V
at V_{QL}	I_P	–	2,2	3,4	mA	17,0	$V_G \geq 8,0$ V
Dynamic data							
Input rise time	t_r	0,1	–	–	V/μs		
Input fall time	t_f	0,1	–	–	V/μs		

[1]) Typical values specified at V_P = 15 V and T_{amb} = 25 °C.

CHARACTERISTICS (continued)

Dynamic data

Loading capacitor connected between C and ø.



Waveforms illustrating measurement of t_{pdr} and t_{pdf}.

Measuring conditions: V_P = 15 V
I_{QL} = 200 mA
C_L = 10 pF
resistive load

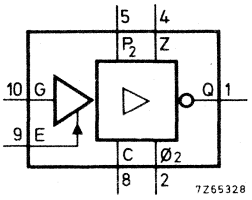
input waveform: $V_{pd} = \frac{1}{2} V_P$
output waveform: $V_{pd} = \frac{1}{2} V_{Pload}$

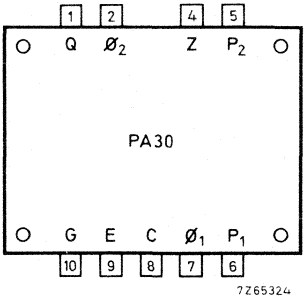
$t_{pdf} = (0,55 + 0,55 \times C_L)$ ns
$t_{pdr} = (0,30 + 0,30 \times C_L)$ ns

C_L in nF; C_L is 10 to 1000 nF

The 30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

POWER AMPLIFIER





top view

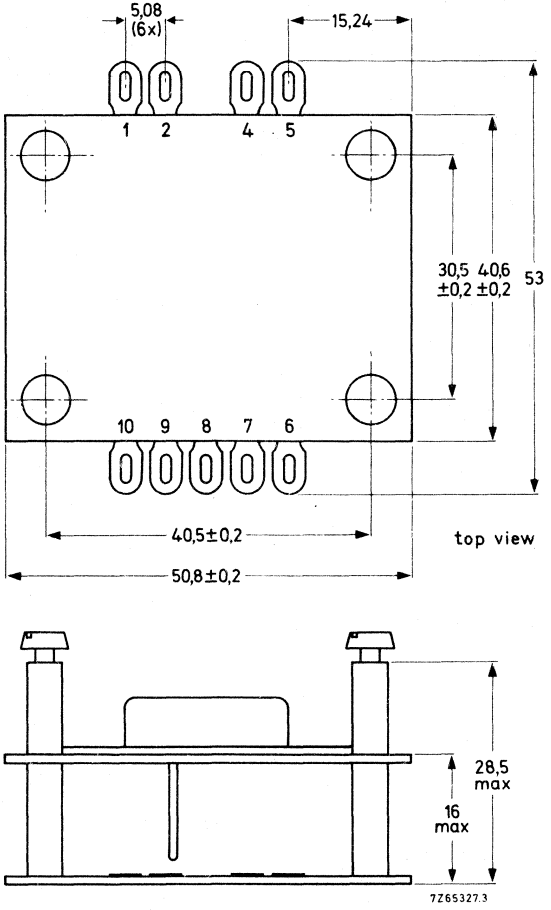
QUICK REFERENCE DATA				
Supply voltage	V_{P1}		11,4 to 17,0	V
	V_{PS}		11,4 to 55	V
Operating ambient temperature	T_{amb}		−30 to +75	°C
Output current (t_{av} = 20 ms)	I_{QL}	max.	2	A
Repetitive peak output current	I_{QLM}	max.	5	A
D.C. noise margin at T_{amb} = 25 °C	M_L	typ.	5	V
	M_H	typ.	8	V
Average power consumption at T_{amb} = 25 °C V_{P1} = 15 V; Q = unloaded; V_{PS} = 15 V; R_V = 0	P_{av}	typ.	240	mW

PACKAGE OUTLINE 9 leads special execution (see next page).

PACKAGE OUTLINE

Dimensions in mm

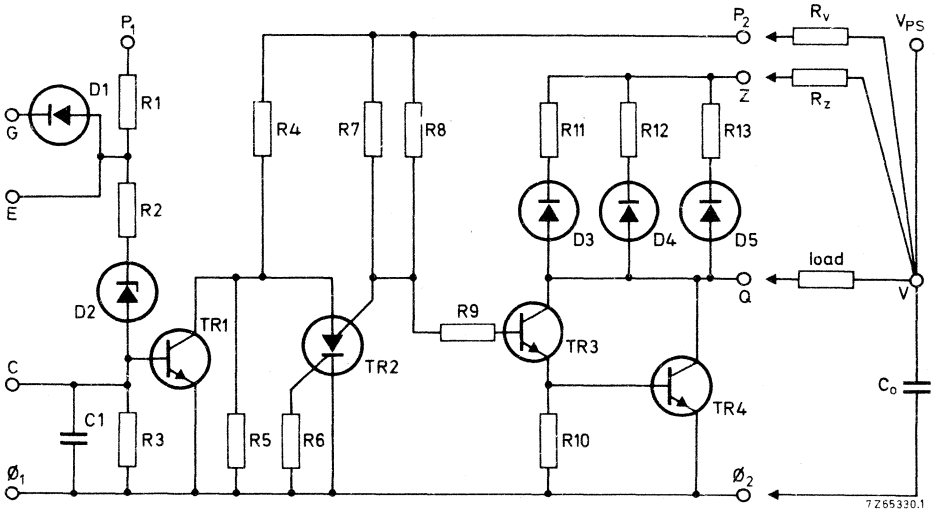
9 leads special execution



GENERAL DESCRIPTION

The PA30 is a power amplifier for output currents up to 2 A and output voltages up to 55 V, intended for driving heavy resistive and inductive loads.
The number of gate inputs can be extended by connecting up to 15 diodes (type BAW62) to the expander terminal E (connect anode of diode to E). *)
To increase the a.c. noise immunity, a capacitor can be connected between terminals C and ϕ_1 (see also "Operating notes"). The load has to be connected between Q and point V.
For inductive loads, terminal Z must also be connected to V, if necessary via a series resistor R_Z (see note 3 of "Operating notes").
Dependent on the V_{PS} value, a resistor R_V must be connected between terminal P_2 and point V (see note 1 of "Operating notes").
When the wire connection between V and supply voltage unit V_{PS} has some inductance, it is necessary to connect a capacitor C_o ($\approx 10\ \mu F$ per metre of wire) between V and ϕ_2 as close as possible to the unit.

CIRCUIT DIAGRAM



*) Diode leads should be kept as short as possible.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages	V_{P1}	max.	20	V	[1]
	V_{PS}	max.	55	V	
Output voltage	V_{QH}	max.	55	V	
Input voltage	V_{GH}	max.	30	V	
Negative input voltage	$-V_{GL}$	max.	4	V	
Output current (average; t_{av} = 20 ms)	I_{QL}	max.	2	A	
Output current (peak value)	I_{QLM}	max.	5	A	
Storage temperature	T_{stg}		−40 to +85	°C	
Operating ambient temperature	T_{amb}		−30 to +75	°C	

1) See note 1 of "Operating notes".

CHARACTERISTICS Test conditions: T_{amb} = −30 to +75 °C

	Sym-bol	min.	typ. [1]	max.		Conditions and references: V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	11,4 and 17,0	V_Q = LOW
Input LOW	V_{GL}	–	–	4,5	V	11,4 and 17,0	V_Q = HIGH
Output HIGH	V_{QH}	–	–	55	V	11,4 and 17,0	I_Q = 5 mA $V_G \leq 4,5$ V
Output LOW	V_{QL}	–	0,9	1,3	V	11,4 and 17,0	I_Q = 2 A $V_G \geq 7,5$ V
D.C. noise margin: LOW	M_L	2,8	5	–	V	11,4 and 17,0	
HIGH	M_H	2,5	8	–	V	11,4	
Currents							
Input HIGH	I_{GH}	–	0,1	10	µA	17,0	V_G = 17 V
Input LOW	$-I_{GL}$	–	–	5,1	mA	17,0	V_G = 1,7 V
Output HIGH	I_{QH}	–	1 µA	5	mA	11,4 and 17,0	V_{QH} = 55 V $V_G \leq 4,5$ V
Output LOW (t_{av} = 20 ms)	I_{QL}	–	–	2	A	11,4 and 17,0	V_{QL} = 1,3 V $V_G \geq 7,5$ V
(peak value)	I_{QLM}	–	–	5	A	11,4 and 17,0	V_{QL} = 1,3 V

[1]) All typical values under test conditions: V_{P1} = 15 V; V_{PS} = 15 V; R_v = 0; T_{amb} = 25 °C.

CHARACTERISTICS (continued) Test conditions: T_{amb} = −30 to +75 °C

	Symbol	min. typ. [1] max.	Conditions and references	
			V_P (V)	
Supply data				
Currents	I_{P1}	− 4,3 − mA	15	V_G = 1,7 V
	I_{P1}	− 2,6 − mA	15	V_G ≥ 7,5 V
	I_{P2}	− 14,5 − mA	15	V_G ≤ 4,5 V
	I_{P2}	− 12,5 − mA	15	V_G ≥ 7,5 V

[1]) All typical values under test conditions: V_{P1} = 15 V; V_{PS} = 15 V; R_V = 0; T_{amb} = 25 °C.

OPERATING NOTES

1. Supply voltage V_{PS}

When terminal P_2 is directly connected to point V the value of V_{PS} must be between 11,4 V and 19 V (15,2 V ± 25%).
By connecting a suitable resistor (R_V) between P_2 and V, any supply voltage V_{PS} between 11,4 and 55 V may be used, having a tolerance of ± 25%.
The values of R_V can be calculated from:

$$R_V = 75\ (V_{PSnom} - 15)\ \Omega \pm 8\%$$

2. For capacitor C_o see "General description"

3. Unit loaded with an inductive load

When an inductive load is switched, the built-in diodes (which protect the output transistor against voltage transients) have to be connected (Z to point V).
This protection is realized at the expense of a very long decay time of the current in the load.
At V_{PS} below 55 V a resistor R_Z may be connected in series with the protection diodes to decrease this decay time.

The maximum permissible value of R_Z can be calculated from:

$$R_Z < \frac{1}{I_Q}\ (55 - V_{PSmax})\ \Omega$$

Where: I_Q = the load current at switching-off.

The decay time of the load current can be calculated from:

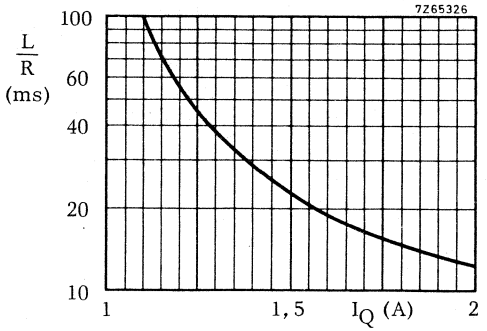
$$I_L = I_Q \exp - \frac{t}{L/R}$$

Where: I_Q = the load current at switching-off in amperes
L = inductance of the load in henrys
R = sum resistance of load and possible applied R_Z in ohms

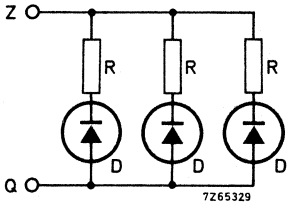
Note: V may be connected directly to Z ($R_Z = 0$) if there are no problems with decay time.

OPERATING NOTES (continued)

4. Inductance of the load



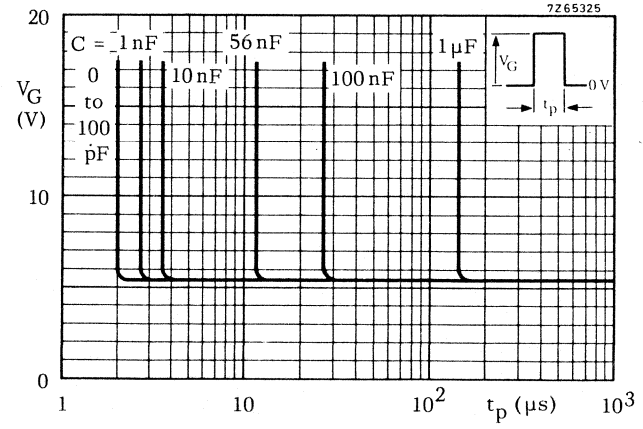
The maximum allowable inductance of the load can be calculated from the maximum permissible value of L/R as follows from the graph above.
I_Q = the load current at switching-off.
R = sum resistance of load and possible applied R_Z.



R = 1,5 Ω
D = BAX12

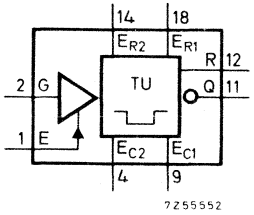
When the above circuit is connected between the terminals Z and Q, loads with any inductance value and currents up to 2 A can be applied.

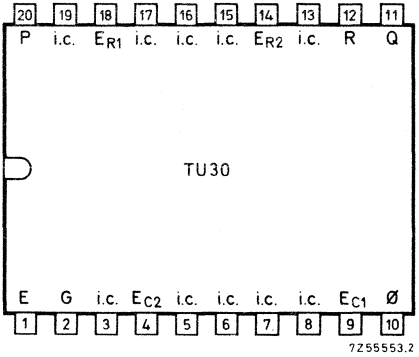
5. Input voltage versus input pulse duration as a function of a capacitor between terminals C and ϕ_1.



The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

TIMER UNIT

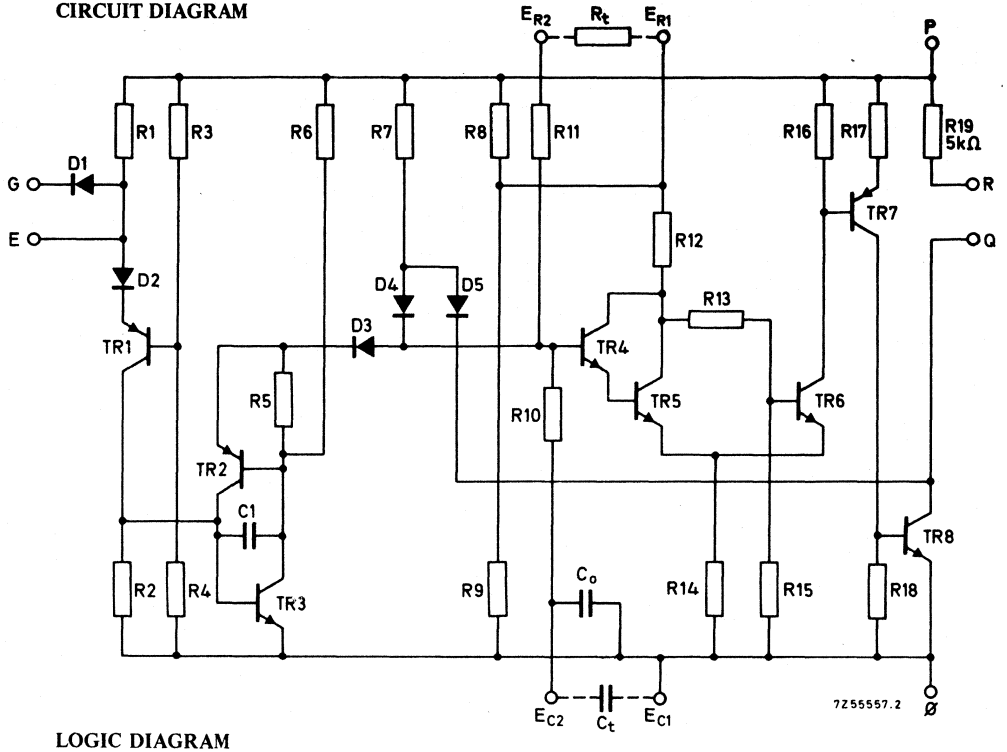




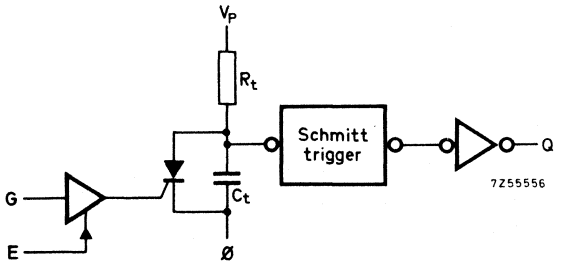
QUICK REFERENCE DATA				
Supply voltage	V_P	11,4 to 17,0		V
Operating ambient temperature	T_{amb}	−30 to +75		°C
Delay time; T_{amb} = 25 °C	t_d	max.	10	s/µF
Available d.c. fan-out (T_{amb} = −25 to +70 °C) LOW state	N_{aL}	max.	22	
D.C. noise margin at T_{amb} = 25 °C, V_P = 15 V	M_L	typ.	6,5	V
	M_H	typ.	6,5	V
Power consumption at T_{amb} = 25 °C	P_{av}	typ.	300	mW

PACKAGE OUTLINE 20 lead dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC DIAGRAM



GENERAL DESCRIPTION

The TU30 is a direct-coupled timer that gives a constant delay irrespective of the duration of the gate input signal. The delay begins when the gate input changes from HIGH to LOW (see timing diagram). When the gate input changes from LOW to HIGH, the output goes LOW. A gate input signal during a delay cycle will restart the delay.

The length of the delay is determined by an external capacitor connected across terminals E_{C1} and E_{C2}, and an external resistor connected across terminals E_{R1} and E_{R2}.

The number of gate inputs can be extended by connecting up to 15 diodes (BAW62) to the expander input terminal E (connect anode of diode to terminal E). *)
To prevent capacitive coupling with other lines the connection between the diodes and expander inputs must be as short as possible.

When using the TU30 to drive other members of the FZ/30-Series, interconnect terminals Q and R.

When using it to drive a small relay, connect the relay across terminals Q and P, and leave terminal R unconnected (floating).

When driving an inductive load (also relays), connect a clamping diode (such as a BAW62) across terminals Q and P (anode of diode to terminal Q). *)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_{QH}	max.	V_P	
Output current (Q and R not interconnected)	I_{QL}	max.	46	mA
Input voltages	V_G	max.	18	V
	$-V_G$	max.	1	V
Input current (for negative input voltage)	$-I_G$	max.	2,0	mA
Output capacitance	C_L	max.	500	pF
Storage temperature	T_{stg}	−25 to +85		°C
Operating ambient temperature	T_{amb}	−25 to +70		°C

*) Diode leads should be kept as short as possible.

CHARACTERISTICS Test conditions: T_{amb} = −25 to +70 °C.

	Sym-bol	min.	typ[1])	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	6,8	–	–	V	11,4	I_{QL} = 43 mA *)
	V_{GH}	9,3	–	–	V	17,0	I_{QL} = 46 mA **)
Input LOW	V_{GL}	–	–	4,5	V	11,4	V_{QHmin} = 0,9 V_P
	V_{GL}	–	–	7,3	V	17,0	$-I_{QH}$ = 0,25 mA
Output HIGH	V_{QH}	10	13	–	V	11,4	V_{GL} = 4,5 V; $-I_{QH}$ = 0,25 mA
	V_{QH}	15,3	–	–	V	17,0	V_{GL} = 4,5 V; $-I_{QH}$ = 0,25 mA
Output LOW	V_{QL}	–	–	0,5	V	11,4	V_{GH} = 6,8 V; I_{QL} = 43 mA *); I_{QL} = 46 mA **)
D.C. noise margin: HIGH	M_H	3,2	–	–	V	11,4	V_{GH} = 10 V
LOW	M_L	2,8	–	–	V	11,4	V_{GL} = 1,7 V
HIGH	M_H	–	6,5	–	V	15,0	V_{GH} = 1,4 V
LOW	M_L	–	6,5	–	V	15,0	V_{GL} = 1,0 V
Currents							
Input HIGH	I_{GH}	–	–	1	µA	17,0	V_{GH} = 17,0 V
Input LOW	$-I_{GL}$	–	–	0,95	mA	11,4	V_{GL} = 1,7 V
	$-I_{GL}$	–	–	1,6	mA	17,0	V_{GL} = 1,7 V
Output HIGH	$-I_{QH}$	–	–	0,50	mA	11,4	V_{GL} = 4,5 V; V_{QH} = 10 V *)
	$-I_{QH}$	–	–	0,50	mA	17,0	V_{GL} = 7,3 V; V_{QH} = 15,3 V *)
Output LOW	I_{QL}	–	–	43	mA	11,4 and 17,0	V_{GH} = 0,6 V_P; V_{QL} = 0,5 V *)
	I_{QL}	–	–	46		11,4 and 17,0	V_{GH} = 0,6 V_P; V_{QL} = 0,5 V **)
Supply data							
Currents							
Output HIGH	I_P	–	6,5	7,5	mA	17,0	V_G = 0 V
Output LOW	I_P	–	17	20	mA	17,0	V_G = 17 V

1) Typ. values specified at V_P = 15 V and T_{amb} = 25 °C.
*) Terminal R connected to terminal Q.
**) Terminal R not connected.

CHARACTERISTICS at V_P = 15 V; T_{amb} = 25 °C

Dynamic data

Gate input HIGH duration	T_{GH}	>	5	µs	
Output rise time for C_L = 10 pF	t_{Qr}	typ.	110	ns	1)
Output fall time for R_C = 5 kΩ; C_L = 10 pF	t_{Qf}	typ.	50	ns	
Fall propagation delay time	t_{pdf}	typ.	3	µs	
Delay time (C_t in F; R_t in Ω)	t_d	>	1	ms	
		typ.	$C_t(R_t+10\,k\Omega)$	s	
Timing resistor	R_t		0 Ω to 10	MΩ	
Timing capacitor	C_t		no limit		2)
Change in delay time versus temperature (R_t = 1 MΩ; V_P = 15 V)		typ.	−0,1	%/°C	
Change in delay time versus supply voltage (T_{amb} = 25 °C; R_t = 1 MΩ)		typ.	−0,5	%/°C	

1) t_{Qr} = (11 x C_L) ns. C_L is the wiring capacitance in pF with a maximum permissible value of 500 pF.

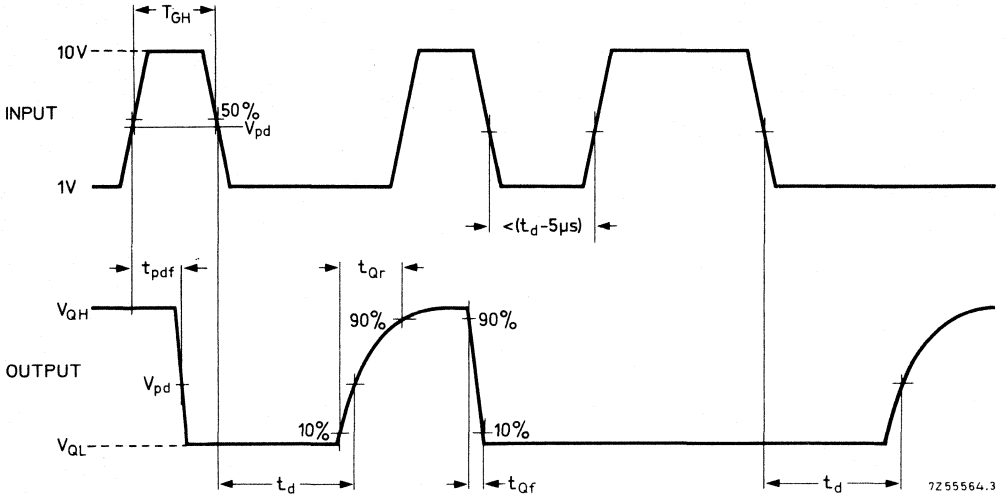
2) Preferred value for C_t: > 1 nF.
The circuit is not developed for electrolytic capacitors because of their high leakage currents. However, electrolytic capacitors may be used (+ side connected to terminal E_{C2}), provided that the charge current is large compared to the leakage current of the capacitor e.g.:

$$I_{charge} > 10.I_{leakage}$$

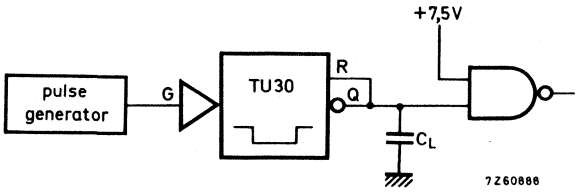
$$\text{where } I_{charge} = \frac{0,3\,V_P}{R_t + 10\,k\Omega}$$

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns
t_f = 120 ns
t_{GH} = 5 µs
V_{pd} = 4,5 V



Measuring conditions: V_P = +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = +25 °C

Waveforms and loading circuit illustrating measurement of t_{Qr}, t_{Qf} and t_{pdf}.

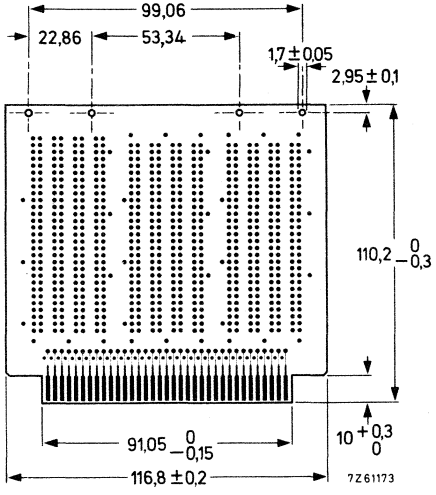
Accessories for HNIL FZ/30-Series

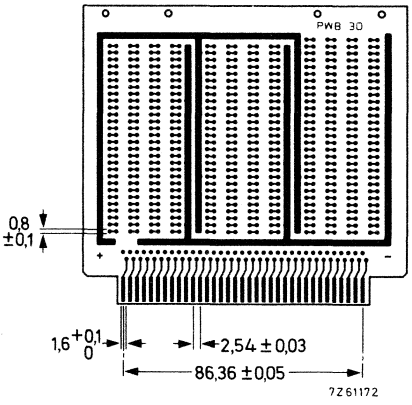
EXPERIMENTERS' PRINTED-WIRING BOARD

for integrated circuits in dual-in-line package

This printed-wiring board has been designed for dual-in-line packages with a different number of pins; the packages are connected with each other and with the connector by means of insulated wires. The packages are mounted perpendicular to the connector, so the wires to the connector can run parallel to the rows of pins of the packages, instead of between the pins.
The maximum number of packages which can be mounted is given below:

number of pins of the package	max. number of packages per board
2 x 7	24
2 x 8	18
2 x 9	18
2 x 10	12
2 x 11	12





Material	glass-epoxy
Board thickness	1,6 mm
Holes	plated-through, 0,8 mm diameter, provided with soldering lands
Contact pads	2 x 35, gold-plated

Circuit blocks
40-Series and CSA70 (L)

INTRODUCTION

In any analogue system for instrumentation and control there are a number of basic functions. The units of the 40-Series have been developed to perform basic analogue functions, thus to save the system designer considerable time and costs.
Great care has been taken to make them versatile so that a greater part of the required functions in analogue systems can be performed without needing complex external circuitry.
Being capable of handling signals down to d.c. they are very reliable and operate with a high degree of stability.

The 40-Series units find wide application in, for instance.

signal generating circuits
process and alarm circuits
closed-loop power control systems
A-D and D-A converters
electronic measuring instruments

Extensive information on the principles and applications can be found in the Application Book: "Measurement and control with the 40-Series modules".

The 40-Series comprises the following units:

DOA 40, Operational Amplifier
DZD 40, Differential Zero Detector
PSM 40, Phase Shift Module

OPERATIONAL AMPLIFIER

GENERAL

The DOA40 is a high gain, wide band, low drift d.c. differential amplifier. Input voltage offset can be externally corrected.
A 6 dB/octave roll-off network is built-in. Terminals are available to connect an external roll-off network.

This unit is developed for use with power supplies of 15 V. As many control systems use 12 V supplies, some data are given for use at these voltages at the end of the specification.

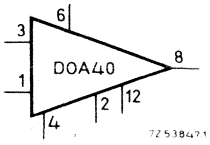


Fig.1. Drawing symbol

Dimensions in mm

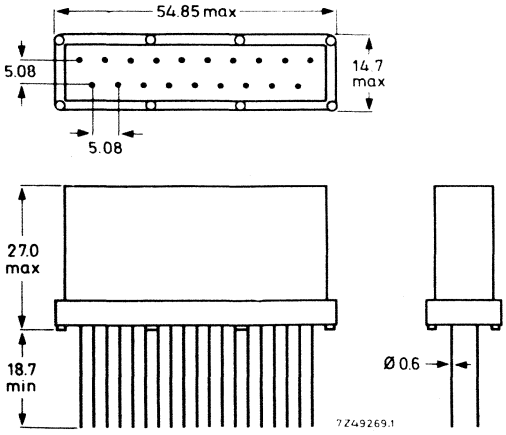


Fig.2.

The complete circuit is potted inside a metal can with 19 wire terminals. The can is internally connected to terminal 10 (0 V)

Circuit diagram and terminal location

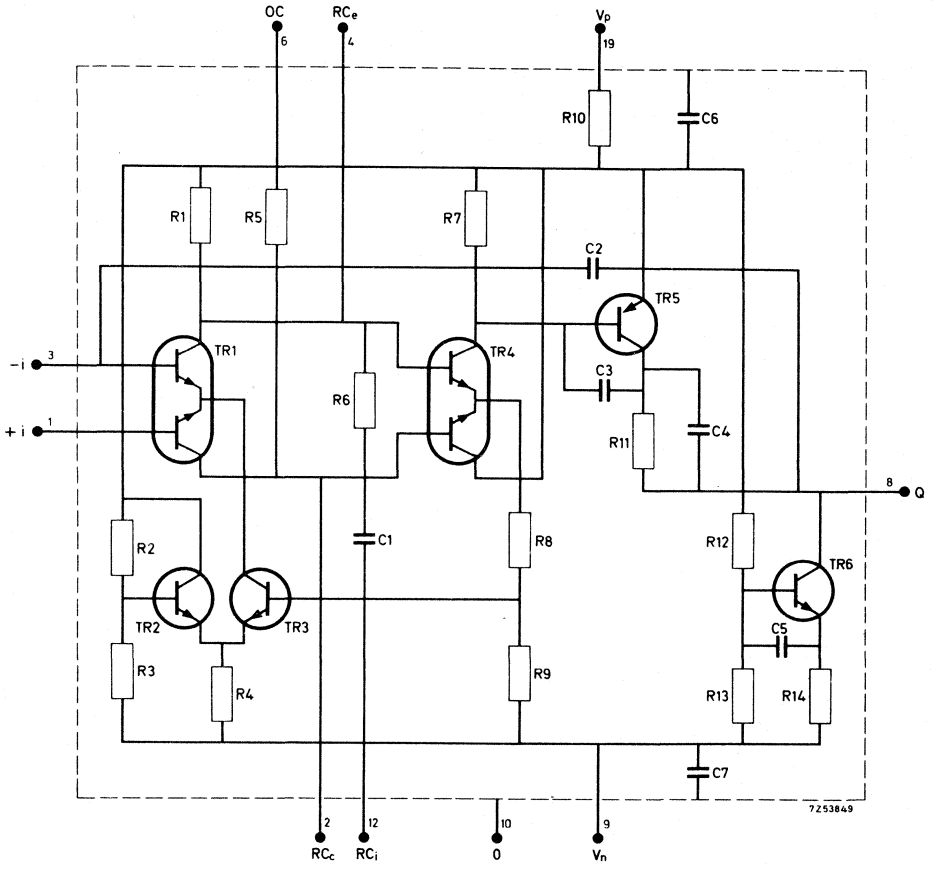


Fig.3. Circuit diagram

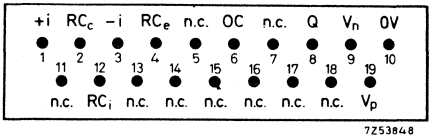


Fig.4. Terminal location

TECHNICAL PERFORMANCE

Ambient temperature range: operating	0 to +85 °C
storage	−40 to +85 °C
Max. case temperature	91 °C

Power supply

Supply voltages	V_P = +15 V ± 3% V_N = −15 V ± 3%
Supply currents	I_P = 10 mA + load current I_N = 10 mA + load current

Input data (ambient temperature +25 °C unless noted otherwise)

Open loop gain	minimum	typical
DC, max. load	25 000	60 000
DC, 100 kΩ load	100 000	150 000

Input voltage offset

Initial offset can be trimmed to zero by means of an external variable resistor of 15 kΩ between terminals OC and V_P

	maximum	typical
drift with temperature change (0 °C to +85 °C)	5 μV/deg C	3 μV/deg C
drift with supply voltage change		
for +15 V supply	7 μV/%	3 μV/%
for −15 V supply	3 μV/%	2 μV/%

Input current	maximum	typical
Each input: bias current	700 nA	300 nA
drift with temperature change (0 °C to +85 °C)	7 nA/deg C	3 nA/deg C
Differential: initial offset	35 nA	6 nA
drift with temperature change (0 °C to +85 °C)	1 nA/deg C	0.3 nA/deg C

Input impedance	minimum	typical
between inputs	75 kΩ	200 kΩ
common mode	60 MΩ	100 MΩ

Input voltage

max. voltage between inputs	+5 and −5 V
max. common mode voltage	+10 and −10 V
common mode rejection	min. 20 000 typ. 60 000
Voltage noise (16 Hz - 16 kHz)	3 μV (rms)

Output data

Output voltage (at a load current of 6 mA)	min. +10 V to −10 V	
Load resistance	min. 1.67 kΩ	
Output resistance	< 5 kΩ	

Frequency response

Unity gain bandwidth (small signal)	min. 8.5 MHz	typ. 9.5 MHz
Full output response (20 V_{p-p})		
with 10 kΩ load	min. 40 kHz	typ. 60 kHz
with 1.67 kΩ load	min. 33 kHz	typ. 50 kHz
Slewing rate (R_{load} = 10 kΩ)	min. 2.5 V/μs	typ. 3.7 V/μs

Specifications for the DOA40 used with 12 V supply

If the DOA40 is used with 12 V supply, the specifications remain the same as those given for the 15 V supply, except those listed below.

Power supply voltages	V_P = +12 V ± 5% V_N = −12 V ± 5%
Power supply currents (load current and feedback current to be added)	I_P = 8 mA I_N = 8 mA
Input currents	multiply the data given for 15 V supply by 0.8
Common mode voltage	+8 V, −8 V
Output voltage at a load current of 5 mA	+9 V, −9 V
Load resistance	1.8 kΩ (min.)

APPLICATION INFORMATION

When used in a follower circuit, the DOA40 may exhibit instability. To avoid this, it is good practice to insert a 10 kΩ resistor between the signal source and the amplifier input.

The characteristics of the DOA40 are such that adaption circuitry is unnecessary for most applications. However, three special situations which are sometimes encountered - comparatively small input currents, comparatively large output capability, and the need to adjust input current to zero - can also be handled by the DOA40 with the simple adaption circuits described below.

Reduction of input current and increase of input impedance

The dual transistor BCY87 connected as an emitter-follower in the circuit of Fig.5 can be used to reduce the input current to 40 nA per input and increase the input impedance to 15 MΩ between inputs (typical values).

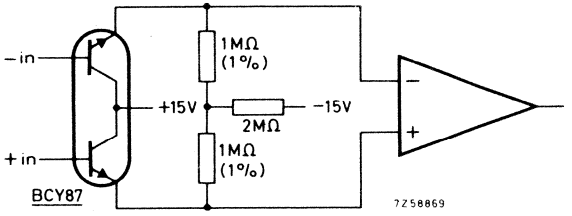


Fig.5. Configuration giving reduced input current and increased input impedance. The component values given are typical.

The characteristics of the circuit are given below. Other characteristics not listed are those of the DOA40 unit alone.

Supply voltage rejection (both supplies)	typical	80 μV/V
Input voltage, drift with temperature change	typical	5 μV/deg C
	maximum	10 μV/deg C
Input current / each input		
bias current	typical	40 nA
	maximum	60 nA
drift with temperature change / differential	typical	0.25 nA/deg C
initial offset	typical	4 nA
	maximum	6 nA
drift with temperature change	typical	0.1 nA/deg C
Input impedance between inputs,	typical	15 MΩ
	minimum	10 MΩ
common mode	typical	600 MΩ
Common mode rejection	typical	10 000
Unity gain bandwidth	typical	6.5 MHz
Full output frequency (20 V_{p-p})	typical	40 kHz

Increase of the output capability

The circuit of Fig.6 is capable of delivering 50 mA at +10 V and −10 V. The output can be short-circuited momentarily without causing damage to the circuit. Feedback networks if used should be connected to the circuit output, not the DOA40 output.

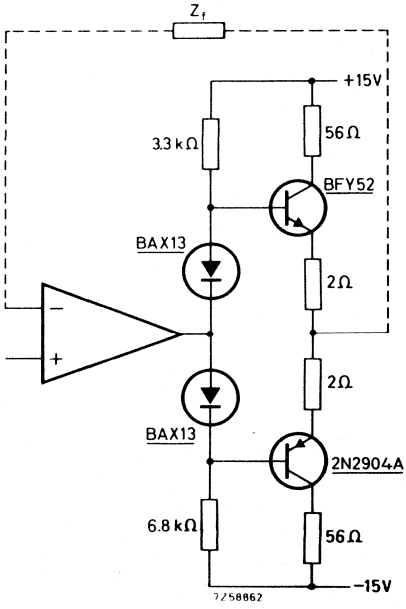


Fig.6. Configuration giving increased output capability.

Zero adjustment of input current

Each DOA40 input requires a bias current of 700 nA to give zero output voltage. By supplying this bias current from an external source, the DOA40 output can be made zero for a driving signal current equal to zero.

In Fig.7a the negative input (pin 3) is to be so adjusted. A 10 MΩ resistor should be connected between the output and pin 3, and the potentiometer adjusted so that the output voltage of the DOA40 becomes equal to zero. The 10 MΩ resistor should then be removed.

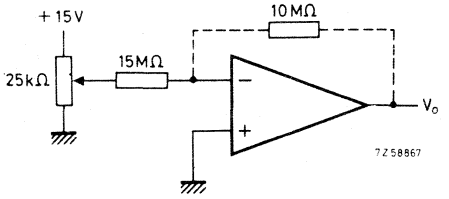


Fig.7a. External supply of bias current: adjustment of negative input.

The positive input (pin 1) may now be adjusted with the circuit of Fig.7b. Connect pin 3 to the DOA40 output, and the 10 MΩ resistor between pin 1 and ground. The potentiometer can now be adjusted so that the DOA40 output becomes zero. Disconnect the 10 MΩ resistor.

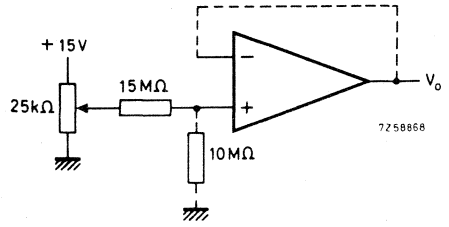


Fig.7b. External supply of bias current: adjustment of positive input.

Several publications are available which may be of further interest.

1. "Operational Amplifiers", Application Information.
   This publication gives an introduction to the use of operational amplifiers as engineering tools. The concepts and terminology of the general operational amplifier, and the properties and accuracy of a typical circuit are presented.
2. "Digital to Analogue and Analogue to Digital Conversion", Application Information.
   The publication gives detailed information on the construction of both types of converter.
3. "Flux Meter with Digital Read-out", Application Note (Print No. 9399 210 00601).
4. "Simple Process Control", Application Note (Print No. 9399 214 05501).
5. "Electronic Potentiometer", Application Note (Print No. 9399 260 00201).
6. "A level Detector Using the Operational Amplifier DOA40", Application Note (Print No. 9399 260 03101).

The Application Notes (3, 4, 5 and 6) give brief descriptions of practical applications of the DOA40.
Small discrepancies may be seen to exist in terminal location drawings in the above publications. The terminal locations as given in this Data Sheet are the ones to be followed.

DIFFERENTIAL ZERO DETECTOR

GENERAL

This unit can be used as a zero detector, voltage comparator, polarity detector, adjustable discriminator or differential amplifier.
Its feature of offering compatible signals for digital systems (e.g. composed of circuit blocks of the 10- Series) makes this unit a natural interface in hybrid systems.
The DZD 40 has been used succesfully in a wide range of instruments and control systems:

- digital to analogue and analogue to digital converters
- flux meter with digital read out
- automatic pH control system
- electronic potentiometer
- voice or no-voice detector
- automatic frequency characteristic testing
- over and under voltage detection
- over-dissipation switch in transmitter power stage
- servo control
- gas leak detector.

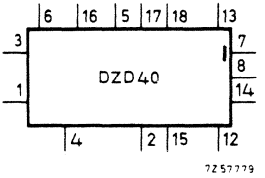
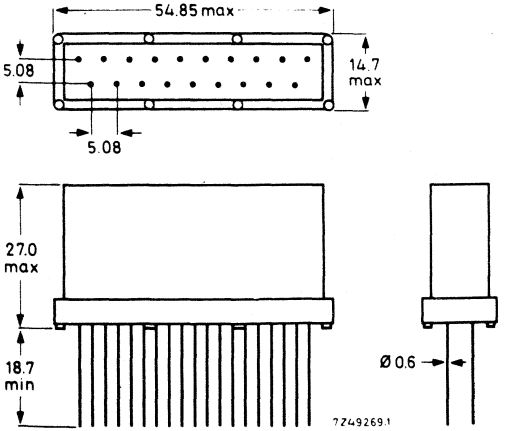


Fig.1 Drawing symbol

Dimensions in mm



The complete circuit is potted inside a metal can with 19 wire terminals.
The can is internally connected to the 0V supply (terminal 10).

Fig.2

Ambient temperature range

operating	0 to 70 °C
storage	−40 to +85 °C

Power supply

Supply voltages

V_P= + 12V ± 5%, V_N= - 12V ± 5%
or V_P= + 15V ± 1%, V_N= - 15V ± 1%
($V_V = V_B = V_{P'}$ = approx. V_P)

Nominal consumed current at nominal values of V_P and V_N

I_P = 6 mA, I_N = 8.3 mA

CIRCUIT DESCRIPTION

The differential zero detector comprises a two stage d.c. - coupled differential amplifier followed by an OR-gate and an inverting amplifier.
A voltage difference between the input terminals W_1 and W_2 is amplified about 1000 x by the two stage complementary differential amplifier (TR_1, TR_2, TR_3, TR_4). This amplified voltage difference is applied to the bases of TR_6 and TR_7.
As long as $|V_{A1} - V_{A2}|$ is less than a certain voltage, TR_5 is conducting.
If this voltage is exceeded TR_6 or TR_7 becomes conducting, the base current of TR_5 (via R_{10}) diminishes, the voltage across R_{14} goes up and TR_5 is cut off. So if the input voltage difference between W_1 and W_2 has a certain value either TR_6 or TR_7 are conducting (depending upon the polarity of $|V_{W_1} - V_{W_2}|$) and TR_5 is not conducting. From this it can be seen that V_{Q_1} and V_{Q_2} are in phase opposition with regards to V_{W_1} and V_{W_2}.

Truth table

inputs		outputs		
W_1	W_2	Q_1	Q_2	Q_3
high	high	high	high	low
high	low	low	high	high
low	low	high	high	low
low	high	high	low	high

High-high and low-low in the input rows indicate that signals applied to the inputs differ less than the trip value.

High-low and low-high in the input rows indicate that the voltage difference applied to the input exceeds the trip value.

In the output columns, high stands for +12 V and low for 0 V approximately.

It will be noticed that only one output terminal will be low for any input combination.

Current mode switching (no bottoming of transistors) is used to obtain high switching speeds and to reduce loading of the amplifier.
For this reason the terminals Q_1 and Q_2 should be connected to terminal 0 V if not used and they should be clamped with diodes (as for TR_5) if they are used.

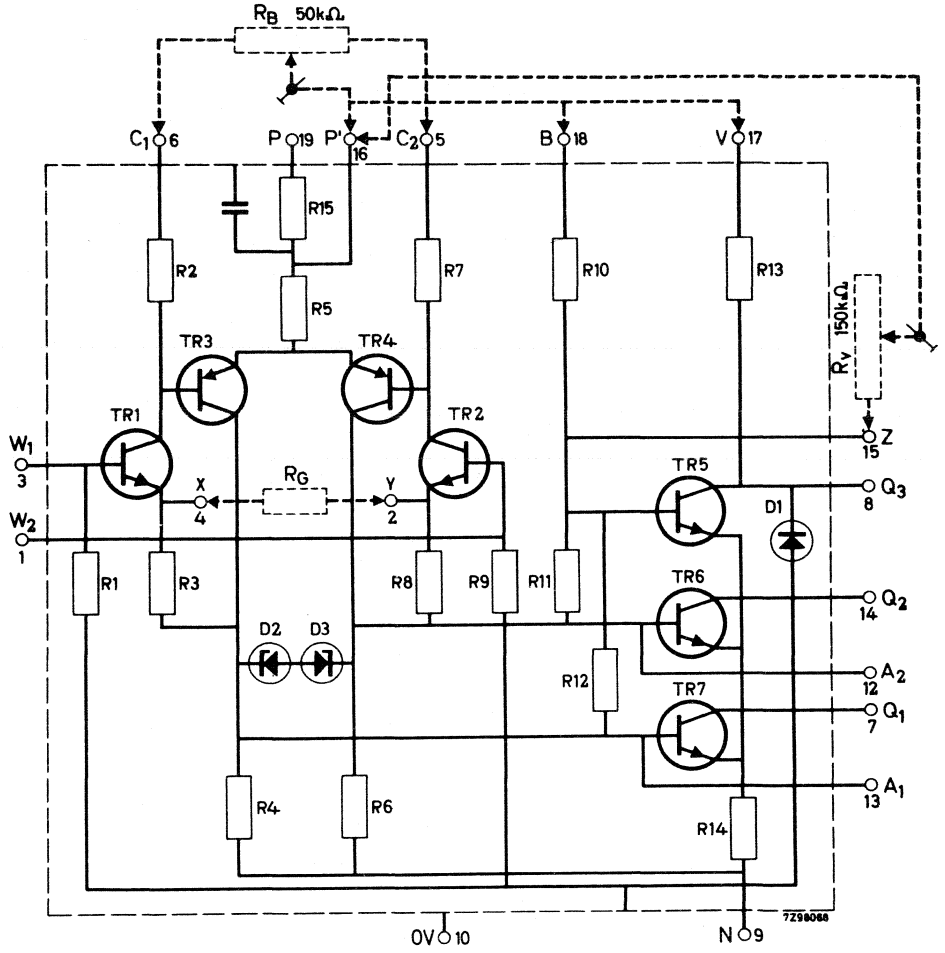


Fig.3. Circuit diagram

Terminal P' should be connected to terminal B for fixed bias or to variable resistor R_V for fine-gain adjustment.

Avoid a shortcircuit between terminals Q_3 and N, as this will damage diode D_1.

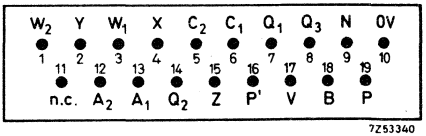


Fig.4. Terminal location

Oscillograms of some voltages with an input voltage of 8 mV_{p-p}, 100 kHz, are shown in the figures below.

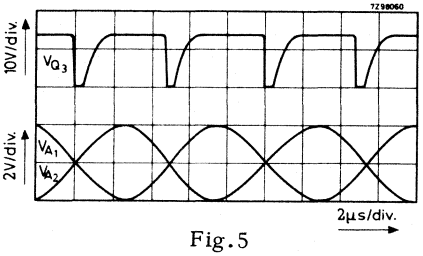


Fig.5

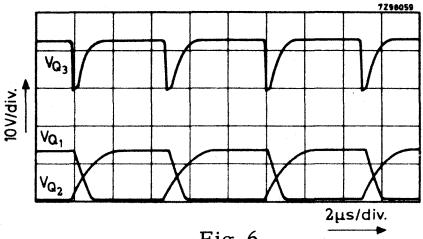


Fig.6

INPUT DATA

Differential off-set voltage after balancing (see "Initial adjustments")	0.1 mV
Voltage drift as a result of a change in temperature, measured at a source impedance of 10 kΩ	
typical value	3 µV / deg C
maximum value	5 µV / deg C
Differential sensitivity ($\lvert V_{W_1} - V_{W_2} \rvert$)	adjustable by means of gain control resistor R_G between X and Y; see graphs below

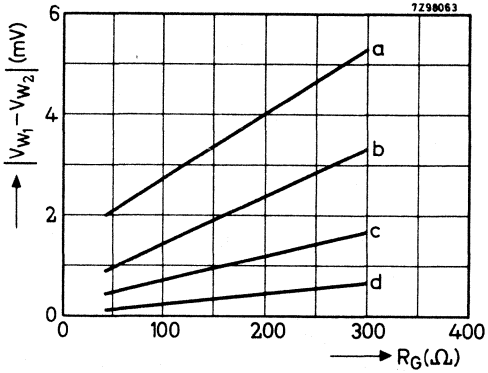
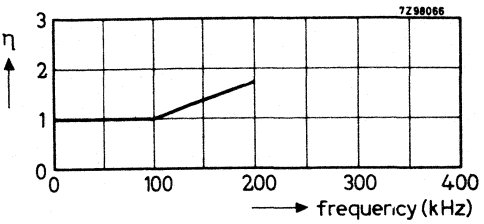


Fig. 7

The curves a and d are worst case limits at T_{amb} = 0 °C.
Curve a applies to the minimum input signal at which TR_5 or TR_6 is conducting (V_{Q_1} or V_{Q_2} is low) and TR_7 is not conducting (V_{Q_3} is high).
Curve d applies to the maximum input signal at which TR_5 or TR_6 is not conducting (V_{Q_1} and V_{Q_2} are high) and TR_7 is conducting (V_{Q_3} is low).
The curves b and c give typical values at T_{amb} = 25 °C.
Curve b : as a.
Curve c : as d.

η = input requirement factor for frequencies over 100 kHz (1.8 at 200 kHz, 1 up to 100 kHz)

Fig.8



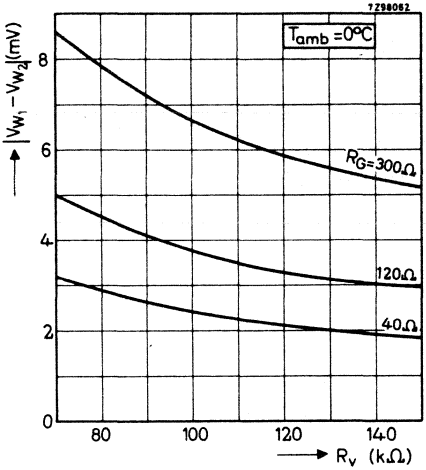


Fig. 9

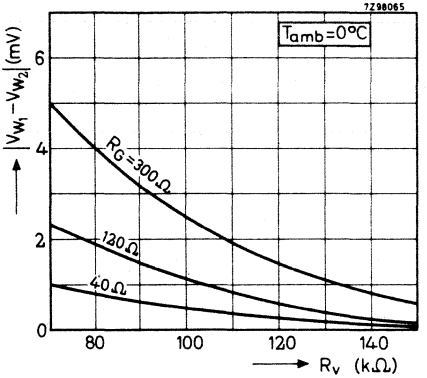


Fig. 10

The curves apply to the minimum input signal at which TR_5 or TR_6 is conducting (V_{Q1} or V_{Q2} is low) and TR_7 is not conducting (V_{Q3} is high).

The curves apply to the maximum input signal at which TR_5 and TR_6 are not conducting (V_{Q1} and V_{Q2} are high) and TR_7 is conducting (V_{Q3} is low).

Maximum value of $\lvert V_{W_1} - V_{W_2} \rvert$ to avoid extra delays	700 mV
Maximum voltage between input terminals	5 V
Frequency range	0-200 kHz. From 100 to 200 kHz the differential sensitivity reduces; the input voltage must be multiplied by the factor η (see Fig.8)
Maximum common mode voltage	$\pm$ 2V
Common mode rejection $\lvert V_{A1} - V_{A2} \rvert$ (typical value)	80 dB
Differential off-set current	< 30 nA
Current drift as a result of a change in temperature (typical value)	1 nA / deg C

Differential input resistance (R_i)	see Figs.11 and 12
Common mode impedance (typical value)	1.2 MΩ

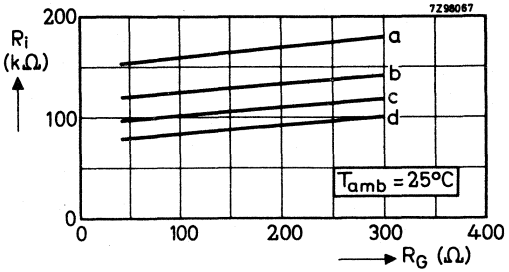


Fig.11

Curve a : typical differential input resistance
Curve b : typical input resistance between each input and 0 V
Curve c : minimum differential input resistance
Curve d : minimum input resistance between each input and 0 V

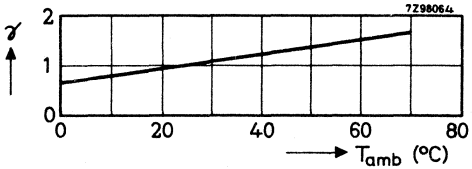


Fig.12. $\gamma = \frac{R_i \text{ at } T_{amb}}{R_i \text{ at } T_{amb} = 25\ ^oC}$

OUTPUT DATA

Outputs A_1 and A_2

Voltage gain	see Fig. 13
Maximum undistorted voltage $V_{A_1} = -V_{A_2}$	1 V
Band width at 3 dB	0 - 150 kHz
Minimum load resistance	100 kΩ

Outputs Q_1 and Q_2 *)

Maximum current at $V_Q > 0V$ **)	3.5 mA
Load resistance	3.6 kΩ

Output Q_3

	V and P' interconnected	V and P' not interconnected
Maximum current	2.5 mA	3.5 mA
Load resistance	5 kΩ	3.6 kΩ

*) If the outputs Q_1 and Q_2 are not used these terminals should be connected to terminal 0 V.

**) Clamp diodes (e.g.BAX13, BAY38, 1N4009) must be externally connected to Q_1 and Q_2.

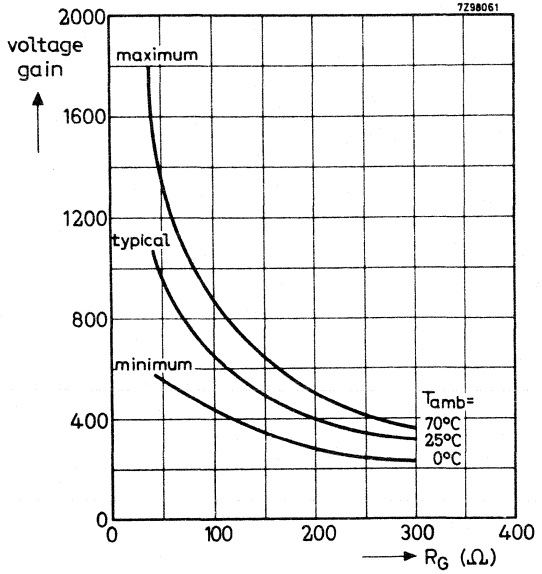


Fig.13

APPLICATION INFORMATION

Application hints

1. Avoid a shortcircuit between the terminals Q_3 and N as diode D_1 (see diagram) will be damaged.
2. In order to avoid instabilities due to transient switching voltages arising on supply lead inductance, the supply terminals N and P should be decoupled directly to terminal 0 V by means of low inductance capacitors.
3. For slowly diminishing voltages below the trip level the dv/dt of the zero going output at Q_3 will be approximately 10000 times as that of the input signal. In case a faster dv/dt is required, the voltage at Q_3 should be applied to a pulse shaper (e.g. PS10, PS20).
4. The terminals Q_1 and Q_2 provide signals that can in most cases directly be used to trigger units of the 10- and 20- Series or logic circuits having similar input requirements.
5. In circuits where high voltages might be detrimental, it is good practice to protect the inputs by an antiparallel diode circuit, thereby limiting the voltage.
6. If possible, arrange the circuit so as to avoid common mode voltage presence on inputs.
7. With a.c. input signals of over 10 kHz a capacitor of 2200 pF should be connected to the terminals Z and 0 V. Then only d.c. common mode voltage is allowed.
8. If terminal V is left unconnected the resistance load on Q_3 can be 3.6 kΩ.

Initial adjustments

Minimum off-set voltage

Connect a trimming potentiometer (R_B, see diagram) of 50 kΩ to the terminals C1 and C_2, slider to terminal P'. Place the slider in the centre position.
Short circuit the input terminals W_1 and W_2.
Connect a resistor to the terminals X and Y to obtain the desired gain (see "Sensitivity", next section).
Connect a d.c. millivoltmeter with high input impedance or an oscilloscope to the terminals A_1 and A_2; the meter or the oscilloscope must be floating.
Apply the supply voltages; allow a few minutes for block temperature distribution to reach a stable value of reading of the amplified off-set voltage on the millivoltmeter.
Correct the off-set voltage by turning the slider of the trimming potentiometer in such a way that minimum reading on the meter or the oscilloscope is obtained. When reading comes below 20% of full-scale value, switch to higher meter sensitivity. A correct adjustment will show a final value of a few millivolts, depending upon the actual gain.
Observe the voltmeter or oscilloscope for some time after balancing has been obtained; the reading should be stable.
Remove the shortcircuit of the input terminals and remove the voltmeter or the oscilloscope. Leave the slider of the potentiometer in optimum position.

Notes - In case no particular requirement for balance is to be met, the trimming potentiometer can be replaced by resistors having the value found during the balance procedure.

Un-balance will give unequal output wave shapes on Q_1 and Q_2 as well as an alternation of two forms on Q_3 with a sinusoidal input voltage.

Sensitivity

Coarse adjustment can be done by connecting a resistor (R_G, see diagram) to the terminals X and Y; if a trimming potentiometer of 500 Ω is used for this purpose the gain can be set over a wide range. The terminals P' and B must be interconnected. For the correct value of R_G, see Fig. 7. After the resistor between the terminals X and Y has been adjusted, fine adjustment can be done by disconnecting terminal P' from terminal B and by connecting a variable resistor (R_V) of 150 kΩ to the terminals Z and P' (without influencing the input impedance).

APPLICATION SUGGESTIONS

Low voltage zero detector giving zero output at zero input

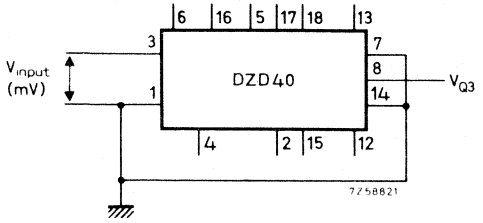


Fig.14

$V_{input} \ll 5\ V_{p-p}$ or $5\ V_{dc}$
$V_{Q3} = +V_{supply}$ as long as V_{input} is higher than the trip level.
$V_{Q3} = 0$ V as V_{input} has reached the trip level.
If V_{input} is an a.c. signal V_{Q3} will be high apart from the zero crossing points i.e. the unit acts as a bidirectional pulse shaper, see Fig.15.

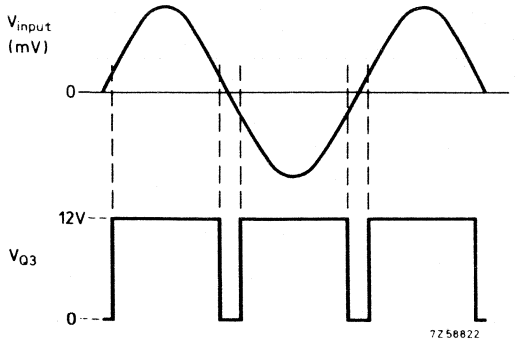


Fig.15

High voltage zero detector giving zero output at zero input

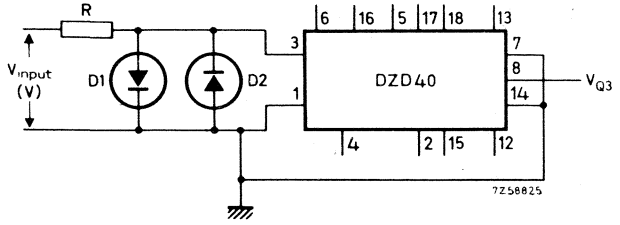


Fig.16

$V_{Q3} = +V_{supply}$ as long as V_{input} is higher than the trip level. $V_{Q3} = 0$ V as V_{input} has reached the trip level. If V_{input} is an a.c. signal V_{Q3} will be high apart from the zero crossing points i.e. the unit acts as a bi-directional pulse shaper (see Fig.15). D_1 and D_2 limit the input voltage. R serves to stay safely within diode current limits and loading of signal source possibilities.
If input frequency exceeds 10 kHz a capacitor of 2200 pF should be connected to the terminals Z and P' (see Figs.3 and 4).

Low voltage zero detector giving complementary outputs

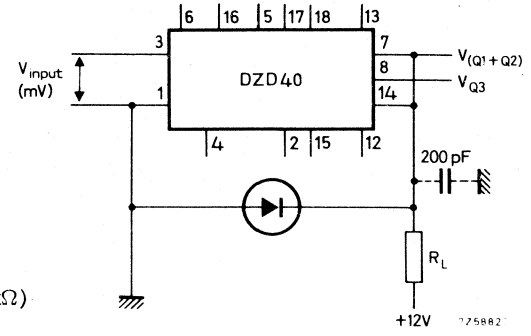


Fig. 17
(R_L = min. 3.6 kΩ)

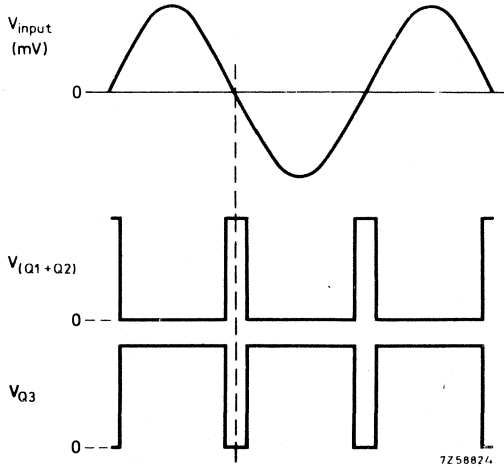


Fig. 18

V_{Q3} may be obtained as well with this circuit, but then it is advisable to give Q_1 and Q_2 a capacitive load of 200 pF or more.

High voltage zero detector giving complementary outputs

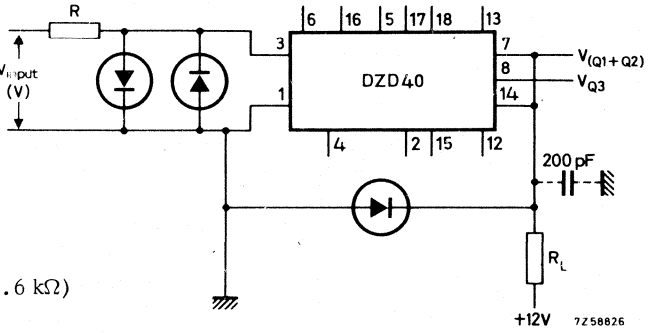


Fig. 19
(R_L = min. 3.6 kΩ)

Low voltage comparator giving zero output at zero difference input

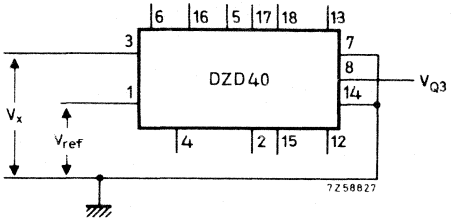


Fig. 20

V_X and $V_{ref} < 1$ V
$V_{Q_3} \approx 0$ V, if $|V_X - V_{ref}| <$ trip level

Low voltage comparator giving high output at zero difference input

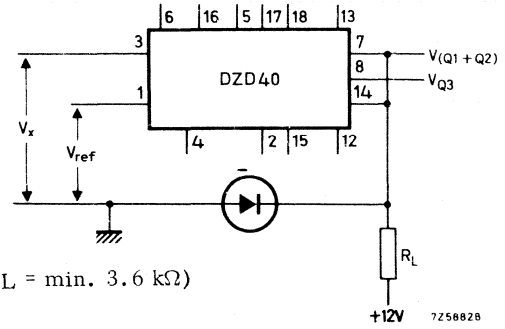


Fig. 21. (R_L = min. 3.6 kΩ)

$V_{(Q_1 + Q_2)}$ = high if $|V_X - V_{ref}| = 0$ V.

High voltage comparator for d.c. voltages

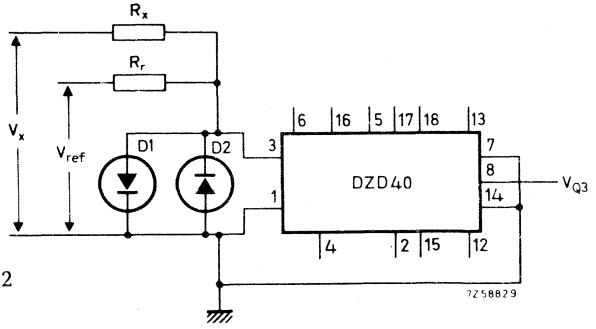


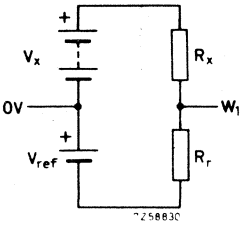
Fig. 22

The outputs can also be arranged as in Fig. 21.

This circuit avoids common mode difficulties. The clamping diodes D_1 and D_2 are to be used if the voltage between 3 and 1 could possibly exceed 5 V.

Note - V_{ref} and V_x are to be operating in series (i.e. not opposition).

Calculation of R_x and R_r.



The voltage between the terminals 0V and W_1 will be zero if

$$\frac{V_x}{V_{ref}} = \frac{R_x}{R_r}$$

R_x and R_r can be selected taking into account the loading of the sources V_r and V_x.

Fig. 23

Example - V_x is a potential between + 60 and + 95V with respect to the 0V line. V_r is a properly connected reference source of 5 V. Both sources can be loaded with 1mA max.

It is desired to produce a positive output signal whenever V_x = 80 V. As $V_x$max = 95V, the total voltage across $R_x + R_r$ is max. 100V. To stay within loading $R_x + R_r$ must be approx. 100 kΩ.

Furthermore $\frac{R_x}{R_r} = \frac{80}{5}$ for zero detection at 80 V, so $R_x = 16\ R_r$.

When R_r = 6.8 kΩ a trimming potentiometer of 150 kΩ can be used for R_x. The output can be taken from $(Q_1 + Q_2)$ as in Fig. 21.

Polarity detector

Use is made of the terminals Q_1 and Q_2, if desired terminal Q_3 can be used to indicate zero difference input.

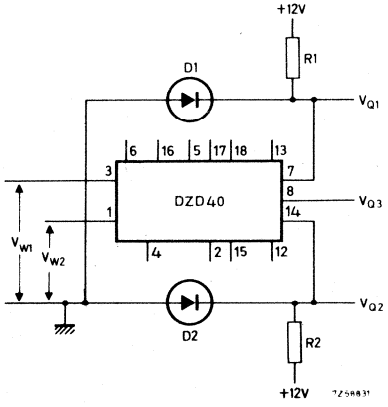


Fig. 24

V_{Q_1} is low, if W_1 (terminal 3) is high.
V_{Q_2} is low, if W_2 (terminal 1) is high.

Clamping diodes across the inputs can be omitted if the input voltages are $< 1\ V_p$.

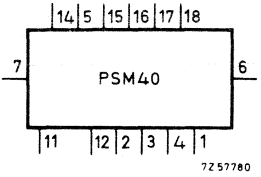
This circuit is extremely useful in servo control, direction determination and tolerance automation.

To avoid common mode influence V_{W_1} and V_{W_2} should be made lower than 2V (resistive step down).

PHASE SHIFT MODULE

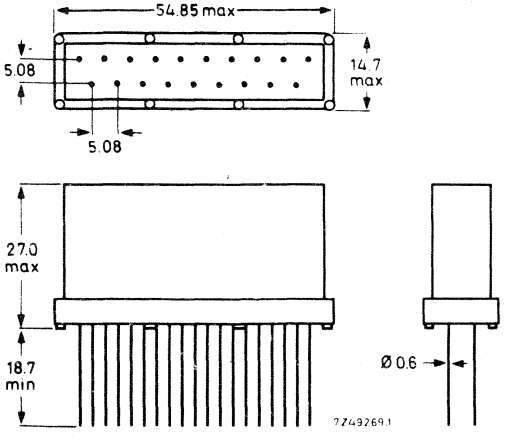
GENERAL

This phase shift module is designed for use in conjunction with a trigger source for the control of the conduction angle of thyristors.
It can be used in single-phase, half- or full-wave applications for control of thyristors operating with an a.c. supply of 15 to 10 000 Hz. The control range is better than 10 to 170°. Three PSM's can be synchronised for 3-phase full-wave control.
An important feature is that one can make a choice between two operation modes, i.e. either linear control of conduction angle by means of a control voltage or linear control of the average voltage across the thyristor load (cosinusoidal control). In the latter case the average thyristor load voltage can be made independent of the a.c. supply voltage (see "CONTROL FACILITIES").



Drawing symbol

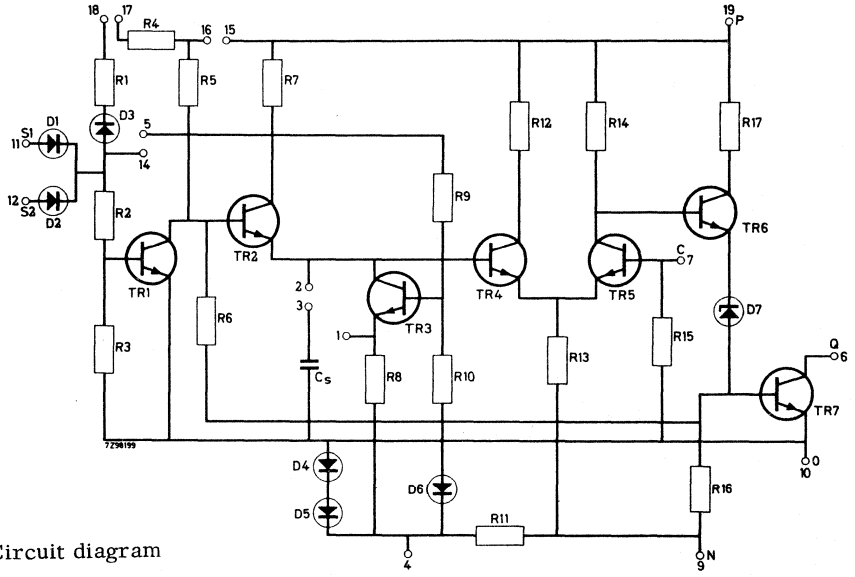
Dimensions in mm



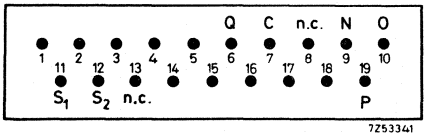
The complete circuit is potted inside a metal can with 19 wire terminals.

CIRCUIT DESCRIPTION

For operation on 50 Hz, terminals 2 and 3 have to be interconnected. Transistor TR_1 is conducting during most of the period that the synchronization voltages are present on S1 and S2. Thereby the collector of TR_1 will be at a low voltage, therefore TR_2 will be non conducting during the time that TR_1 conducts. As soon as the value of the synchronization voltage becomes lower than the diode forward voltage drop (around the zero crossing of the synchronization signal) TR_1 ceases to conduct, TR_2 rapidly charges C_S. A few electrical degrees after synchronization zero TR_1 becomes conducting again, TR_2 cuts off.
TR_3 discharges C_S during the half cycle to zero volts. TR_4 and TR_5 constitute a long tailed pair comparator. As long as the voltage to the base of TR_4 exceeds that applied to TR_5, TR_4 is conducting and TR_5 is off. Consequently base current will flow to TR_6 through R_{14} and TR_6 will conduct. The emitter current of TR_6 drives TR_7 into saturation so that the output Q will be at a low potential for the time that the voltage on point 2 is higher than that applied to the control input terminal C.
The discharge of C_S as a function of time can be made linear by means of TR_3 acting as a constant current discharger or cosinusoidal discharger by using different circuit connections.



Circuit diagram



Terminal location

TECHNICAL PERFORMANCE

Operating temperature range	−25 to +85 °C
Storage temperature range	−40 to +85 °C

Power supply

Supply voltage	V_p = + 12 V ± 5%, V_N = −12 V ± 5% or V_p = + 12 V + 10%, V_N = −12 V + 10% or V_p = + 12 V − 10%, V_N = −12 V − 10%
Consumed current	$I_p = I_N$ = approximately 10 mA (excluding load current)

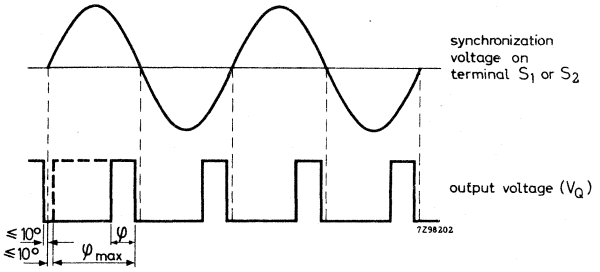
Note - As the output voltage V_Q is dependent upon switch on sequenee and rise time of the supply voltages, it is recommended to short circuit terminal Q temporarily to terminal 0 when switching on.

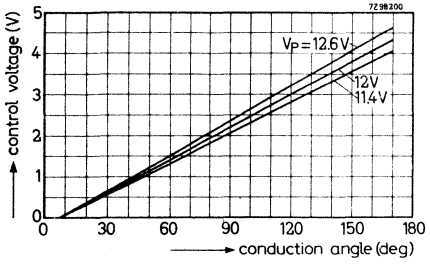
Input data

Control voltage (V_C)	
absolute maximum	5 V
absolute minimum	0 V
Control current (I_C)	0.5 to 0.33 mA
Maximum wiring capacitance at the control input (terminal C)	200 pF

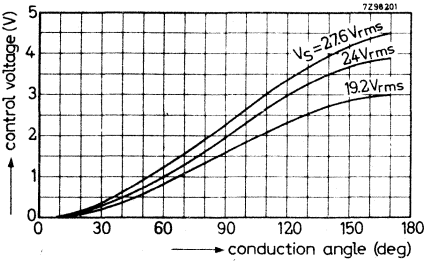
Output data

Output voltage (V_Q)	
high level (TR_7 non conducting)	max. 15 V
low level (TR_7 conducting)	max. 0.5 V min. 0 V
Output current (I_Q)	max. 25 mA at V_Q = max. 0.5 V (T_{amb} = −25 °C)
Minimum control range of conduction angle (φ)	10 − 170°





Linear control



Cosinusoidal control

Synchronization

Synchronization voltage (V_S)	24 V_{rms}, + 15%, -20%
Nominal synchronization current (I_S)	
at linear control	approx. 4 mA
at cosinusoidal control	approx. 8 mA

The synchronization voltage can be supplied by a transformer with or without a center tap and preferably provided with an electrostatic screen between the primary and the synchronization winding to avoid capacitive zero shift.
When a transformer with a center tap is used the outputs of the transformer have to be connected to the terminals S_1 and S_2, whereas the center tap is connected to terminal 0.
When a transformer without a center tap is used the outputs of the transformer have to be connected to the terminals S_1 and S_2. Furthermore two diodes OA200 or an equivalent type, have to be connected with the cathode to the terminals S_1 and S_2, whereas the anodes of these diodes have to be connected to terminal 0.

Synchronization frequency range 15 to 10 000 Hz

When the terminals 2 and 3 are interconnected the unit can be used at a synchronization frequency of 50 Hz.
For frequencies higher or lower than 50 Hz the terminals 2 and 3 have to be left disconnected and an external capacitor has to be connected between the terminals 2 and 10.
Capacitance as a function of the frequency: $C = \frac{11}{f}\ \mu F$

CONTROL FACILITIES

Linear conduction angle control

The conduction angle is proportional to the control voltage. The terminals 5, 15 and 16 have to be interconnected. The terminals 15 and 16 can also be interconnected by means of an adjustable resistor, in case of multi-phase operation.
The conduction angle can be controlled by a voltage level on the control input (terminal C).
When the control voltage is derived by a potentiometer from the d.c. voltage which supplies the conduction angle determining part of the circuit (terminal 16) the variations of the conduction angle, caused by supply voltage variations, are greatly reduced.

Cosinusoidal control of the conduction angle

The course of the conduction angle (φ) as a function of the control voltage (V_c) is given in the formula:

$\varphi = \arccos (1 - aV_c)$, in which

$a = \text{approx.}\ \frac{11}{V_{s_{rms}}}$

At a constant value of the control voltage the variations of the average voltage across the thyristor load, caused by the mains voltage variations, can be greatly reduced as follows.
The conduction angle determining part of the circuit has to be supplied by a full-wave rectified voltage (proportional to the mains voltage) and by a smoothed voltage derived from the mentioned voltage.
Therefore the terminals 14 and 5 have to be interconnected and the terminals 17 and 18 have to be interconnected directly or by means of an adjustable resistor (multi-phase operation). Furthermore an electrolytic capacitor of 100 μF, 40 V has to be connected between terminals 18 and 10.

ADJUSTMENT

1. Single-phase operation

To obtain a conduction angle of 0^o at a control voltage of 0 V, a resistor has to be connected between terminals 1 and 4. For determining its value the following procedure has to be done.
Connect an adjustable resistor with a control range up to 47 kΩ between the terminals 1 and 4, a resistor of 1 kΩ between the terminals Q and P and a d.c. voltmeter between the terminals Q and 0. The control input terminal C has to be connected to terminal 0. Furthermore the necessary interconnections for linear or cosinusoidal control have to be made. Apply the synchronization and d.c. supply voltages.
The output voltage will be about 0 V when the adjustable resistor has its maximum value. This resistor has to be decreased until the moment the output voltage starts to increase. The conduction angle is now close to 0^o at a control voltage of 0 V.
The unit is ready for use after the resistor of 1 kΩ and the voltmeter are removed.

Note - After the resistance value has been determined the variable resistor may be replaced by a fixed resistor of the same value as the inherent stability is such that no readjustment will be required.
Typical value of the resistor for linear control: 10 kΩ, for cosinusoidal control: 33 kΩ.

2. Multi-phase operation

To obtain equal conduction angles of two or more PSM's at a common control voltage within the whole control range the following has to be done.

a. Linear control

Interconnect the terminals 5, 15 and 16. Apply the d.c. supply voltages; the synchronization voltage is not applied. Measure the voltage on terminal 2. This voltage should be equal for all PSM's. If there is a difference between the voltages on terminals 2 a resistor has to be inserted between the terminals 17 and 18 of the unit with the highest voltage on terminal 2. The value of this resistor is approximately 1 Ω per mV voltage difference. For further adjustment, see 2c.

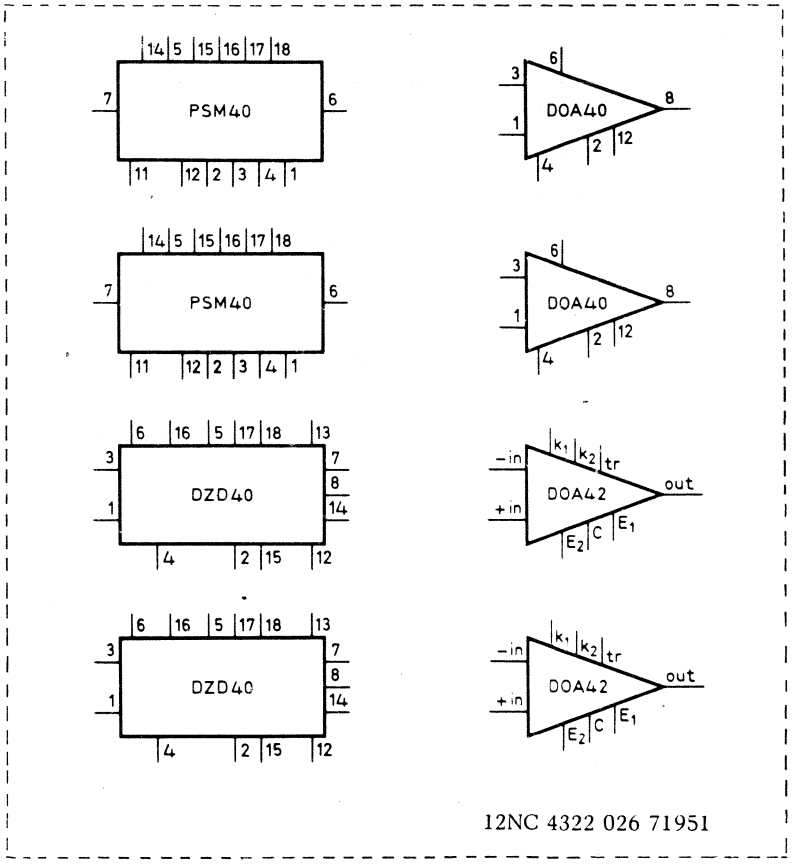
b. Cosinusoidal control

Connect terminal 5 to 15 and terminal 17 to 18. Apply the d.c. supply voltages to the terminals P and N and a d.c. voltage of 30 V to terminal 18; the synchronization voltage is not applied. The same measurements have to be done as for linear control.
If there is a difference between the voltages on terminal 2 of two PSM's a resistor has to be inserted between the terminals 17 and 18 of the unit with the highest voltage on terminal 2. The value of this resistor is approximately 3 Ω per mV voltage difference. For further adjustment, see 2c.

c. With the adjustments described in 2a and 2b the conduction angles of the units will be equal at high values of the control voltage (> 4 V). To obtain equal conduction angles at low values of the control voltage the following has to be done.
The units have to be connected for the desired mode of operation.
Adjust one unit so that a conduction angle of 0^{o} at a control voltage of 0 V is obtained (see 1).
Apply a control voltage of 1 V to all units. Connect a d.c. voltmeter between output Q of the unit which has been adjusted and output Q of the unit to be adjusted. These outputs have to be connected via a resistor of 1 kΩ to terminal P. Vary the value of the resistor between the terminals 1 and 4 of the unit to be adjusted, until minimum reading on the voltmeter has been obtained. Now the conduction angles of both units will be equal within the whole control range.

STICKERS

These are drawing symbols of 40-Series circuit blocks printed on self-adhesive, transparent material on which one can write. They can be used for fast preparation of system drawings.
The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71951.



Note:
This sheet will be re-drawn to exclude the DOA42 when present stocks run out.

CHOPPER-STABILIZED OPERATIONAL AMPLIFIER

QUICK REFERENCE DATA	
Open loop gain	min. 10^7
Initial offset voltage	max. ± 10 μV
Average offset voltage drift with temperature	max. 0,1 μV/degC
Bias current	max. ± 70 pA
Noise voltage (0,01 to 1 Hz), peak to peak	0,7 μV

APPLICATION

The component possesses a high current and voltage stability therefore small d.c. and low-frequency signals receive accurate amplified reproduction. Changes due to environmental conditions such as temperature time and power supply voltages have only a minor influence on the circuit performance. Initial offsets are very small, therefore initial adjustments and periodic calibration can be eliminated in many applications.

DESCRIPTION

To obtain a high d.c. stability, the d.c. and low-frequency signals are chopped, amplified (a.c. amplifier) and then demodulated. The higher frequency component of the signal at the common input is fed via a capacitor directly to the wide-band amplifier (see block diagram, Fig. 1). Offset and drift of the wide-band amplifier is reduced by a factor equal to the gain of the a.c. amplifier.

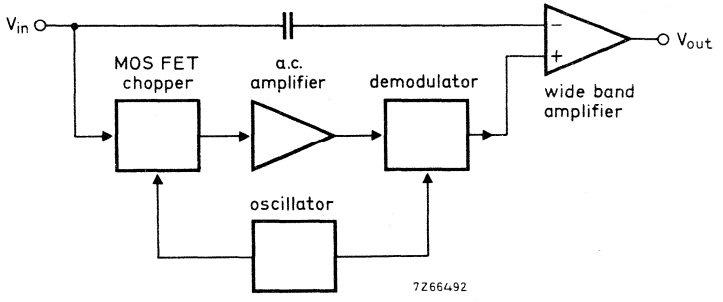


Fig. 1 Block diagram

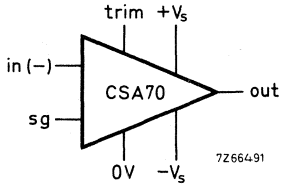


Fig. 2 Drawing symbol

sg = signal earth
in (-) = inverting input
out = output
$+V_S$ = positive supply voltage
$-V_S$ = negative supply voltage
0 V = common supply voltage
trim = offset voltage adjustment

MECHANICAL DATA

Dimensions (mm) and terminal location

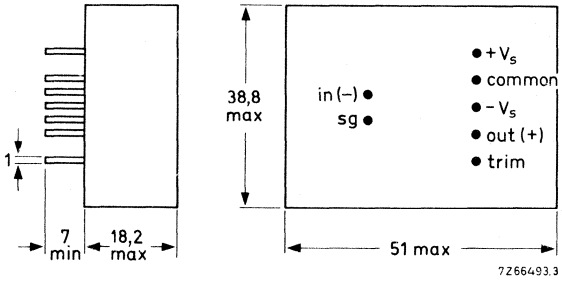


Fig. 3

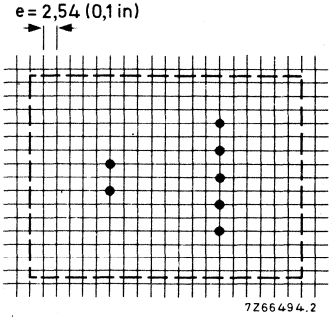


Fig. 4 Terminal location on 0, 1 inch grid.

ELECTRICAL DATA

Ambient temperature +25 °C, supply voltages +15/-15 V, unless stated otherwise.

Ambient temperature range	
Operating, rated specification	0 to +60 °C
Storage	-40 to +85 °C
Power supply	
Voltage, rated specification	± 15 V ± 3%
derated specification	± 12 V to ± 18 V
Typ. current at +15/−15 V	+7/-7 mA + load current
at +12/−12 V	+4/-5 mA + load current
Open loop gain (R_L = 2 kΩ)	min. 10^7
Frequency response	
Unity gain bandwidth (small signal)	min. 0,5 MHz (frequency roll-off 6 dB/oct.)
Full power frequency	min. 5 kHz
Slewing rate	min. 0,3 V/μs
Overload recovery time	typ. 3 s, max. 5 s

For method which will substantially reduce recovery time, see circuit of Fig. 5.

Input data

	typical	maximum
Initial offset voltage (adjustable to zero with 100 kΩ potentiom.*)		± 10 μV
Average offset voltage drift with temperature		0,1 μV/degC
Average offset voltage drift with supply voltage		0,1 μV/%
Average offset voltage drift with time	1 μV/month	
Bias current		± 70 pA
Average bias current drift with temperature		0,7 pA/degC
Average bias current drift with supply voltage	0,4 pA/%	
Average bias current drift with time	10 pA/month	

*) Potentiometer to be connected between $+V_S$ and $-V_S$, slider to "trim".

Input voltage range	± 20 V
Noise voltage	
0,01 Hz to 1 Hz, p-p	0,7 µV
0,01 Hz to 10 Hz, p-p	5 µV
10 Hz to 5 kHz, r.m.s.	2,5 µV
Noise current	
0,01 Hz to 1 Hz, p-p	5 pA
0,01 Hz to 10 Hz, p-p	40 pA
→ Burst noise (popcorn noise) peak voltage of CSA70L, measured across 100 kΩ	< 15 µV
Input impedance	min. 200 kΩ

Output data	typical	minimum
Output voltage, R_L = 10 kΩ	± 14 V	± 12 V
R_L = 2 kΩ	± 13 V	± 10 V
Output current	± 12 mA	
Output resistance (without feedback)		max. 200 Ω

Continuous short circuit is allowed between the output and earth, or between the output and supplies.

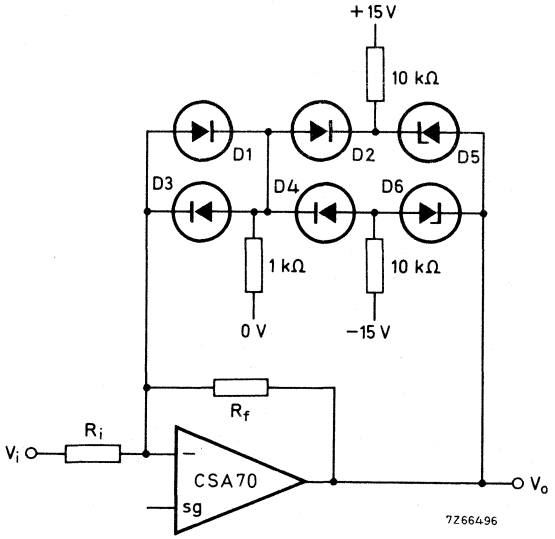


Fig. 5

D1 – D4 = BAW62

D5, D6 = BZX79/C10 or BZY88/C10

The resistors are carbon types, 1/8 W, 5%

APPLICATION INFORMATION

For extensive information on theoretical background and practical applications of operational amplifiers refer to our Application Book: "Measurement and Control using 40-series modules", order number 9399 263 05901.

1. Logarithmic amplifier (6 decade)

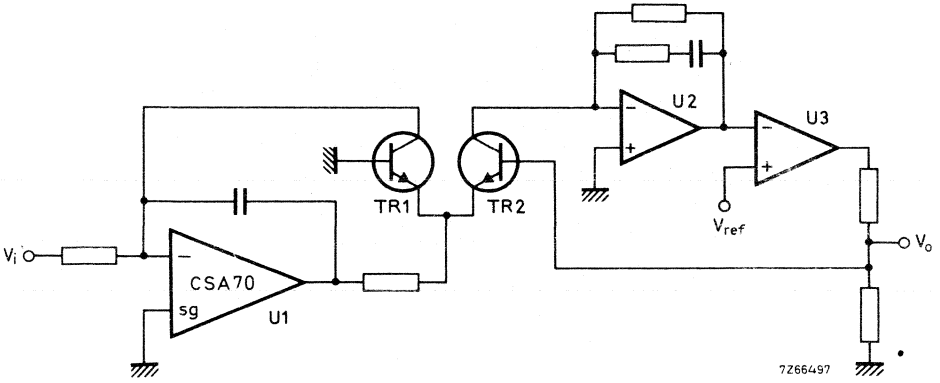


Fig. 6 V_i = 10 μV to 10 V.
TR1, TR2 = matched transistor pair, thermally coupled.
U2, U3 = general purpose amplifiers.

2. Inverting amplifier with very high input impedance

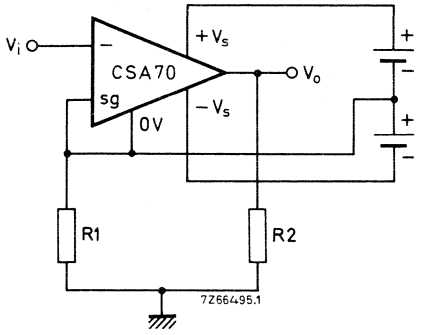


Fig. 7

$+V_S$ and $-V_S$ must be floating.

$$V_o = \frac{R2}{R1} V_i$$

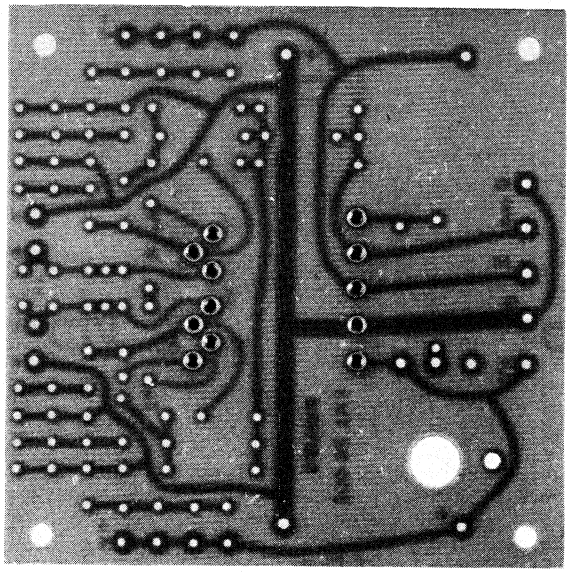
$Z_i > 100\ M\Omega$

(Note that input floats with respect to supplies, and that gain can be chosen less than unity.)

ACCESSORIES

1) A printed-wiring board (see photograph) providing plug-in facilities for the CSA 70 can be ordered separately under catalogue number 4332 000 00501.
This board will also accommodate a trimming potentiometer.

RZ 26423-5



2) Employing the AMP reusable component test receptacles type nr 380 598-2 enables the CSA 70 to be plugged into a printed-wiring board.

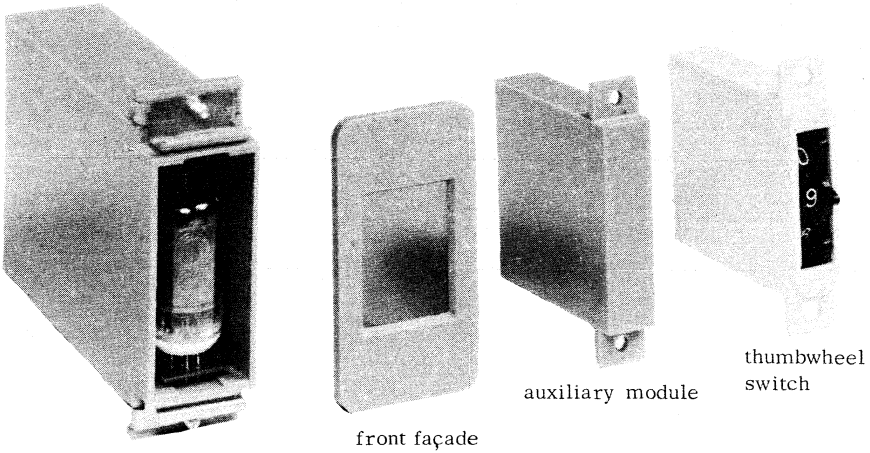
TEST SPECIFICATIONS

The unit has been designed to meet the tests of MIL-STD-202C below. Before and during manufacture samples of modules are regularly subjected to these tests.

1. Shock test according to method 202B; 3 blows 50 g in 3 perpendicular directions.
2. Vibration test according to method 204A; frequency 10-500 Hz 15 min, amplitude 0,75 mm max., 10 g max., 3 x 3 hours.
3. Temperature-cycling test according to method 102A; 5 cycles from −40 to + 85 °C.
4. Moisture resistance according to method 106C; R.H. 90 to 98%, temperature cycling +25 to +65 °C.
5. Solderability according to method 210.
6. Robustness of terminations according to method 211A and B.

Counter modules 50-Series

INTRODUCTION



indicator module

front façade

auxiliary module

thumbwheel switch

RZ 24173

The 50-Series contains uni-directional and bi-directional decade counters with direct display and a number of auxiliary modules offering a complete range of building modules for industrial automation and control.
The use of silicon semiconductors, including silicon-controlled switches (SCS), ensures reliable operation over a wide temperature range.
The simple rules regarding electrical interconnections, mounting accessories and interwiring of the compact self-contained cases, make the 50-Series ideal for immediate installation and assembly in a large variety of applications. Preset programmed control with the aid of compatible preset switches and input/output devices offer excellent possibilities for:

- industrial batch counting
- automatic winding machines
- sequential control and timing
- numerical control systems
- automatic weighing and dosing
- speed control, etc.

MODULES

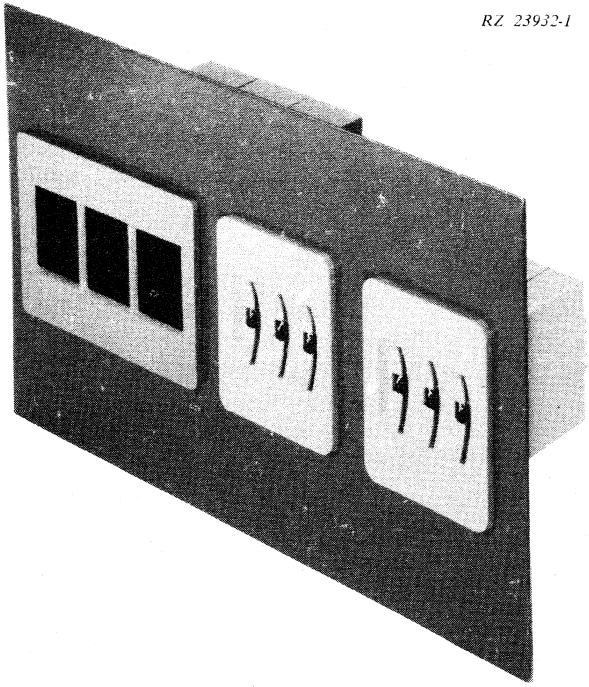
The 50-Series comprises the following modules:

type	description	catalogue number
NIC50	Uni-directional decade counter with decimal outputs and direct display. The use of silicon controlled switches allows for direct drive of the numerical indicator tube.	2722 007 03001
RIC50	Bi-directional decade counter with decimal outputs and direct display. The use of silicon controlled switches allows for direct drive of the numerical indicator tube.	2722 007 04001
MID50	Integral buffer memory with direct display. Accepts decimal information from NIC50 and RIC50.	2722 007 05001
SID50	+ and – sign indicator driver with direct display.	2722 007 06001
SU50	10 position thumbwheel switch for preset counting (type 10P1C).	4311 027 82321
3.NOR50	Buffer adaptation stage and double NOR for sequential and combinational logic operations. The latter can be cross connected to form a d.c. memory function.	2722 007 00001
4.NOR51	Quadruple NOR for sequential and/or combinational logic operations. Two d.c. memory functions can be made from the four NOR's.	2722 007 00011
PSR50	Pulse shaper combined with an automatic/manual reset unit.	2722 007 01001
LRD50	300 mA, 30 V output stage for lamp and relay drive.	2722 007 02001
PDU50A and PDU50B	Printer drive units	2722 007 08001 2722 007 08011

type	description	catalogue number
PSU50	Power supply unit Input: 110, 220, 230, 240 V_{ac} $\pm 10\%$, -15%; 45 to 65 Hz Output: a) 24 V_{dc}, $\pm 5\%$, 250 mA (logic supply) b) 250 V_{dc}, $\pm 18\%$ (supply for 12 indicator tubes).	2722 151 00061
DCD50	General purpose decade counter and divider	2722 007 07001
ECA50	Empty case assembly	2722 007 89001

For detailed electrical information on the above-mentioned modules, see the relevant data sheets; for data on the SU50, see the data sheets of thumbwheel switches 4311 027 82...
For detailed application information the Application Book "Design with 50-series modules", print number 9399 263 06001, should be consulted.

RZ 23932-1



MOUNTING ACCESSORIES

Front façades for indicator modules (NIC50, RIC50, MID50 and SID50)

Front façades are available for one up to and including six indicator modules. They are provided with a coloured polarised screen.

type	number of indicator modules	catalogue number
FIC 1	1	4322 026 70340
FIC 2	2	70350
FIC 3	3	70360
FIC 4	4	70370
FIC 5	5	70380
FIC 6	6	70390

Mounting façades for thumbwheel switches (SU50)

Mounting façades, giving facilities for mounting one up to and including six switches, are available.

type	number of switches	catalogue number
FMF 1	1	4311 027 80598
FMF 2	2	80608
FMF 3	3	80618
FMF 4	4	80628
FMF 5	5	80638
FMF 6	6	80648

Mounting aids for auxiliary modules (3.NOR50, 4.NOR51, PSR50, LRD50, PDU50A, PDU50B and DCD50)

Mounting bar, catalogue number 4322 026 70170
Self tapping screws (2 pieces), 4Nx$\frac{1}{4}$", catalogue number 2522 163 01005
Washer (M3), catalogue number 2522 600 16016

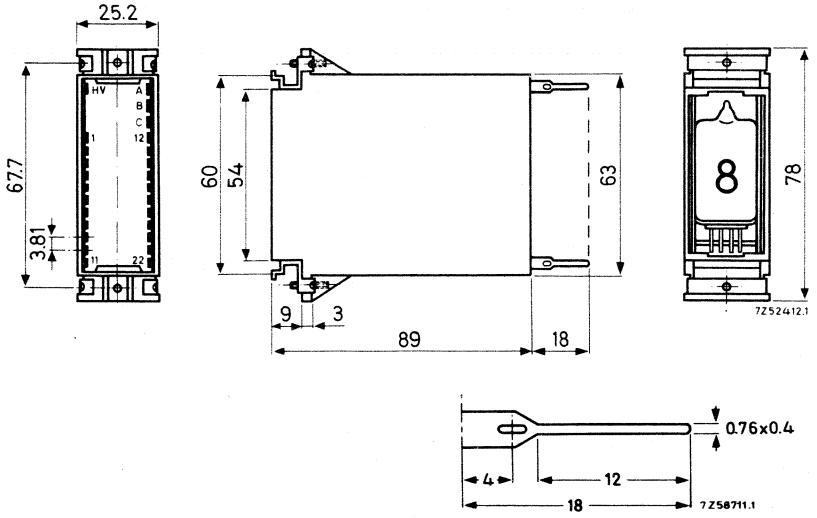
CONSTRUCTION

The various functions are housed in plastic cases, of which the dimensions and terminal locations are shown below.
Each module is provided with pins for soldering and wire-wrapping.

DIMENSIONS

The dimensions in the figures are given in mm; for inch values see the tables.

Indicator modules (NIC50, RIC50, MID50 and SID50)

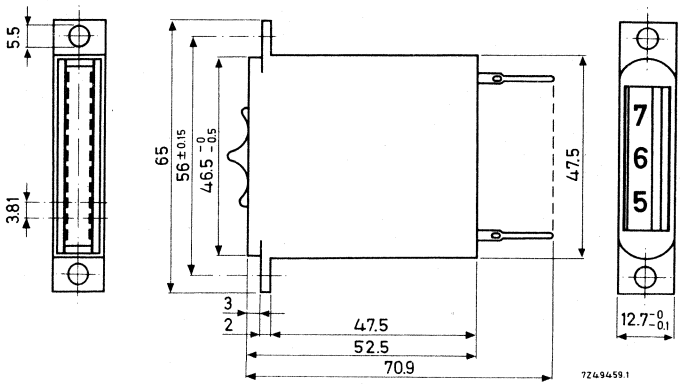


mm	inches
3	0.118
3.81	0.150
4	0.158
9	0.354
12	0.472
18	0.708
25.2	0.992
54	2.126

mm	inches
60	2.362
63	2.480
67.7	2.665
78	3.070
89	3.504

For detailed information on wire-wrapping, see the Application Book "Design with 50-Series modules, print number 9399 263 06001.

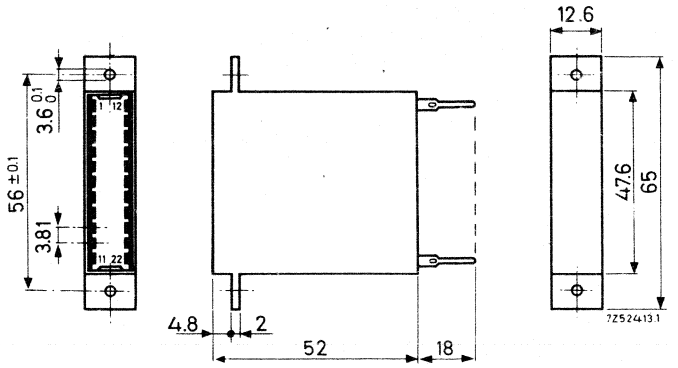
Thumbwheel switch (SU50)



mm	inches
2	0.078
3	0.118
3.81	0.150
5.5	0.216
$12.7^{-0}_{-0.1}$	$0.5^{-0}_{-0.004}$

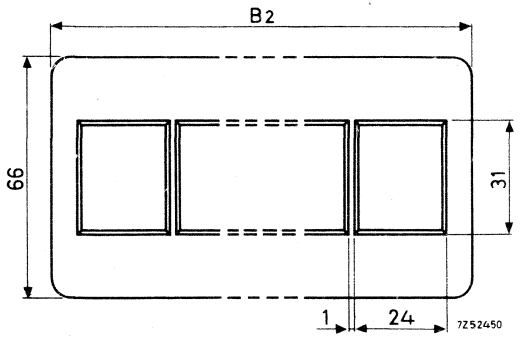
mm	inches
$46.5^{-0}_{-0.5}$	$1.831^{-0}_{-0.02}$
47.5	1.870
52.5	2.067
56 ± 0.15	2.205 ± 0.006
65	2.559
70.9	2.791

Auxiliary modules (3.NOR50, 4.NOR51, PSR50, LRD50, PDU50A, PDU50B and DCD50)

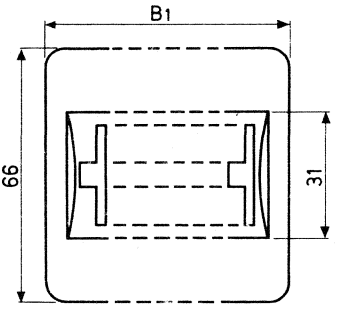


mm	inches	mm	inches
2	0.078	18	0.708
3.6 0.1 0	0.142 0.004 0	47.6	1.874
3.81	0.150	52	2.047
4.8	0.189	56 ± 0.1	2.205 ± 0.004
12.6	0.496	65	2.559

Façades



Front façade for indicator modules
(For B_2 see next page)



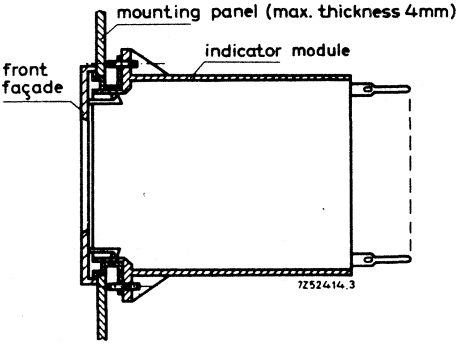
Mounting façade for thumbwheel switches
(For B_1 see next page)

mm	inches
1	0.039
24	0.945
31	1.220
66	2.598

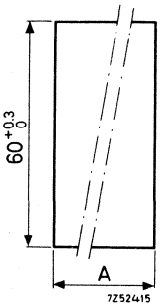
number of modules	indicator modules width B_2		thumbwheel switches width B_1	
	mm	inches	mm	inches
1	35.4	1.394	24	0.945
2	60.8	2.394	36.7	1.445
3	86.2	3.394	49.4	1.945
4	111.6	4.394	62.1	2.445
5	137.0	5.394	74.8	2.945
6	162.4	6.394	87.5	3.445

MOUNTING

Indicator modules (NIC50, RIC50, MID50 and SID50)



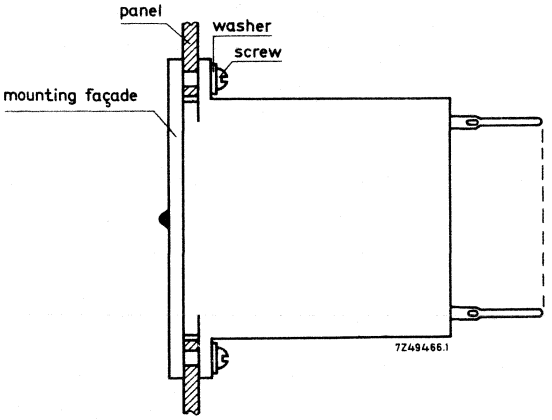
The module is fixed to a mounting panel by means of two screws. The maximum thickness of the mounting panel is 4 mm (0.157 inch). The aperture in the mounting panel is proportional to the number of indicator modules (see table below).
The front façades clip in to the indicator modules.



number of modules	width A	
	mm	inches
1	25.4 + 0.5	1 + 0.02
2	50.8 + 0.5	2 + 0.02
3	76.2 + 0.5	3 + 0.02
4	101.6 + 0.5	4 + 0.02
5	127.0 + 0.5	5 + 0.02
6	152.4 + 0.5	6 + 0.02

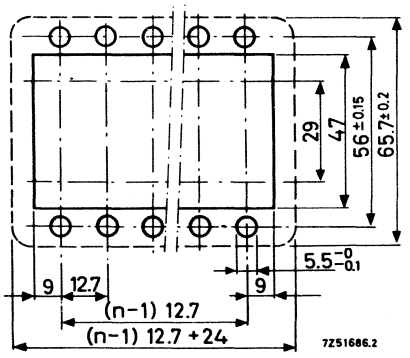
($60^{+0.3}_{0}$ mm = $2.362^{+0.012}_{0}$ inch)

Thumbwheel switches (SU50)



The switches can be mounted in panels with a thickness up to 4 mm by means of mounting façades and the screws and washers supplied. When the panel thickness is less than 4 mm (0.157 inch), additional washers must be used between the panel and the switch.

The dimensions of the necessary apertures in the mounting panel are given in the drawing below; the outline of the mounting façade is indicated by a dash line.

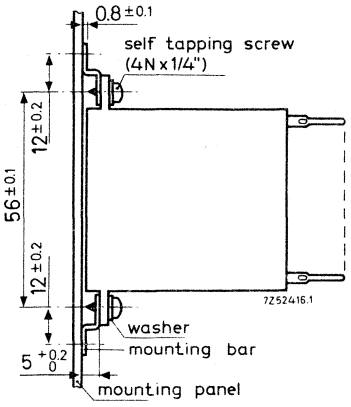


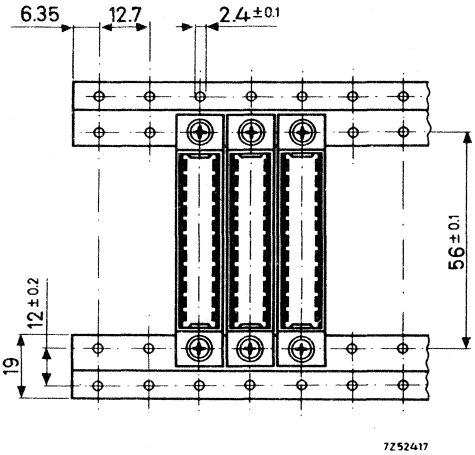
(n = number of switches)

mm	hes
5.5 -0 -0.1	0 -0 -0.004
9	0.354
12.7	0.5
24	0.945
29	1.142
47	1.851
56 ± 0.15	2.205 ± 0.004
65.7 ± 0.2	2.587 ± 0.008

Auxiliary modules (3.NOR50, 4.NOR51, PSR50, LRD50, PDU50A, PDU50B and DCD50)

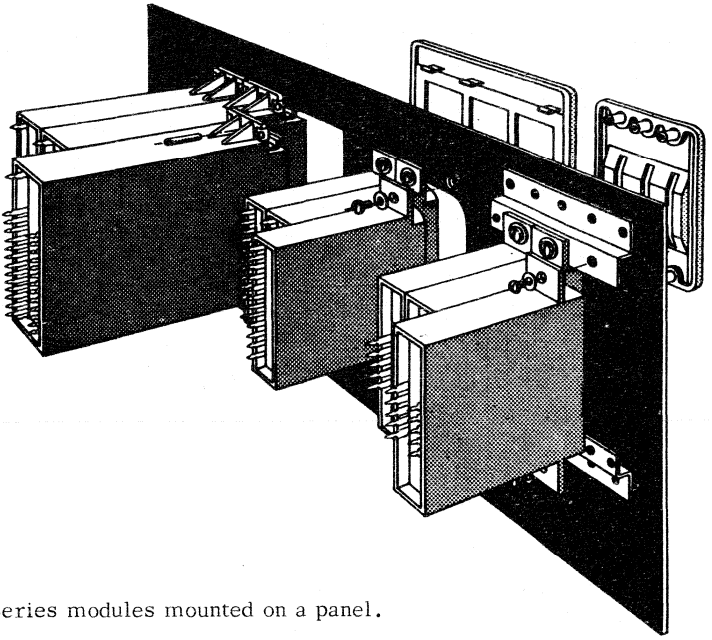
Auxiliary modules are to be fixed to a mounting panel with the aid of two metal bars (available in standard length of 21 positions).
The fixation of each module to the metal bar is done with two self tapping screws (4N x $\frac{1}{4}$inch).



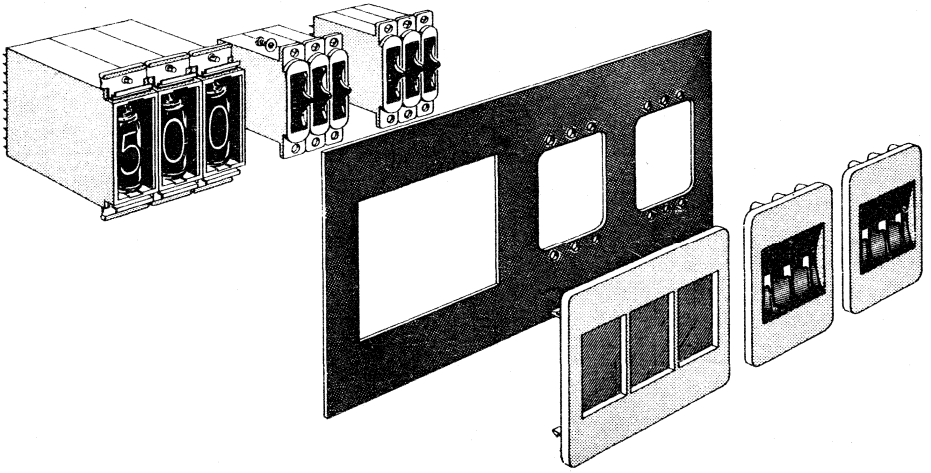


mm	inches
0.8 ± 0.1	0.032 ± 0.004
5 +0.2 0	0.197 +0.008 0
12 ± 0.2	0.472 ± 0.008
56 ± 0.1	2.205 ± 0.004

mm	inches
2.4 ± 0.1	0.094 ± 0.004
6.35	0.25
12 ± 0.2	0.472 ± 0.008
12.7	0.5
19	0.748
56 ± 0.1	2.205 ± 0.004



50-Series modules mounted on a panel.



CHARACTERISTICS

Ambient temperature range

Operating: -25 to +70 °C
-10 to +70 °C, for DCD50 at $V_P = +24\ V_{dc} \pm 25\%$
Storage : -40 to +85 °C

Counting rate

Uni-directional: max. 50 kHz
Bi-directional : max. 12 kHz

Supply voltage

Logic supply: single rail, $+24V_{dc} \pm 10\%$ 1)
Tube supply : high voltage, +250V ± 18%

Fan out

Decade counter: the counter units can be loaded with 6 different programmes.

NOR gate : each output may be loaded with the inputs of six other NOR's. The NOR50 and NOR51 are fully compatible with NOR units of the 60-Series.

1) Note that output units may be operated from a supply voltage of $+24V_{dc}$, ± 25%.

TEST SPECIFICATIONS

All modules of the 50-Series are designed to meet the tests below. Before and during manufacture samples of modules are regularly subjected to these tests.

1. Shock test according to method 202B of MIL-STD-202C, 3 blows 50 g in 3 perpendicular directions.
2. Vibration test according to method 201A of MIL-STD-202C;
   Frequency 10-55 Hz, amplitude 0.76 mm max., cycle time 1 min, 2 hours in 3 perpendicular directions.
3. Temperature-cycling test according to method 102A of MIL-STD-202; 5 cycles from -40 to +100 °C.
4. Long-term humidity test according to I.E.C.68, test C.
   Duration 21 days at 40 °C and R.H. = 90-95%.
5. Solderability according to method 210 of MIL-STD-202.

LOADING TABLE

NOTES

By expressing the input requirements and output capabilities of most modules in "DRIVE UNITS (D.U)", system design is greatly simplified.
Moreover input requirements of all modules are additive.

*) Also suitable for driving 2 x C_F/C_R of RIC50.

**) Two inputs in parallel or one input always floating.

type	function	input		output	
		terminal	required	terminal	available
NIC50	Uni-directional direct display counter	R	To be driven from Q_R of PSR50	Q_0-Q_9	To drive 6 x buffer NOR's + 1 x T-NIC50 + I_0-I_9 of 6 x MID50 + PDU50
		T	To be driven from Q_T of PSR50 or Q_0-Q_9 of NIC50		
RIC50	Bi-directional direct display counter	R	To be driven from Q_R of PSR50	Q_0-Q_9	To drive 6 x buffer NOR's + 1 x T-RIC50 + I_0-I_9 of 6 x MID50 + PDU50
		T_F/T_R	To be driven from Q_T of PSR50 or Q_0-Q_9 of RIC50		
		C_F/C_R	To be driven from Q of LRD50 or Q of NOR50/51		
MID50	Buffer memory with direct display	I_0-I_9	To be driven from Q_0-Q_9 of NIC50, RIC50 or MID50	Q_0-Q_9	To drive decimal input of PDU50 + I_0-I_9 of 3 x MID50
		T_C	To be driven from Q_R or Q_T of PSR50		
SID50	Driver plus and minus indicator tube	+ and - character	1 D.U.	none	Not applicable
3.NOR50	6 Input buffer NOR	G_1-G_6	To be driven from Q_0-Q_9 of NIC50 or RIC50	Q_1	2 D.U.
	Dual 4 input NOR	G_7-G_{14}	1 D.U.	Q_2/Q_3	6 D.U.*)
4.NOR51	Quadruple 4 input NOR	G_1-G_{16}	1 D.U.	Q_1-Q_4	6 D.U.*)

type	function	input terminal	input required	output terminal	output available
PSR50	Pulse shaper	B (via R = 39 kΩ)	2 D.U.	Q_T	2 x (T_R + T_F) - RIC50 + 2 D.U. or 4 x T-NIC50 + 2 D.U. or 6 x T_C-MID50
	Reset	T	1 D.U.	Q_R	6 x R-NIC50/RIC50 or 6 x T_C-MID50
		G	1 D.U.	Q_L	4 D.U.
LRD50	Lamp/relay driver	G_1-G_3	1 D.U.	Q	300 mA, 30V (abs.max.) or 6 x C_F/C_R -RIC50
PDU50A	Printer drive unit	I_0-I_9	To be driven from Q_0-Q_9 of NIC50, RIC50 or MID50	Q_0-Q_9	2 D.U.
		L	To be driven from L_1-L_3 of PDU50B		
PDU50B	Printer drive unit	C	To be driven from: -Q_T of PSR50 or -NOR unit**	L_1-L_3	To drive input L of PDU50A
		S_1-S_3	To be driven from: -Q_0-Q_9 of NIC50 or RIC50 -DCD50 -NOR unit**		
DCD50	Decade counter and divider	$T_A/T_C/T_D$ T_{B_1}/T_{B_2} S	0 D.U. 1 D.U. 1.5 D.U.	Q_A, $\overline{Q_A}$, Q_B, $\overline{Q_B}$, Q_C, $\overline{Q_C}$, Q_D, $\overline{Q_D}$	To drive 1 x T-NIC50/RIC50
		C_S	6 D.U.	Q_A, Q_B, $\overline{Q_B}$, Q_C, $\overline{Q_C}$	6 D.U. + 1 x T-DCD50 or 4 D.U. + 1 x B-PSR50
				$\overline{Q_A}$, Q_D, $\overline{Q_D}$	see data sheet

Survey of terminal location

terminals	indicator modules (Fig.A)				auxiliary modules (Fig.B)						
	NIC50	RIC50	MID50	SID50	3.NOR50	4.NOR51	PSR50	LRD50	PDU50A	PDU50B	DCD50
HV	V_{p3}	V_{p3}	V_{p3}	V_{p3}	not provided	not provided	not provided	not provided	not provided	not provided	not provided
A	not provided	not provided	LS	X	not provided	not provided	not provided	not provided	not provided	not provided	not provided
B	not provided	not provided	T_C	Y	not provided	not provided	not provided	not provided	not provided	not provided	not provided
C	not provided	not provided	I_0	Z	not provided	not provided	not provided	not provided	not provided	not provided	not provided
1	V_{p1}	V_{p1}	V_{p1}	V_{p1}	V_{p1}	V_{p1}	V_{p1}	not provided	I_1	V_{p1}	V_{p1}
2	0	0	0	0	0	0	0	0	I_2	0	0
3	not provided	C_F	I_1	not provided	G_1	G_1	Q_R	V_{p2}	I_3	K_1	$\overline{Q}_D$
4	not provided	C_R	I_2	not provided	G_2	G_2	Q_L	not provided	I_4	K_2	Q_D
5	F	F	I_3	not provided	G_3	G_3	Q_T	Q	I_5	L_1	Q_C
6	not provided	not provided	I_4	+	G_4	Q_2	i.c.	not provided	L	L_2	$\overline{Q}_C$
7	Q_5	Q_5	Q_5	-	G_5	Q_1	B	not provided	Q_1	L_3	T_{D_2}
8	Q_4	Q_4	Q_4	not provided	G_6	G_5	Z	G_1	Q_2	S_1	T_{D_1}
9	Q_3	Q_3	Q_3	not provided	D_1	G_6	A	G_2	Q_3	S_2	T_C
10	Q_2	Q_2	Q_2	not provided	D_2	G_7	G	G_3	Q_4	S_3	S_C
11	Q_1	Q_1	Q_1	not provided	Q_1	G_8	T	not provided	Q_5	C	S_D
12	not provided	not provided	I_9	~	G_7	G_9	not provided	not provided	Q_6	not provided	S_B
13	not provided	not provided	I_8	not provided	G_8	G_{10}	not provided	not provided	Q_7	not provided	Q_B
14	R	R	I_7	not provided	G_9	G_{11}	not provided	not provided	Q_8	not provided	$\overline{Q}_B$
15	not provided	T_R	I_6	not provided	G_{10}	G_{12}	not provided	not provided	Q_9	not provided	S_A
16	T	T_F	I_5	not provided	Q_3	Q_4	not provided	not provided	Q_0	not provided	Q_A
17	DP	DP	DP	not provided	Q_2	Q_3	not provided	not provided	L	not provided	$\overline{Q}_A$
18	Q_6	Q_6	Q_6	not provided	G_{11}	G_{13}	not provided	not provided	I_6	not provided	T_{B_1}
19	Q_7	Q_7	Q_7	not provided	G_{12}	G_{14}	not provided	not provided	I_7	not provided	T_{B_2}
20	Q_8	Q_8	Q_8	not provided	G_{13}	G_{15}	not provided	not provided	I_8	not provided	K
21	Q_9	Q_9	Q_9	not provided	G_{14}	G_{16}	not provided	not provided	I_9	not provided	T_A
22	Q_0	Q_0	Q_0	not provided	R_1	G_4	not provided	not provided	I_0	not provided	C_S

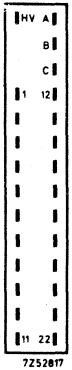


Fig.A.

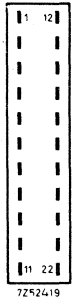
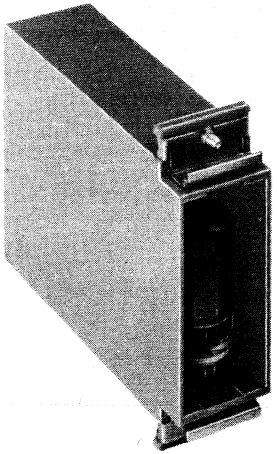


Fig.B.

NUMERICAL INDICATOR COUNTER

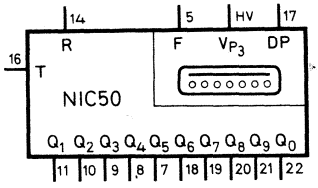


RZ 23932-3

Function	Uni-directional decade counter with direct numerical display for preset programmed control systems. Maximum counting rate: 50 kHz.

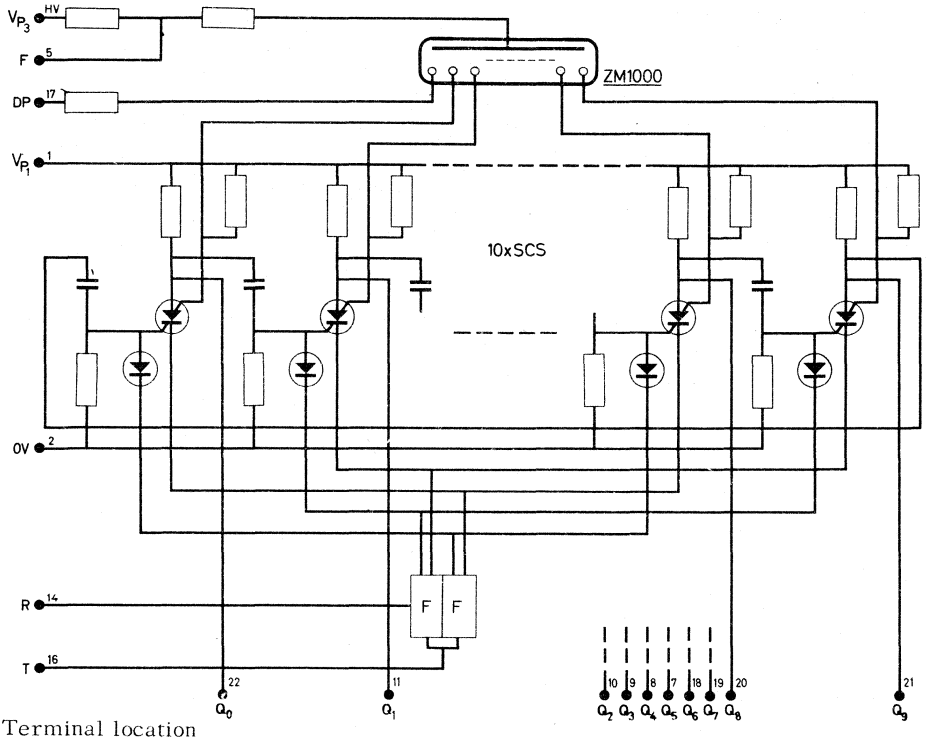
DESCRIPTION

The NIC50 is a uni-directional decade counter coupled to the numerical indicator tube ZM1000, assembled in one plastic case. The ZM1000 is mounted at the front of the case, the input and output terminals are found at the rear.
Ten decimal outputs enable connection to other units for active counting operations. There is also a terminal for display of the decimal point in the ZM1000 at the left of any numeral.
Use is made of silicon controlled switches featuring a direct drive of the ZM1000.
Carry pulses to trigger a succeeding counter NIC50 are obtained from output Q_0 (terminal 22) at the nine to zero transition.
The trigger (counting) pulse and the reset pulse are delivered by the pulse shaper/reset unit PSR50.
Filtering of the high voltage from transients can be obtained by connecting a capacitor of approximately 0.1 μF between terminal F and the central earth point.

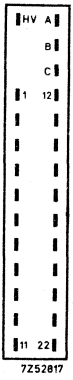


Drawing symbol

CIRCUIT DATA



Terminal location



HV = V_{p_3} = +250 V supply for numerical indicator tube
A = not provided
B = not provided
C = not provided
1 = V_{p_1} = +24 V supply
2 = 0 = common 0 V
3 = not provided
4 = not provided
5 = F = connection for filtering purposes
6 = not provided
7 = Q_5 = decimal output 5
8 = Q_4 = decimal output 4
9 = Q_3 = decimal output 3
10 = Q_2 = decimal output 2
11 = Q_1 = decimal output 1
12 = not provided
13 = not provided
14 = R = reset input
15 = not provided
16 = T = counting trigger input
17 = DP = input decimal point
18 = Q_6 = decimal output 6
19 = Q_7 = decimal output 7
20 = Q_8 = decimal output 8
21 = Q_9 = decimal output 9
22 = Q_0 = decimal output 0

Power supply

	voltage	current
Tube supply	+250 V ± 18%	3 mA
Logic supply	+ 24 V ± 10%	12 mA

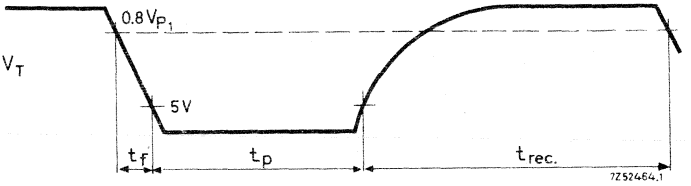
INPUT DATA

Trigger (counting) input T (terminal 16)

This input is to be driven by a negative going pulse, delivered by output Q_T of the unit PSR50, or by a preceding counter unit.

Voltage	V_T = from 0.8 V_{P_1} to 5 V
Required direct current	$-I_T$ = max. 1.5 mA (at V_T = 5 V)
Required transient charge when V_T changes from 0.8 V_{P_1} to 5 V in 1 μs	$-Q_T$ = max. 6.3 nC

Time data



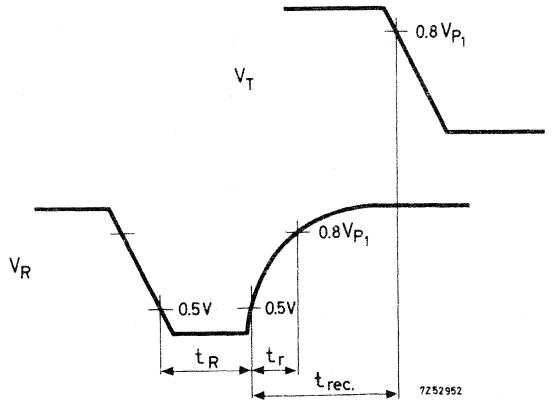
Fall time	t_f = max. 1 μs
Pulse duration	t_p = min. 4 μs
Recovery time	t_{rec} = max. 10 μs

Reset input R (terminal 14)

This input is to be driven by a LOW voltage level, delivered by output Q_R of the unit PSR50.

Required voltage	V_R = max. 0.5 V
Required direct current	I_R = max. 8.5 mA

Time data



Input pulse duration	t_R = min. 15 μs
Recovery time	t_{rec} = max. 50 μs
Trailing edge	t_r = max.1.2 μs

Decimal point input DP (terminal 17)

This input is to be driven by a LOW voltage level with the following requirements:

Decimal point ON

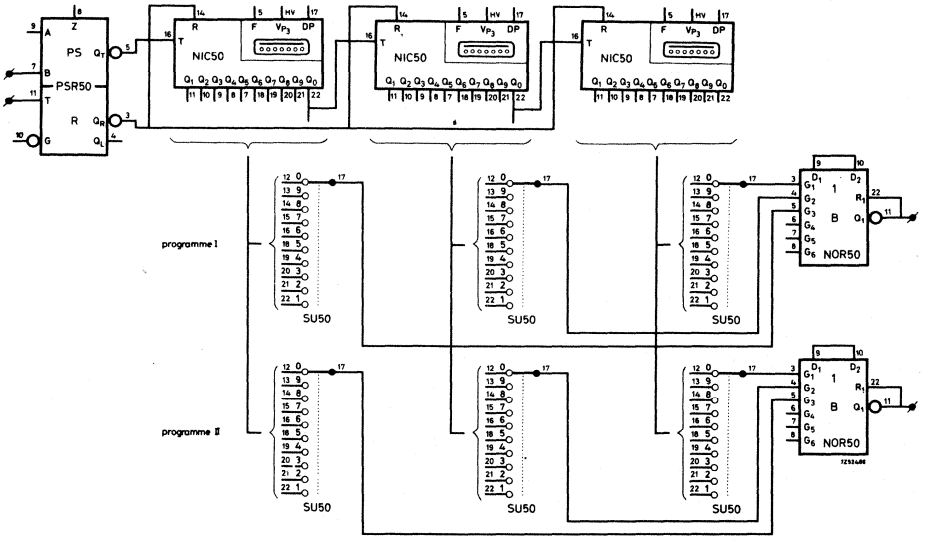
Voltage	V_{DP} = max. 0.5 V
Direct current	I_{DP} = 165 μA (typical)

Decimal point OFF

Voltage	V_{DP} = min. 50 V or terminal 17 floating

OUTPUT DATA

The digits 0-9 are available at the output terminals Q_0-Q_9.
These outputs are primarily intended to drive the buffer NOR in the unit 3.NOR50, in most cases via the 10 position preset switch SU50 as indicated below.



Each Q-output can be loaded with 6 buffer NOR's of the 3.NOR50 units simultaneously in excess of the carry pulse for the succeeding NIC50 counter. This means that 6 preset programmes can be applied as a maximum.

Output voltage LOW (SCS conducting)

Voltage	V_Q = max. 5 V
Available direct current	I_Q = max. 1.5 mA
Available transient charge when V_Q changes from 0.8 V_{P_1} to 5 V in 1 μs	Q_Q = max. 9.5 nC

Output voltage HIGH (SCS non conducting)

Voltage	V_Q = 0.8 V_{P_1} to V_{P_1}
Available direct current	$-I_Q$ = max. 0.32 mA

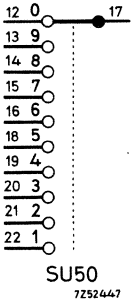
Wiring capacitance C_w = max. 200 pF

Time data

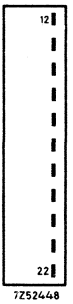
Delay between trigger input and positive going output t_{d_1} = max. 3 μs
Delay between trigger input and negative going output t_{d_2} = max. 4 μs

10 position preset switch

In the 50-Series for preset programmed counting, use is made of the 10 position thumbwheel switch SU50, which is identical to the existing type 10P1C, catalogue number 4311 027 82321.



Drawing symbol



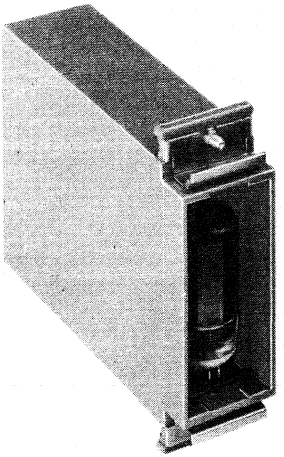
Terminal location

12 = input 0
13 = input 9
14 = input 8
15 = input 7
16 = input 6
17 = output (pole)
18 = input 5
19 = input 4
20 = input 3
21 = input 2
22 = input 1

The ten input terminals 0-9 have to be connected directly to the ten decimal output terminals Q_0-Q_9 of the decade counter NIC50.
The output terminal 17 has to be connected to one of the inputs of the buffer NOR in the unit 3.NOR50.

Note - For more specific data of the thumbwheel switch 10P1C, see data sheets of thumbwheel switches 4311 027 82...

REVERSIBLE INDICATOR COUNTER

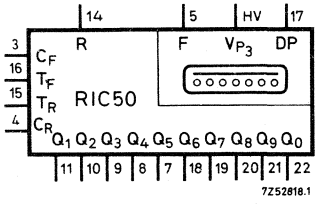


RZ 23932-3

Function	Bi-directional decade counter with direct numerical display for preset programmed control systems. Maximum counting rate: 12 kHz.

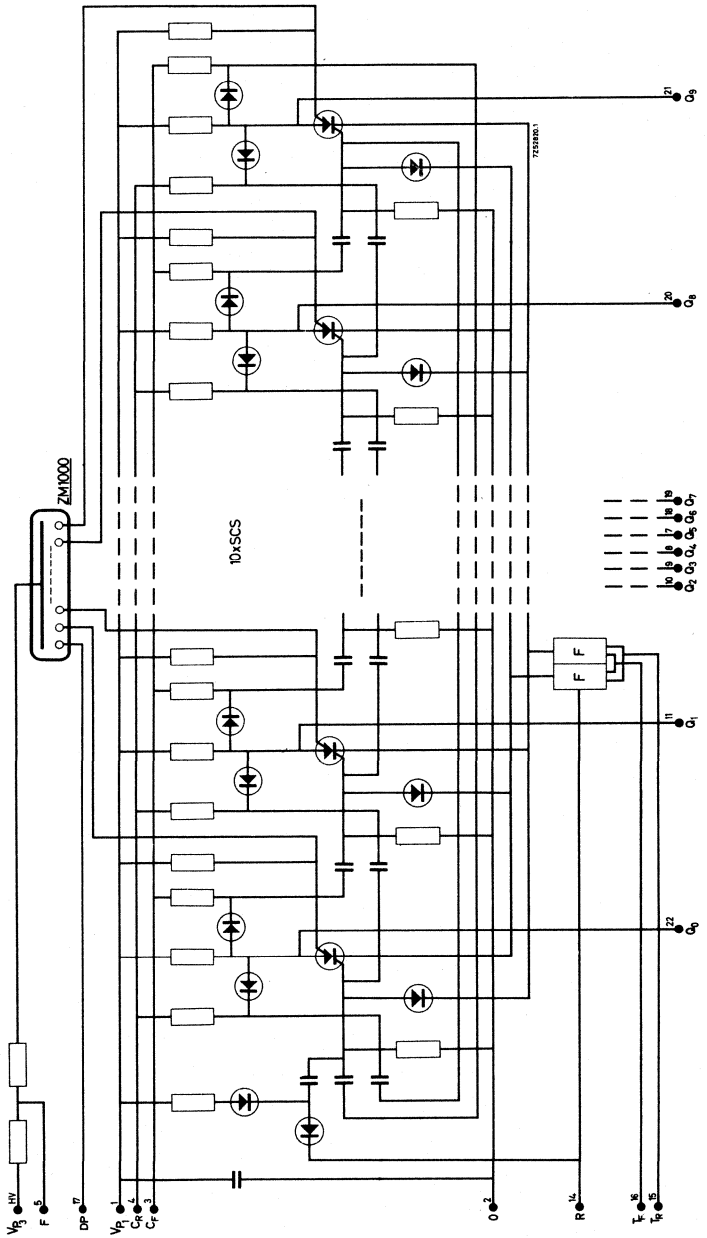
DESCRIPTION

The RIC50 is a bi-directional decade counter coupled to the numerical indicator tube ZM1000, assembled in one plastic case. The ZM1000 is mounted at the front of the case, the input and output terminals are found at the rear.
Ten decimal outputs enable connection to other units for active counting operations. There is also a terminal for display of the decimal point in the ZM1000 at the left of any numeral.
Use is made of silicon controlled switches featuring a direct drive of the ZM1000. The trigger (counting) pulses and the reset pulse are delivered by the pulse shaper/reset unit PSR50.
Filtering of the high voltage from transients can be obtained by connecting a capacitor of approximately 0.1 μF between terminal F and the central earth point.

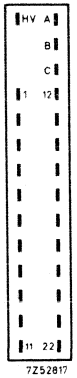


Drawing symbol

CIRCUIT DATA



Terminal location



HV = V_{p_3} = +250 V supply for numerical indicator tube
A = not provided
B = not provided
C = not provided
1 = V_{p_1} = +24 V supply
2 = 0 = common 0 V
3 = C_F = control forward direction
4 = C_R = control reverse direction
5 = F = connection for filtering purposes
6 = not provided
7 = Q_5 = decimal output 5
8 = Q_4 = decimal output 4
9 = Q_3 = decimal output 3
10 = Q_2 = decimal output 2
11 = Q_1 = decimal output 1
12 = not provided
13 = not provided
14 = R = reset input
15 = T_R = trigger input reverse counting
16 = T_F = trigger input forward counting
17 = DP = input decimal point
18 = Q_6 = decimal output 6
19 = Q_7 = decimal output 7
20 = Q_8 = decimal output 8
21 = Q_9 = decimal output 9
22 = Q_0 = decimal output 0

Power supply

	voltage	current
Tube supply	+250 V ± 18%	3 mA
Logic supply	+ 24 V ± 10%	23 mA

INPUT DATA

Counting conditions

The counting direction is determined by the voltage levels applied to C_F (terminal 3) and C_R (terminal 4).

Forward counting

V_{CF} = max. 1.6 V I_{CF} = max. 7.5 mA
V_{CR} = 0.95 V_{p_1} to V_{p_1}
} Each input to be driven by LRD50 or NOR unit

Counting pulse from PSR50 - Q_T to be applied to input T_F (terminal 16).

Reverse counting

V_{CR} = max. 1.6 V I_{CR} = max. 7.5 mA
V_{CF} = 0.95 V_{p_1} to V_{p_1}
} Each input to be driven by LRD50 or NOR unit

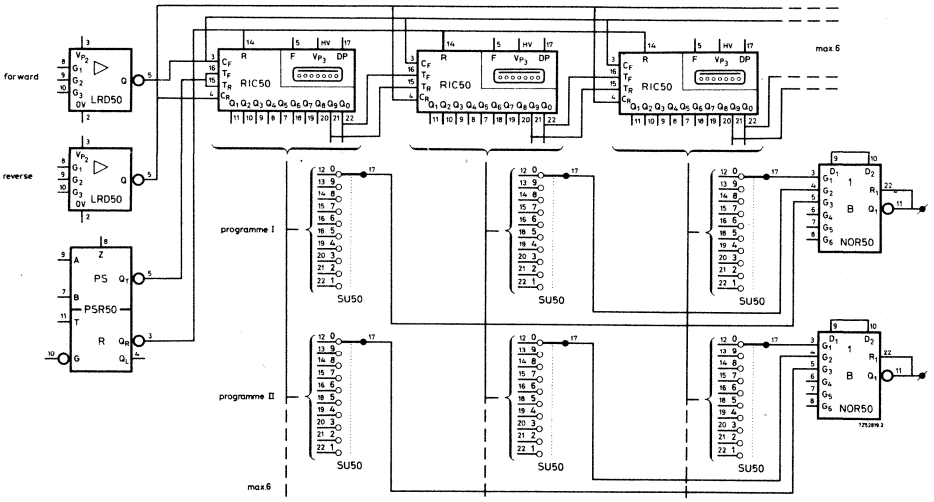
Counting pulse from PSR50 - Q_T to be applied to input T_R (terminal 15).

Note - When both control inputs C_F and C_R are HIGH the RIC50 is blocked for counting pulses.

When two units RIC50 are operating in series the following interconnections have to be made (see figure below).

For forward counting: Q_0 (terminal 22) of the preceding RIC50 has to be connected to T_F (terminal 16) of the succeeding RIC50.

For reverse counting: Q_9 (terminal 21) of the preceding RIC50 has to be connected to T_R (terminal 15) of the succeeding RIC50.



When the levels of the control voltages at C_F or C_R are changed a recovery time t_{rec} = min. 100 μs is to be observed.

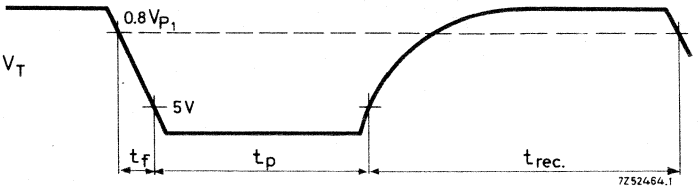
Trigger (counting) inputs T (terminals 16 and 15)

These inputs are to be driven by the negative going pulse, delivered by output Q_T of the unit PSR50 or by the corresponding output Q_0 (forward) or Q_9 (reverse) of the preceding counting decade RIC50.

Triggering edge	V_T = 0.8 V_{p_1} to 5 V
Required direct current	I_T = max. 1.5 mA (at V_T = 5 V)
Required transient charge when V_T changes from 0.8 V_{p_1} to 5 V in 1 μs	Q_T = max. 6.3 nC

When two trigger inputs are interconnected the above I_T and Q_T requirements have to be doubled.

Time data



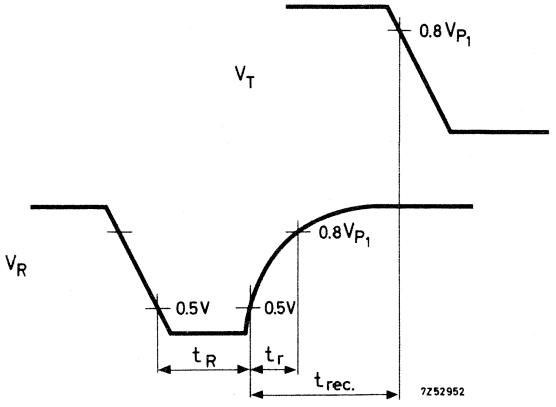
Fall time	t_f	= max. 1 μs
Pulse duration	t_p	= min. 4 μs
Recovery time	t_{rec}	= min. 15 μs
Time between two successive pulses		min. 85 μs

Reset input R (terminal 14)

This input is to be driven by a LOW voltage level, delivered by output Q_R of the unit PSR50.

Required voltage	V_R	= max. 0.5 V
Required direct current	I_R	= max. 8.5 mA

Time data



Pulse duration	t_R	= min. 15 μs
Recovery time	t_{rec}	= max. 80 μs
Trailing edge	t_r	= max. 1.2 μs

Decimal point input DP (terminal 17)

This input is to be driven by a LOW voltage level with the following requirements:

Decimal point ON

Voltage	V_{DP} = max. 0.5 V
Direct current	I_{DP} = 165 μA (typical)

Decimal point OFF

Voltage	V_{DP} = min. 50 V or terminal 17 floating

OUTPUT DATA

The digits 0-9 are available at the output terminals Q_0-Q_9.
These outputs are primarily intended to drive the buffer NOR in the unit 3.NOR50, in most cases via the 10 position preset switch SU50.
Each Q-output can be loaded with 6 buffer NOR's of the 3.NOR50 units simultaneously in excess of the carry pulses for the succeeding RIC50 counter. This means that 6 preset programmes can be applied as a maximum.

Output voltage LOW (SCS conducting)

Voltage	V_Q = max. 5 V
Available direct current	I_Q = max. 1.5 mA
Available transient charge when V_Q changes from 0.8 V_{p1} to 5 V in 1 μs	Q_Q = max. 9.5 nC

Output voltage HIGH (SCS non conducting)

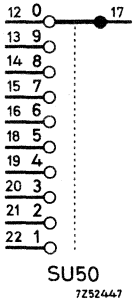
Voltage	V_Q = 0.8 V_{p1} to V_{p1}
Available direct current	I_Q = max. 0.32 mA
Wiring capacitance	C_W = max. 200 pF

Time data

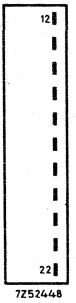
Delay between trigger input and positive going output t_{d1} = max. 3 μs.
Delay between trigger input and negative going output t_{d2} = max. 4 μs.

10 position preset switch

In the 50-Series for preset programmed counting, use is made of the 10 position thumbwheel switch SU50, which is identical to the existing type 10P1C, catalogue number 4311 027 82321.



Drawing symbol



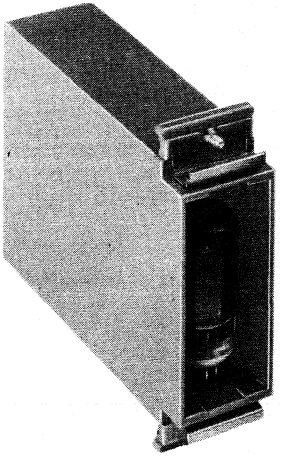
Terminal location

12 = input 0
13 = input 9
14 = input 8
15 = input 7
16 = input 6
17 = output (pole)
18 = input 5
19 = input 4
20 = input 3
21 = input 2
22 = input 1

The ten input terminals 0-9 have to be connected directly to the ten decimal output terminals Q_0-Q_9 of the reversible decade counters RIC50.
The output terminal 17 has to be connected to one of the inputs of the buffer NOR in the unit 3.NOR50.

Note - For more specific data of the thumbwheel switch 10P1C, see data sheets of thumbwheel switches 4311 027 82...

MEMORY INDICATOR DRIVER



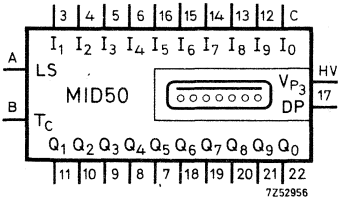
RZ 23932-3

Function

Integral buffer memory with direct numerical display for storage of information from decade counters NIC50 or RIC50.
Apart from numerical display, decimal output is available for e.g. printer drive.

DESCRIPTION

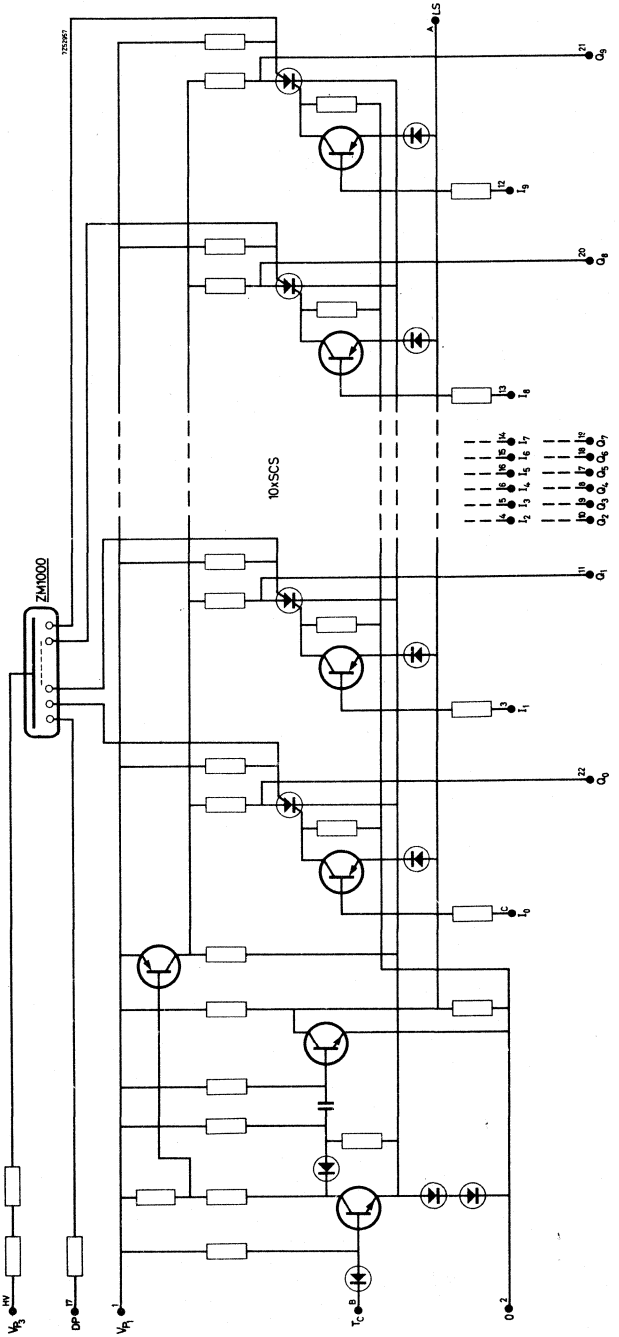
The MID50 is a buffer memory coupled to the numerical indicator tube ZM1000, assembled in one plastic case. The ZM1000 is mounted at the front of the case, the input and output terminals are found at the rear.
Use is made of silicon controlled switches featuring a direct drive of the ZM1000.
The ten decimal inputs (I_0-I_9) can be connected directly to the 10 corresponding outputs (Q_0-Q_9) of either the uni-directional decade counter NIC50 or the bi-directional decade counter RIC50, without influencing the output capability (fan out) of both types of counters.
By applying one single pulse to input T_C (terminal B) the decimal information is transferred from the decade counter into the buffer memory MID50 and remains there steadily displayed.
The MID50 is also provided with 10 decimal outputs for e.g. printer read-out *).
There is a terminal for display of the decimal point in the ZM1000 at the left of any numeral.



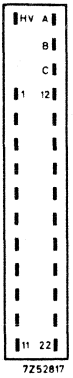
Drawing symbol

*) For this purpose printer drive units PDU50A and PDU50B are available.

CIRCUIT DATA



Terminal location



HV = V_{p3} = +250 V supply for numerical indicator tube
A = LS = level shift facility
B = T_C = shift pulse input
C = I_0 = decimal input 0
1 = V_{p1} = +24 V supply
2 = 0 = common 0 V
3 = I_1 = decimal input 1
4 = I_2 = decimal input 2
5 = I_3 = decimal input 3
6 = I_4 = decimal input 4
7 = Q_5 = decimal output 5
8 = Q_4 = decimal output 4
9 = Q_3 = decimal output 3
10 = Q_2 = decimal output 2
11 = Q_1 = decimal output 1
12 = I_9 = decimal input 9
13 = I_8 = decimal input 8
14 = I_7 = decimal input 7
15 = I_6 = decimal input 6
16 = I_5 = decimal input 5
17 = DP = input decimal point
18 = Q_6 = decimal output 6
19 = Q_7 = decimal output 7
20 = Q_8 = decimal output 8
21 = Q_9 = decimal output 9
22 = Q_0 = decimal output 0

Power supply

	voltage	current
Tube supply	+250 V ± 18%	3 mA
Logic supply	+ 24 V ± 10%	20 mA

INPUT DATA

Decimal inputs I_0-I_9

These inputs are to be fed by the decimal outputs Q_0-Q_9 of either the uni-directional decade counter NIC50 or the bi-directional decade counter RIC50.
One of the ten inputs must be fed with a LOW voltage level, the remaining nine inputs with a HIGH voltage level. By applying one transfer pulse to T_C (terminal B) that output Q becomes LOW of which the corresponding input I carries the LOW voltage, while simultaneously the corresponding figure of the indicator tube is lit. The other nine outputs of the MID50 will be HIGH. The decimal information of a NIC50 or RIC50 is transferred into the MID50 at the positive going edge of the transfer pulse

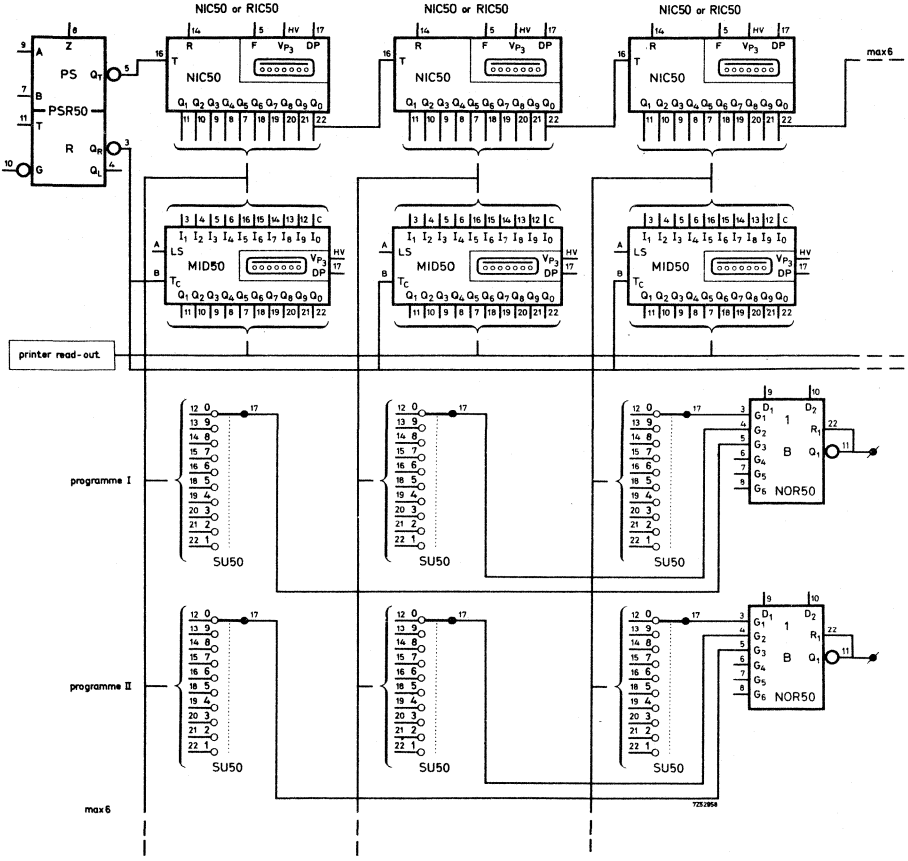
Voltage LOW

V_I = max. 5 V

I_I = max. 0.06 mA

Voltage HIGH

V_I = 0.8 V_{p1} to V_{p1}



Level shift input LS (terminal A)

By connecting a suitable zener diode between LS and 0 V and a resistor between LS and V_{P1}, the correct functional behaviour of the MID50 can be accomplished also when the inputs I_0-I_9 are fed with non-standard voltage levels (not derived from NIC50 or RIC50).

Transfer pulse input T_C (terminal B)

This input is driven by a pulse generated at output Q_R or Q_T of the unit PSR50. The transferring action takes place at the positive going edge. Maximum 6 inputs T_C can be driven simultaneously by output Q_R or Q_T of the PSR50.

Voltage LOW

V_B = max. 0.5 V

I_B = max. 0.5 mA

Voltage HIGH

V_B = 0.62 V_{p1} to V_{p1}

Decimal point input DP (terminal 17)

This input is to be driven by a LOW voltage level with the following requirements:

Decimal point ON

Voltage	V_{DP} = max. 0.5 V
Direct current	I_{DP} = 165 μA (typical)

Decimal point OFF

Voltage	V_{DP} = min. 50 V or terminal 17 floating

OUTPUT DATA

The digits 0-9 are available at the output terminals Q_0-Q_9. These outputs are primarily intended for either printer read-out purposes or shift register configurations.

Output voltage LOW (SCS conducting)

Voltage	V_Q = max. 3.5 V
Available direct current	I_Q = max. 0.2 mA*)

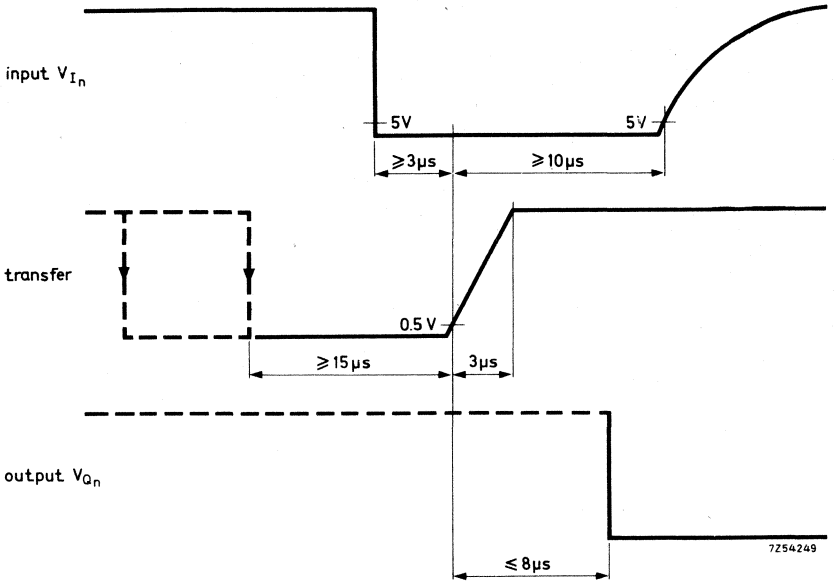
Output voltage HIGH (SCS non conducting)

Voltage	V_Q = 0.8 V_{p1} to V_{p1}
Available direct current	$-I_Q$ = max. 0.84 mA

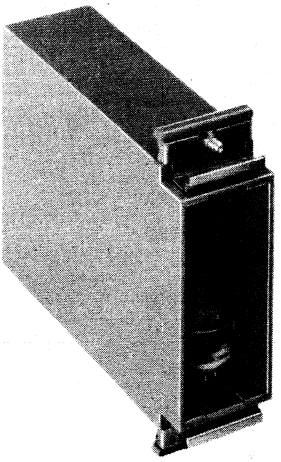
Wiring capacitance C_W = max. 200 pF

*) The sum of the output currents I_{Q0}-I_{Q9} may not exceed 200 μA.

Time data


input V_{I_n}
5V
5V
≥3μs
≥10μs
transfer
0.5 V
≥15μs
3μs
output V_{Q_n}
≤8μs
7Z54249

SIGN INDICATOR DRIVER

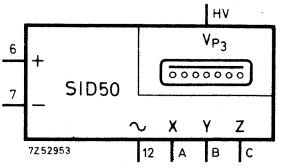


RZ 23932-3

Function	Driver of plus and minus character indicator tube. Characters ~, X, Y and Z are accessible

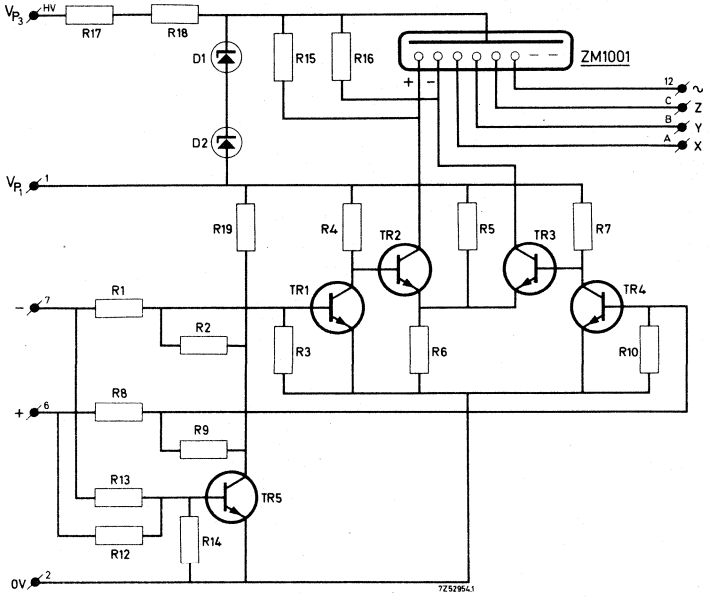
DESCRIPTION

The SID50 contains the plus and minus indicator tube ZM1001 and its driver stages in one plastic case. The ZM1001 is mounted at the front of the case, the connecting terminals are found at the rear.
A dark position of the ZM1001 can be obtained when both plus and minus inputs are driven by equal voltage levels.
The characters ~, X, Y and Z provided in the ZM1001 are also accessible.

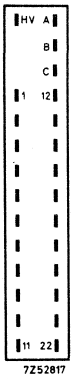


Drawing symbol

CIRCUIT DATA



Terminal location



HV = V_{p3} = +250 V supply for numerical indicator tube
A = X = X character
B = Y = Y character
C = Z = Z character
1 = V_{p1} = +24 V supply
2 = 0 = common 0 V
3 = not provided
4 = not provided
5 = not provided
6 = + = input driving + character
7 = − = input driving − character
8 to 11 = not provided
12 = ~ = ~ character
13 to 22 = not provided

Power supply

	voltage	current
Tube supply	+250 V ± 18%	2.8 mA
Logic supply	+ 24 V ± 10%	5.0 mA

INPUT DATA

Input terminals characters + and –

These inputs are to be driven by a HIGH voltage level to illuminate the corresponding character. A LOW level extinguishes the character.

HIGH voltage

V_+/V_- = 0.62 V_{p1} to V_{p1}

I_+/I_- = 0.17 mA (V = 13.4 V); EQUALS ONE D.U.*).

LOW voltage

V_+/V_- = max. 0.3 V

Characters ~, X, Y and Z

Visible : $V\sim/V_X/V_Y/V_Z$ = 0 to 10 V

Not visible: $V\sim/V_X/V_Y/V_Z$ = 60 to 120 V or floating

Dark : $V\sim/V_X/V_Y/V_Z$ = 80 to 120 V or floating

*) See also loading table.

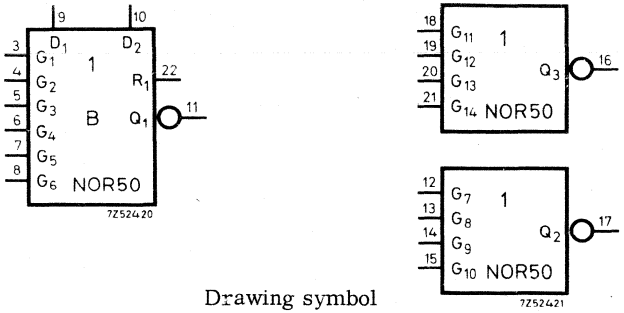
TRIPLE NOR GATE

Function

- 6 input buffer NOR for adapting the output levels of the NIC50 and the RIC50 to standard logic levels and
- dual 4 input NOR for logic purposes e.g. to form a memory function.

DESCRIPTION

The 3.NOR50 is intended to be used to memorize the count when the content of the unit(s) NIC50 or RIC50 corresponds with the preset position of the 10 position thumb-wheel switch SU50.



Drawing symbol

6 input buffer NOR

The 6 input buffer NOR is intended to adapt the output levels of the NIC50 or the RIC50 to the standard logic levels of the 4 input NOR's.
To this end each input of the 6 input buffer NOR is to be connected, directly or via the switch SU50, to one of the decimal outputs of the units NIC50 or RIC50.

Simplified truth table:

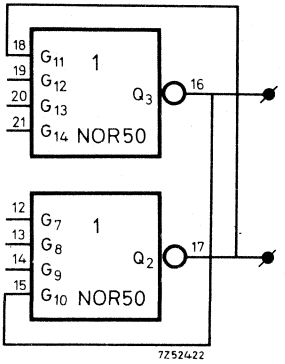
G_1	G_2	Q_1
H	H	L
L	H	L
H	L	L
L	L	H

All inputs (G_1 to G_6) must be LOW or floating for Q_1 is HIGH.

The 6 input buffer NOR can be provided with an intentional delay by interconnecting D_1 (terminal 9) and D2 (terminal 10) (see Time data). This intentional delay cancels hazardous (false) pulses that can occur during e.g. the transition from 499 to 500 at the transit counts 490 and 400, if preset programs have been set at these counts. The maximum delay can be decreased (the maximum counting rate increased) when an external capacitor is connected between D_1 and D_2.

Dual 4 input NOR

The 4 input NOR is intended for logic operations, such as memorizing the preset counts. To this end a memory function can be formed by cross connecting the two NOR's.

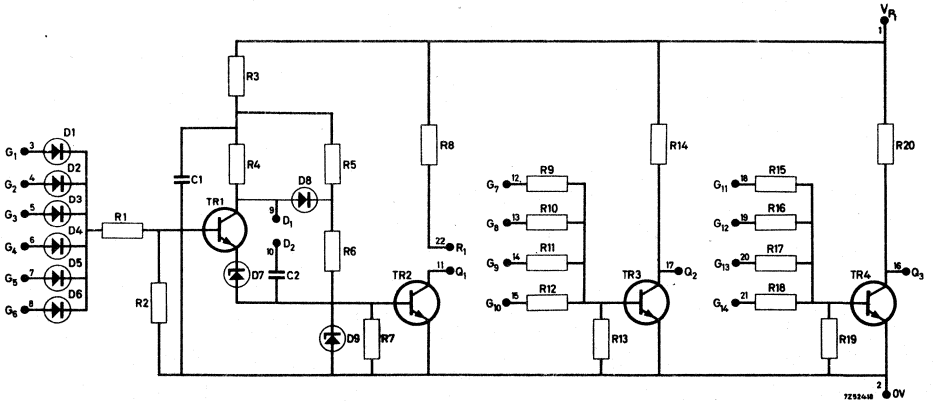


Simplified truth table:

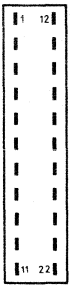
$G_7(G_{11})$	$G_8(G_{12})$	$Q_2(Q_3)$
H	H	L
H	L	L
L	H	L
L	L	H

All inputs G of a NOR must be LOW or floating for Q is HIGH.

CIRCUIT DATA



Terminal location



1 = V_{p_1} = +24 V supply
2 = 0 = common 0 V
3 = G_1 = input buffer NOR1
4 = G_2 = input buffer NOR1
5 = G_3 = input buffer NOR1
6 = G_4 = input buffer NOR1
7 = G_5 = input buffer NOR1
8 = G_6 = input buffer NOR1
9 = D_1 = } when interconnected
10 = D_2 = } providing built-in delay
11 = Q_1 = output buffer NOR1
12 = G_7 = input NOR2
13 = G_8 = input NOR2
14 = G_9 = input NOR2
15 = G_{10} = input NOR2
16 = Q_3 = output NOR3
17 = Q_2 = output NOR2
18 = G_{11} = input NOR3
19 = G_{12} = input NOR3
20 = G_{13} = input NOR3
21 = G_{14} = input NOR3
22 = R_1 = collector resistor buffer NOR1

Power supply

Voltage	V_{p_1} = 24 V ±10%
Current	I_{p_1} = 10.5 mA

INPUT DATA

6 input buffer NOR

Input HIGH: V_G = 0.8 V_{p_1} to V_{p_1}

I_G = 53 μA (V_G = 18.35 V)

Input LOW: V_G = 0 to 5.5 V

4 input NOR

Input HIGH: V_G = 0.62 V_{p_1} to V_{p_1}

I_G = 0.17 mA (V_G = 13.4 V); EQUALS ONE D.U.*)

Noise immunity: a voltage shift of 2 V on the minimum high level will not cause a change of the output voltage.

Input LOW: V_G = 0 to 0.3 V

Noise immunity: a voltage of +1 V with respect to the 0 V line applied to any one input (the other inputs at low level or floating) will not cause a change of the output voltage. The noise immunity can be increased by connecting unused inputs to 0 V.

*) See also loading table.

OUTPUT DATA

6 input buffer NOR

Output current: I_{Q_1} = 0.35 mA (V_{Q_1} = 13.4 V); EQUALS TWO D.U.*)

4 input NOR

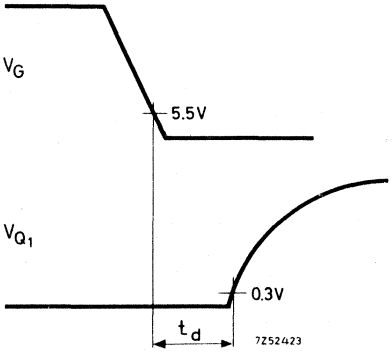
Output current: I_{Q_2/Q_3} = 1.02 mA (V_{Q_2/Q_3} = 13.4 V); EQUALS SIX D.U.*)

Time data

6 input buffer NOR

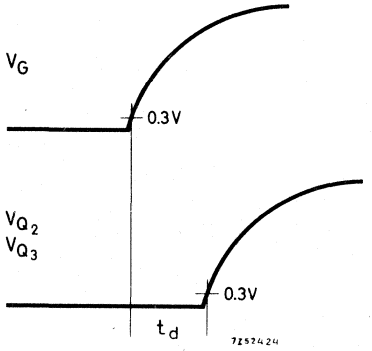
D_1 and D_2 interconnected: t_d = 7-18 μs

D_1 and D_2 not connected : t_d = 4 - 9 μs



4 input NOR

Delay, measured over two stages: t_d = max. 12 μs.
The delay is specified for C_w = 200 pF and worst input and output conditions.



*) See also loading table.

QUADRUPLE NOR GATE

Function — Quadruple 4 input NOR for logic operations e.g. to form memory functions.

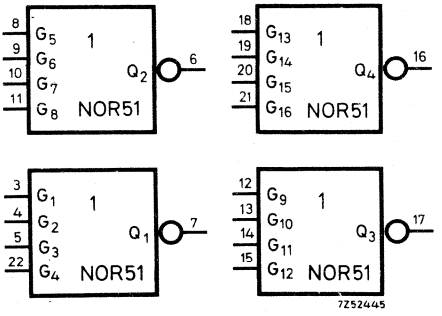
DESCRIPTION

The 4 input NOR is intended for logic operations. A memory function can be formed by cross connecting two NOR's.

Simplified truth table:

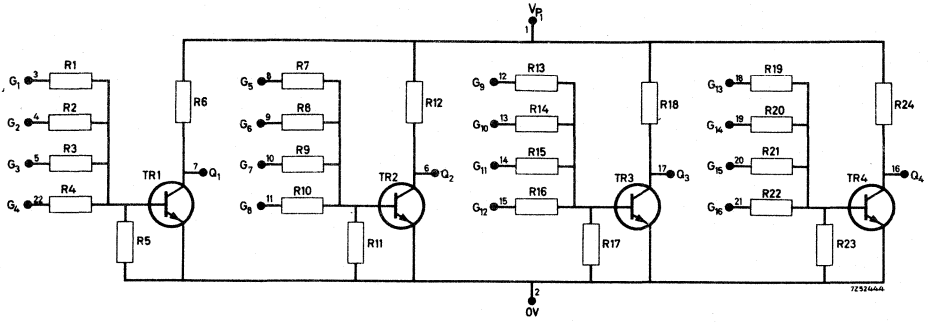
$G_1(G_5, G_9, G_{13})$	$G_2(G_6, G_{10}, G_{14})$	$Q_1(Q_2, Q_3, Q_4)$
H	H	L
H	L	L
L	H	L
L	L	H

All inputs G of a NOR must be LOW or floating for Q is HIGH.

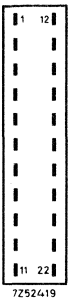


Drawing symbol

CIRCUIT DATA



Terminal location



1 = V_{p1}	= +24V supply	12 = G_9	= input NOR 3
2 = 0	= common 0 V	13 = G_{10}	= input NOR 3
3 = G_1	= input NOR 1	14 = G_{11}	= input NOR 3
4 = G_2	= input NOR 1	15 = G_{12}	= input NOR 3
5 = G_3	= input NOR 1	16 = Q_4	= output NOR 4
6 = Q_2	= output NOR 2	17 = Q_3	= output NOR 3
7 = Q_1	= output NOR 1	18 = G_{13}	= input NOR 4
8 = G_5	= input NOR 2	19 = G_{14}	= input NOR 4
9 = G_6	= input NOR 2	20 = G_{15}	= input NOR 4
10 = G_7	= input NOR 2	21 = G_{16}	= input NOR 4
11 = G_8	= input NOR 2	22 = G_4	= input NOR 1

Power supply

Voltage	V_{p1} = 24 V ± 10%
Current	I_{p1} = 8 mA

INPUT DATA

Input HIGH: V_G = 0.62 V_{P1} to V_{P1}

I_G = 0.17 mA (V_G = 13.4 V); EQUALS ONE D.U.*)

Noise immunity: a voltage shift of 2 V on the minimum high level will not cause a change of the output voltage.

Input LOW: V_G = 0 to 0.3 V

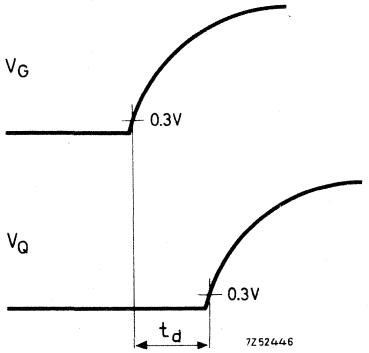
Noise immunity: a voltage of +1 V with respect to the 0 V line applied to any one G input (the other inputs at low level or floating) will not cause a change of the output voltage. The noise immunity can be increased by connecting unused inputs to 0 V.

OUTPUT DATA

Output current: I_Q = 1.02 mA (V_Q = 13.4 V); EQUALS SIX D.U.*)

Time data

Delay, measured over two stages: t_d = max. 12 μs
The delay is specified for Cw = 200 pF and worst input- and output conditions.



*) See also loading table.

PULSE SHAPER AND RESET UNIT

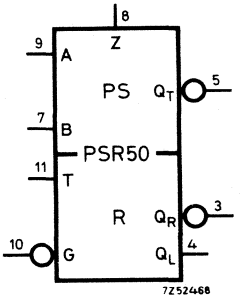
Function

Pulse shaper for converting input signals into counting pulses for the NIC50 and the RIC50, and

reset unit for generating pulses for resetting the NIC50 and the RIC50,
generating pulses for resetting memories formed by cross-connected 4 input NOR's,
generating transfer pulses for the MID50.

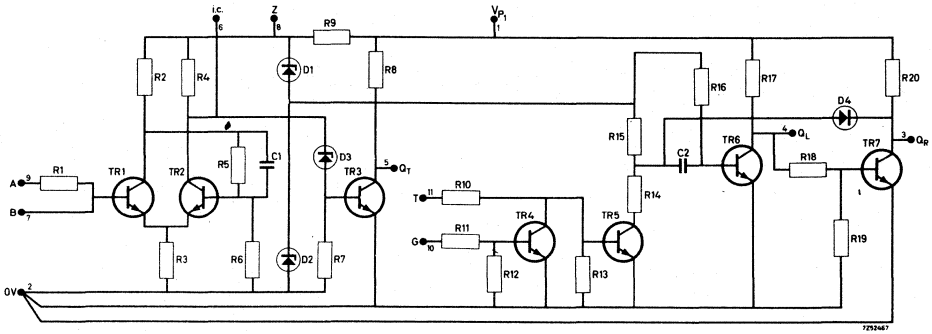
DESCRIPTION

The unit PSR50 contains a pulse shaper and a reset unit. The pulse shaper circuit consists of a Schmitt trigger followed by an inverting amplifier.
The circuit of the reset unit is a monostable multivibrator with one condition input and one trigger input.

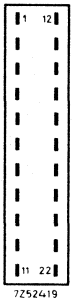


Drawing symbol

CIRCUIT DIAGRAM



Terminal location



1 = V_{p_1} = +24 V supply
2 = 0 = common 0 V
3 = Q_R = counter reset output
4 = Q_L = logic reset output
5 = Q_T = pulse shaper output
6 = internally connected
7 = B = direct base input pulse shaper
8 = Z = internally connected
9 = A = resistor input pulse shaper
10 = G = gate input reset unit
11 = T = trigger input reset unit
12 to 22 = not provided

Power supply

Voltage V_{p_1} = +24 V ± 10%

Current I_{p_1} = 23 mA nominal

PULSE SHAPER

A HIGH level at input B (terminal 7) produces a LOW level at output Q_T (terminal 5), a LOW level at input B produces a HIGH level at output Q_T.

The pulse shaper can be used as follows:

- as a pulse shaper driven by an external source (input transducers)
- as a pulse shaper driven by NOR's of the 50- or 60-Series
- in a relaxation oscillator circuit

INPUT DATA

Pulse shaper driven by an external source

The input voltage has to be applied to B (terminal 7).

HIGH level (operating)

Voltage	V_B = min. 4.0 V
Current	I_B = max. 0.06 mA

LOW level (operating)

Voltage	V_B = max. +1.36 V

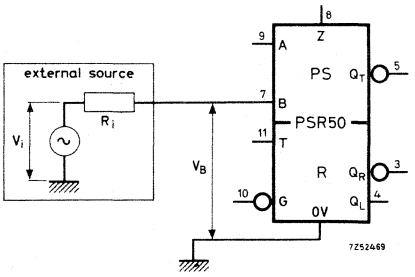
Limiting values

Voltage	V_B = max. +7.0 V min. −2 V
Current	I_B = max. 16 mA

Internal resistance of the driving external source

R_i = max. 33 kΩ

Hysteresis (difference between ON and OFF thresholds)



The hysteresis is affected by the R_i of the external source.
The relation is given by the following formula:

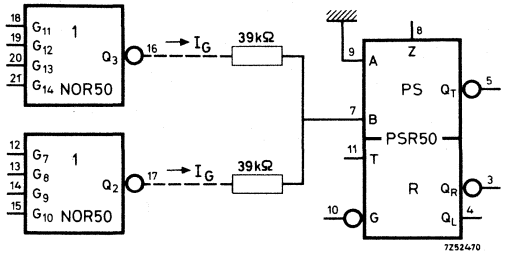
$$\Delta V_i = \text{min. } (1.5 - 0.0455\ R_i)\ V$$

$$\Delta V_B = \frac{\Delta V_i}{1 + 0.046\ R_i}\ V$$

R_i in kΩ and V in volt

Pulse shaper driven by a standard NOR

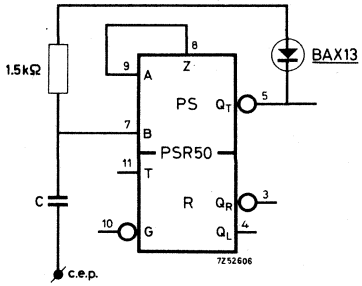
A (terminal 9) has to be connected to 0 (terminal 2).
The input voltage has to be applied to B (terminal 7), via a resistor of 39 kΩ (nominal).
I_G = max. 0.34 mA; EQUALS TWO D.U.*)



The maximum number of driving NOR's is two as shown in the diagram above.

Pulse shaper used in a relaxation oscillator circuit

For this application the connections must be made as shown in the circuitry below.



OUTPUT DATA

Available output suitable for driving three decade counters NIC50 or RIC50 simultaneously

Output voltage LOW

Voltage	V_{QT} = max. 0.5 V
Direct current	I_{QT} = max. 25 mA (V_{QT} = 0.5 V) max. 10 mA (V_{QT} = 0.3 V)
Transient charge	Q_{QT} = max. 30 nC
Wiring capacitance at Q_T	C_W = max. 200 pF

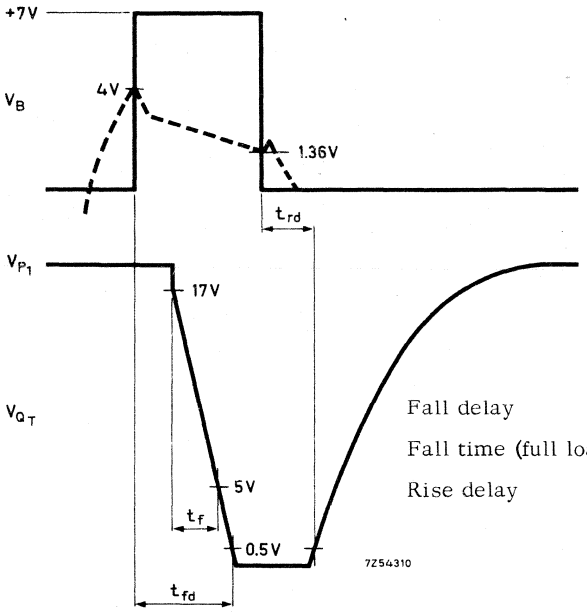
*) See also loading table.

Output voltage HIGH

Voltage	V_{QT} =	0.62 V_{p1} to V_{p1}
Direct current	$-I_{QT}$ =	max. 0.34 mA; EQUALS TWO D.U.*)

Wiring capacitance C_W = max. 200 pF

Time data (when the PSR50 is used in combination with 50-Series units)



Fall delay	t_{fd}	= max.	2 μs
Fall time (full load)	t_f	= max.	1 μs
Rise delay	t_{rd}	= max.	2 μs

RESET UNIT

Reset pulses are only generated when:

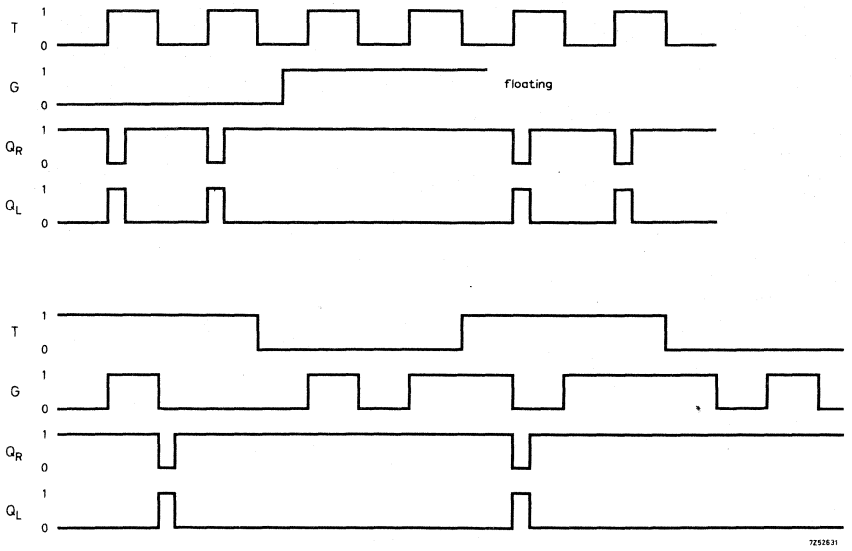
the HIGH level is applied to the trigger input T (terminal 11), and
the gate input G (terminal 10) is kept at the LOW level or left floating.

The unit generates two reset pulses simultaneously, namely:

from the logic reset output Q_L (terminal 4) for resetting d.c. memories built with NOR's
from the counter reset output Q_R (terminal 3) for resetting decade counters NIC50 and RIC50.

Note - A reset pulse is also generated when the G-input changes from the HIGH to the LOW level, whilst the T-input is at the HIGH level.

*) See also loading table.



INPUT DATA

Input HIGH

Voltage	$V_{T(G)}$ = 0.62 V_{P_1} to V_{P_1}
limiting value	$V_{T(G)}$ = +100 V
Current	$I_{T(G)}$ = 0.17 mA ($V_{T(G)}$ = 13.4 V); EQUALS ONE D.U.*)

Noise immunity: a voltage shift of 2 V on minimum HIGH level will not cause a change of the output voltage.

Input LOW

Voltage	$V_{T(G)}$ = max. 0.3 V
limiting value	$V_{T(G)}$ = −15 V

Noise immunity: a voltage of +1.25 V with respect to the 0 V terminal applied to either the T- or the G-input will not cause a change of the output voltage.

OUTPUT DATA

Output Q_L: capable of driving max. 4NOR's; EQUALS FOUR D.U.*)

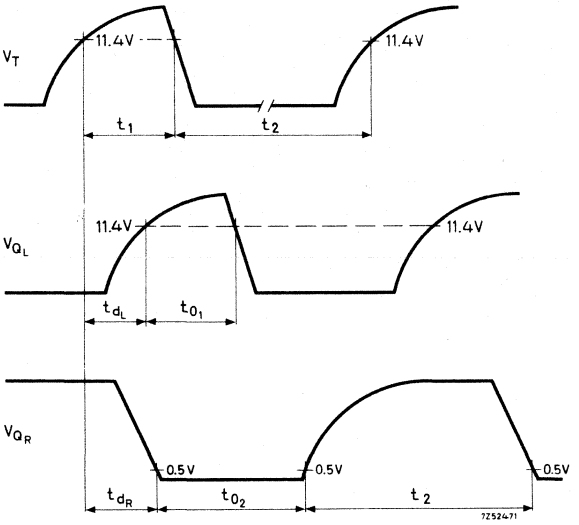
Voltage	V_{QL} = min. 0.53 V_{P_1}
Direct current	$-I_{QL}$ = max. 0.55 mA (V_{QL} = 11.4 V)

*) See also loading table.

Output Q_R: capable of driving the reset input of 6 decade counters NIC50 or RIC50 simultaneously

Voltage	V_{QR} = max. 0.5 V
Direct current	I_{QR} = max. 51 mA
Wiring capacitance	C_w = max. 200 pF at Q_R and Q_L

Time data



Input pulse duration	t_1	= min. 20 μs
Recovery time *)	t_2	= min. 20 μs
Output pulse duration	t_{0_1}	= min. 15 μs max. 45 μs
	t_{0_2}	= min. 15 μs max. 50 μs
Delay between V_T and V_{Q_L}	t_{d_L}	= max. 3 μs
Delay between V_T and V_{Q_R}	t_{d_R}	= max. 7 μs
Rise time at T	t_r	= max. 100 μs (between 0.5 V and 11.4 V)
Fall time at G	t_f	= max. 100 μs (between 11.4 V and 0.5 V)

*) The recovery time starts at the trailing edge of V_T when $t_1 > t_{0_2}$ or starts at the trailing edge of V_{Q_R} when $t_{0_2} > t_1$.

LAMP/RELAY DRIVER

Function — Low-power amplifier for driving lamps and relays

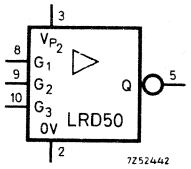
DESCRIPTION

The circuit consists of an inverting amplifier preceded by a 3 input OR-gate.
The load has to be connected between output Q and the unstabilised +24 V supply voltage (abs. max. 30 V).
The load is energised when one or more inputs are HIGH (Q is LOW).
The output transistor is protected against voltage transients which occur when inductive loads are driven.

Simplified truth table:

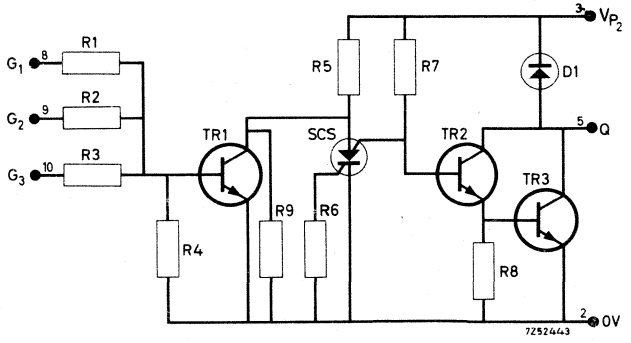
G_1	G_2	Q
H	H	L
H	L	L
L	H	L
L	L	H

All inputs G must be LOW or floating for Q is HIGH.

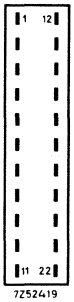


Drawing symbol

CIRCUIT DATA



Terminal location



1 = not provided
2 = 0 = common 0 V
3 = V_{p_2} = +24 V supply
4 = not provided
5 = Q = output
6 = not provided
7 = not provided
8 = G_1 = input
9 = G_2 = input
10 = G_3 = input
11 = not provided
12 to 22 = not provided

Power supply

Voltage	V_{p_2} = +24 V ±25%
Current	I_{p_2} = (4.4 + I_Q) mA

INPUT DATA

Output transistor ON

Input HIGH: : V_G = 0.62 V_{p_1} to V_{p_1}
I_G = max. 0.17 mA (V_G = 13.4 V); EQUALS ONE D.U.*)

Noise immunity: A voltage shift of 2 V on the minimum high level will not cause a change of the output voltage.

Output transistor OFF

Input LOW : V_G = max. 0.3 V

Noise immunity: A voltage of 1.25 V with respect to the 0 V line applied to any one input (other inputs at low level or floating) will not cause a change of the output voltage. The noise immunity can be increased by connecting unused inputs to 0 V.

OUTPUT DATA

Output transistor ON

I_Q = abs. max. 300 mA ($V_Q \leq$ 1.6 V)

Output transistor OFF

I_Q = max. 0.5 mA at V_Q = abs. max. 30 V.

*) See also loading table.

PRINTER DRIVE UNIT

Function — Intermediate stages to drive decimal input printers

DESCRIPTION

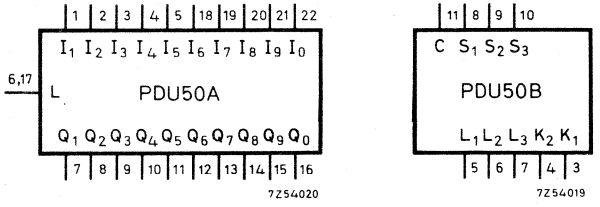
With the units PDU50A and PDU50B a complete printer drive circuit is formed. This circuit is intended to be used in combination with the NIC50, RIC50 or MID50 and a printer which requires decimal information at its inputs. A diagram for driving such a printer is given on the next page. One PDU50A unit, which contains ten inverter stages, must be used per decade.

The ten decimal inputs I_0 to I_9 can be connected directly to the ten corresponding outputs Q_0 to Q_9 of either the uni-directional decade counter NIC50 or the bi-directional decade counter RIC50 or the buffer memory MID50.

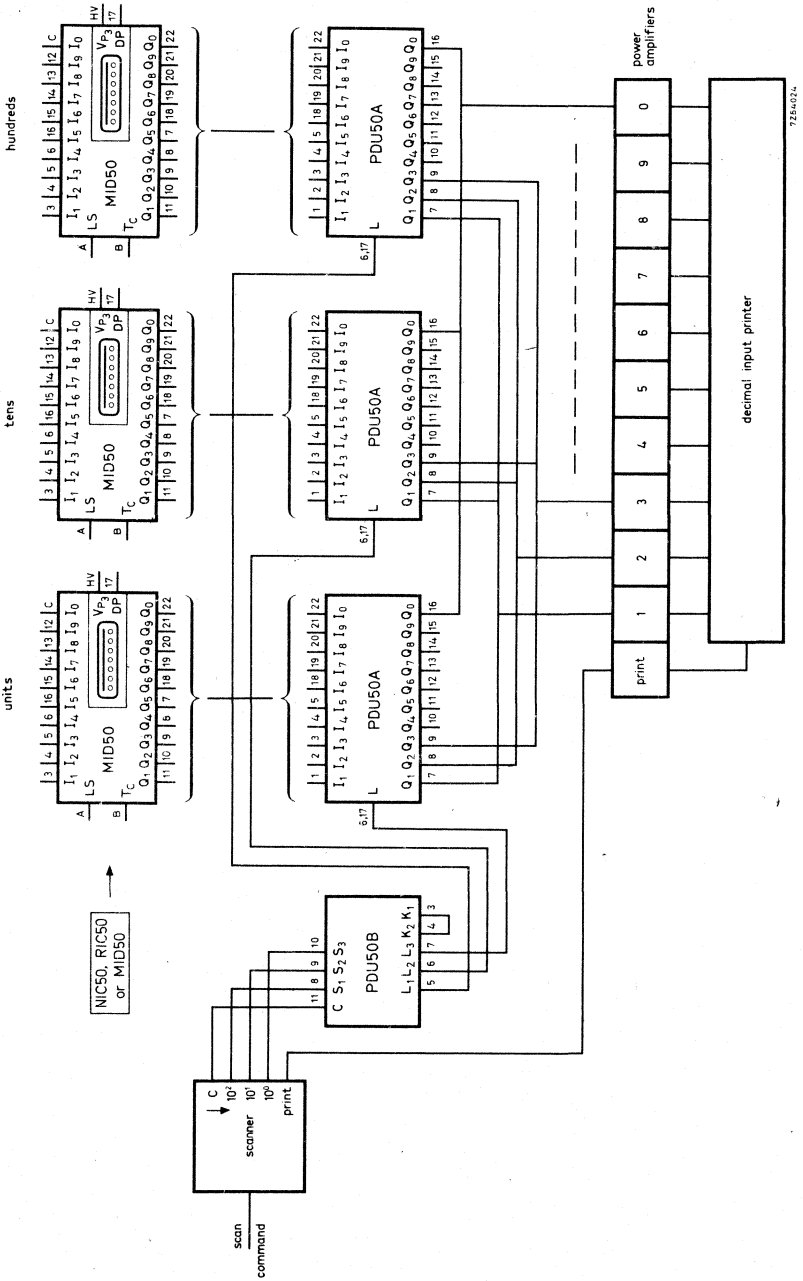
When a positive voltage is applied to control input L, that particular output Q will become HIGH, which has a LOW level at its input.

The PDU50B contains one clock control and three scan control circuits suitable to operate with a three decade counting system.

When simultaneously both the clock control input C and one of the scan control inputs S_1 to S_3 are at LOW level a positive voltage is available at the corresponding control output L_1 to L_3 of the PDU50B. Each control output of the PDU50B is connected to the control input L of the PDU50A.



Drawing symbols


hundreds
tens
units
MID50
LS
PDU50A
PDU50B
NIC50, RIC50 or MID50
power amplifiers
decimal input printer
print
scanner
scan command
7254024

Summarising the functions of the PDU50A and PDU50B it becomes clear that a particular output Q of the PDU50A is at a HIGH level only, when the three following conditions are fulfilled:

- the corresponding input I of the PDU50A at a LOW level,
- the clock control input C of the PDU50B at a LOW level,
- the corresponding scan control input S_1 to S_3 of the PDU50B at a LOW level.

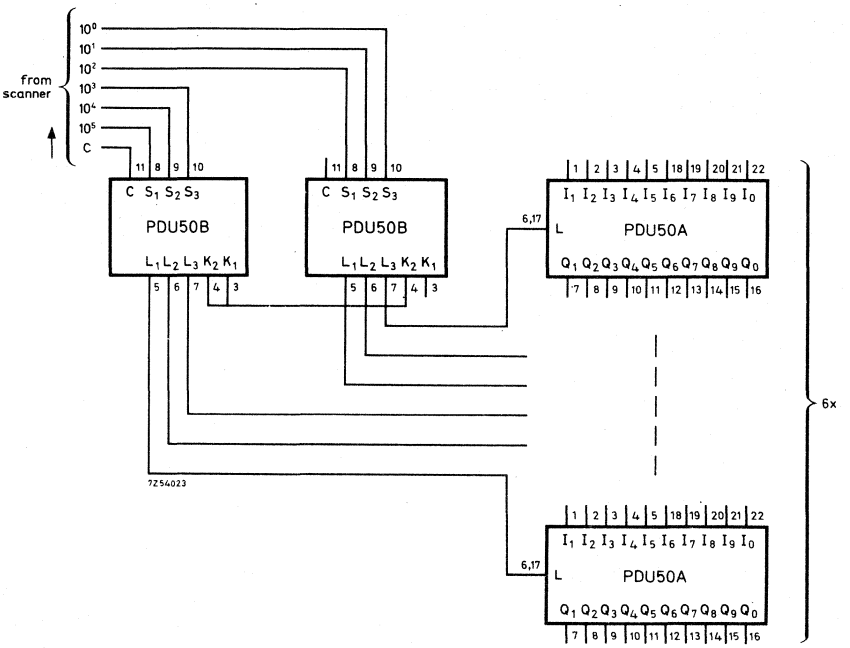
Note that only one output Q of the PDU50A is HIGH at a time as shown in the truth table below.

Truth table:

inputs			output
PDU50B		PDU50A	
C	S	I	Q
H	H	H	L
L	H	H	L
H	L	H	L
L	L	H	L
H	H	L	L
L	H	L	L
H	L	L	L
L	L	L	H

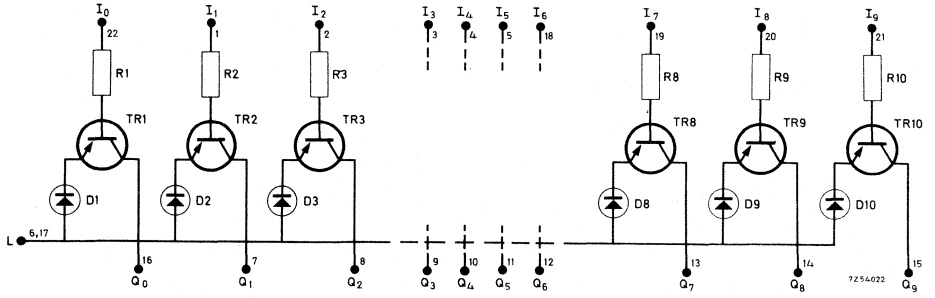
As the positive voltage derived from the PDU50B is fed to terminal L of only one PDU50A at a time it is permissible to common the corresponding outputs of all PDU50A units without any feedback consequences. These ten commoned PDU50A outputs are to be connected to ten power stages, of which the output power depends on the driving input requirements of the decimal input printers, e.g. the LRD50 supplies 300 mA/30V.

The description above holds for systems up to three decades, for which the terminals K_1 and K_2 of the PDU50B have to be interconnected.
When however more than three decades are required another PDU50B unit must be added to the system.
In this case terminals K_1 and K_2 need be interconnected for only one PDU50B.
For the other units PDU50B the terminals K_1 and K_2 are left open.
An interconnection diagram is given on the next page.

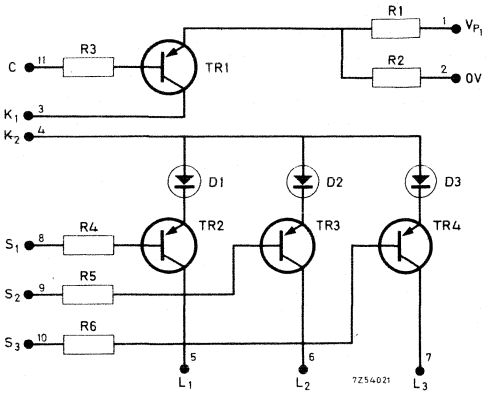


Note - When the input signal for the PDU50A is obtained from a MID50 unit either the clock pulse input C or all the scan inputs of the PDU50B must be at the HIGH level during the time the shift pulse input T_C of the MID50 is at the LOW level.

CIRCUIT DATA



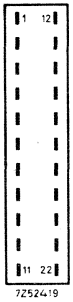
PDU50A



PDU50B

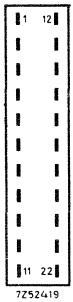
Terminal location

PDU50A



1 = I_1 = decimal input 1
2 = I_2 = decimal input 2
3 = I_3 = decimal input 3
4 = I_4 = decimal input 4
5 = I_5 = decimal input 5
6 = L = control input
7 = Q_1 = decimal output 1
8 = Q_2 = decimal output 2
9 = Q_3 = decimal output 3
10 = Q_4 = decimal output 4
11 = Q_5 = decimal output 5
12 = Q_6 = decimal output 6
13 = Q_7 = decimal output 7
14 = Q_8 = decimal output 8
15 = Q_9 = decimal output 9
16 = Q_0 = decimal output 0
17 = L = interconnected with 6
18 = I_6 = decimal input 6
19 = I_7 = decimal input 7
20 = I_8 = decimal input 8
21 = I_9 = decimal input 9
22 = I_0 = decimal input 0

PDU50B



1 = V_{p_1} = +24 V supply
2 = 0 = common 0 V
3 = K_1 = interconnecting point
4 = K_2 = interconnecting point
5 = L_1 = control output 1
6 = L_2 = control output 2
7 = L_3 = control output 3
8 = S_1 = scan control input 1
9 = S_2 = scan control input 2
10 = S_3 = scan control input 3
11 = C = clock control input
12 to 22 = not provided

Power supply PDU50B

Voltage V_{p_1} = 24 V ± 10%

Current I_{p_1} = 1 mA

INPUT DATA

PDU50A

Decimal inputs I_0 to I_9

These inputs are to be driven from decimal outputs Q_0 to Q_9 of either NIC50, RIC50 or MID50.
By applying a suitable, positive voltage to input L derived from output L_1, L_2 or L_3 of the PDU50B, that output Q becomes HIGH which has a LOW level at its input.

Voltage LOW:
V_I = max. 5 V
I_I = max. 35 μA

Voltage HIGH:
V_I = min. 0.8 V_{p_1}

PDU50B

Clock control input C (terminal 11)

Voltage LOW:
V_C = max. 5 V
I_C = max. 35 μA

Voltage HIGH:
V_C = min. 0.9 V_{p_1}

Scan control inputs S_1, S_2, S_3 (terminals 8, 9, 10)

Voltage LOW:
V_S = max. 5 V
I_S = max. 35 μA

Voltage HIGH:
V_S = min. 0.9 V_{p_1}

OUTPUT DATA

PDU50A

Output voltage LOW:
V_Q = max. 0.3 V

Output voltage HIGH:
I_Q = max. 0.34 mA (V_Q = 13.4 V); EQUALS TWO D.U.

PDU50B

Available output at the HIGH and LOW level (terminals L_1 to L_3) are adapted to the input requirements of the input terminal L of units PDU50A.

DECADE COUNTER AND DIVIDER

Function	Divider of 2, 3, 4, 5, 6, 8, 9, 10, 12 and 16
Ambient temperature range	
operating	−25 to +70 °C (at V_P = 24 V ±10%) −10 to +70 °C (at V_P = 24 V ±25%)
storage	−40 to +85 °C

DESCRIPTION

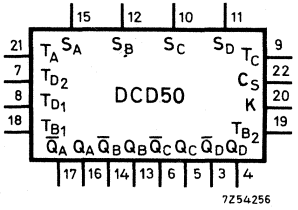
The DCD50 consists of four flip-flops. By correctly interconnecting the terminals a divider of 2, 3, 4, 5, 6, 8, 9, 10, 12 or 16 can be obtained. Each flip-flop is driven by a positive-going pulse. The flip-flops have one common reset input and four separate preset inputs, their condition being governed by a positive-going pulse applied to the appropriate terminal(s). When setting or presetting the DCD50 one sometimes has to apply a HIGH level signal to one of the trigger inputs of the second flip-flop (input K, via a diode).

Truth table (decade counter configuration):

	FF-A	FF-B	FF-C	FF-D
pulse	$\overline{Q_A}$	$\overline{Q_B}$	$\overline{Q_C}$	$\overline{Q_D}$
initial state	1	1	1	1
1	0	1	1	1
2	1	0	1	1
3	0	0	1	1
4	1	1	0	1
5	0	1	0	1
6	1	0	0	1
7	0	0	0	1
8	1	1	1	0
9	0	1	1	0

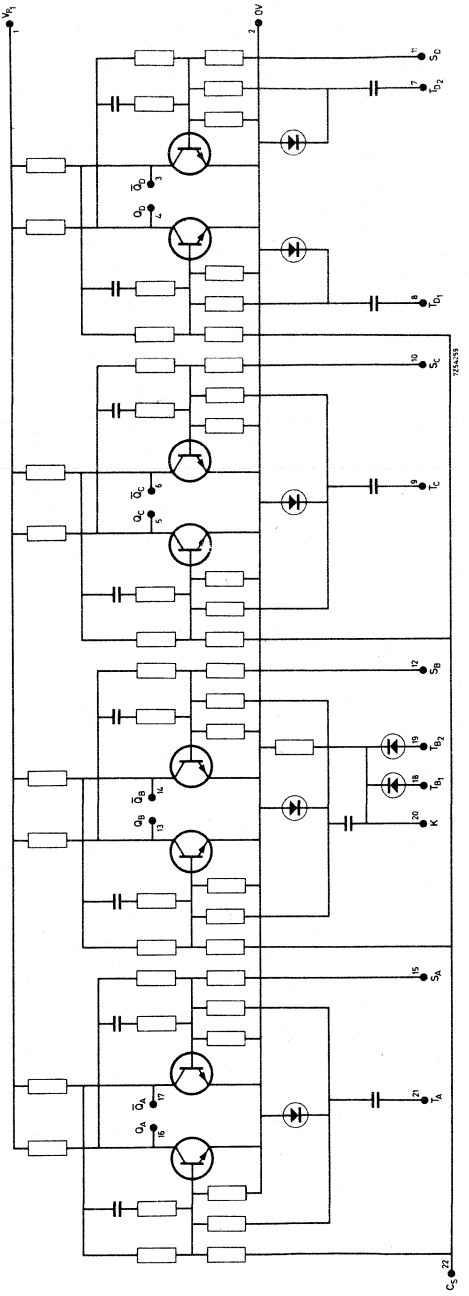
The table below shows the interconnections to be made externally for the various dividers:

divider	input	interconnection	output
2	8	7-8	$\overline{Q_D}$
	9	–	$\overline{Q_C}$
	18	–	$\overline{Q_B}$
	21	–	$\overline{Q_A}$
3	18	4-19, 7-14, 8-18	$\overline{Q_D}$
4	9	6-7-8	$\overline{Q_D}$
	21	17-18	$\overline{Q_B}$
5	18	4-19, 6-7, 8-18, 9-14	$\overline{Q_D}$
6	21	4-19, 7-14, 8-17-18	$\overline{Q_D}$
8	21	6-7-8, 9-17	$\overline{Q_D}$
9	18	4-19, 6-7, 8-18, 9-17, 14-21	$\overline{Q_D}$
10	21	4-19, 6-7, 8-17-18, 9-14	$\overline{Q_D}$
12	9	4-19, 6-21, 7-14, 8-17-18	$\overline{Q_D}$
16	21	6-7-8, 9-14, 17-18	$\overline{Q_D}$

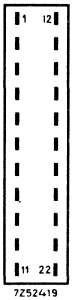


Drawing symbol

CIRCUIT DIAGRAM



Terminal location



1 = V_{p_1} = +24 V supply
2 = 0 = common 0 V
3 = $\overline{Q_D}$ = output $\overline{Q}$ of flip-flop D
4 = Q_D = output Q of flip-flop D
5 = Q_C = output Q of flip-flop C
6 = $\overline{Q_C}$ = output $\overline{Q}$ of flip-flop C
7 = T_{D2} = trigger input T of flip-flop D
8 = T_{D1} = trigger input T of flip-flop D
9 = T_C = trigger input T of flip-flop C
10 = S_C = preset input of flip-flop C
11 = S_D = preset input of flip-flop D
12 = S_B = preset input of flip-flop B
13 = Q_B = output Q of flip-flop B
14 = $\overline{Q_B}$ = output $\overline{Q}$ of flip-flop B
15 = S_A = preset input of flip-flop A
16 = Q_A = output Q of flip-flop A
17 = $\overline{Q_A}$ = output $\overline{Q}$ of flip-flop A
18 = T_{B1} = trigger input T of flip-flop B
19 = T_{B2} = trigger input T of flip-flop B
20 = K = extender input of flip-flop B
21 = T_A = trigger input T of flip-flop A
22 = C_S = common reset input

Power supply

Voltage: V_{p_1} = +24 V ±10% (at T_{amb} = −25 to +70 °C)
V_{p_1} = +24 V ±25% (at T_{amb} = −10 to +70 °C)

Current: I_{p_1} = 25 mA nominal

INPUT DATA

Trigger inputs T_A, T_{B1}, T_{B2}, T_C, T_{D1} and T_{D2} (terminals 21, 18, 19, 9, 8 and 7)

The trigger inputs require a positive-going pulse.

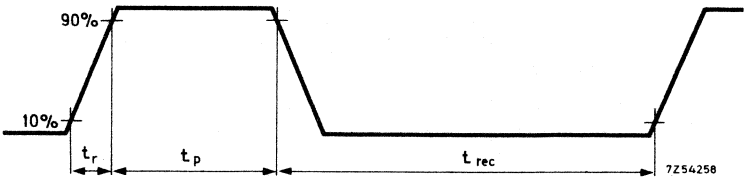
From another DCD50

	V_{p_1} = 24 V ±10%	V_{p_1} = 24 V ±25%
Triggering edge	from 0.3 V to 0.7 V_{p_1}	from 0.3 V to 0.8 V_{p_1}
Wiring capacitance C_w	C_w = max. 150 pF	

From a PSR50 (output Q_T) or from a NOR unit

	V_{p_1} = 24 V ±10%	V_{p_1} = 24 V ±25%
Triggering edge	from 0.3 V to 0.91 V_{p_1}	from 0.3 V to 0.83 V_{p_1}
Permissible load at output of driving unit	max. 1 D.U.	max. 2 D.U.
Wiring capacitance C_w	max. 150 pF	max. 50 pF

Time data



Fall time of negative-going input pulse to NOR-unit	t_f	= max.	2 μs
Rise time of input pulse to trigger input T of DCD50 from another unit than those mentioned above	t_r	= max.	1 μs
Pulse duration	t_p	= min.	4 μs
Recovery time for inputs T_A, T_C, T_{D1}, T_{D2}	t_{rec}	= min.	10 μs
	t_p+t_{rec}	= min.	30 μs
for inputs T_{B1}, T_{B2}	t_{rec}	= min.	80 μs, required at input: 1 D.U.
	t_{rec}	= min.	40 μs, with external resistor of 82 kΩ between K and 0; required at input: 2 D.U.
	t_{rec}	= min.	27.5 μs, with external resistor of 43 kΩ between K and 0; required at input: 3 D.U.

Noise margin 1.5 V

Common reset input C_S (terminal 22) and preset inputs S_A, S_B, S_C and S_D (terminals 15, 12, 10 and 11)

Voltage LOW

V_S
V_{CS} = max. 0.3 V

Voltage HIGH

V_S
V_{CS} = min. 0.62 V_{P1}

I_S = min. 0.24 mA (V_S = 13.4 V); EQUALS 1.5 D.U.

I_{CS} = min. 0.96 mA (V_{CS} = 13.4 V); EQUALS 6 D.U.

Resetting

When a DCD50 is used as a divider of 3, 5 or 9 an inhibit pulse (HIGH level) must be applied to K (terminal 20) via a diode type BAX13 (cathode to K).

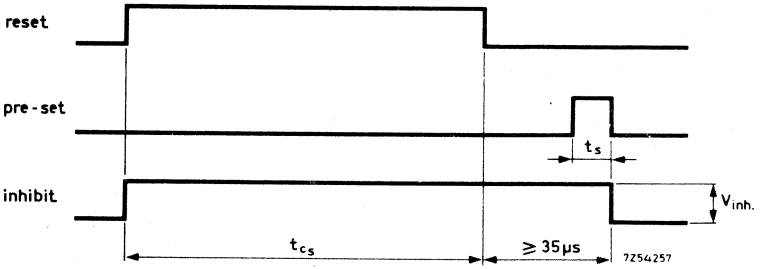
Presetting

When a DCD50 is used as a divider of 3, 5 or 9 and presetting via S_D (terminal 11) is required, an inhibit pulse must be applied to K (terminal 20) via a diode BAX13 (cathode to K).

When a DCD50 is used as divider of 6, 10 and 12 and presetting via S_A and S_D (terminals 15 and 11) is required, an inhibit pulse must be applied to K (terminal 20) via a diode BAX13 (cathode to K).

Time data

The reset pulse and the preset pulse must not be applied at the same time.



Reset pulse duration	t_{cs} = min. 20 µs per flip-flop
Preset pulse duration	t_s = min. 5 µs
Time delay between reset (preset) pulse and trigger input signal	t_{r-t} = min. 30 µs
Time delay between end of reset pulse and end of preset pulse	t_{r-p} = min. 35 µs

Inhibit pulse:

Voltage HIGH: $V_{inh} \geq V_{TB1\ (TB2)} - 1.5\ V$

When inhibit pulses are applied the total reset time in a chain of dividers, built with the DCD50, can be reduced to t = (n + 1) 20 µs, where n = maximum number of flip-flops between two inhibited flip-flops.

OUTPUT DATA

The outputs of the four flip-flops are Q_A, $\overline{Q_A}$, Q_B, $\overline{Q_B}$, Q_C, $\overline{Q_C}$, Q_D and $\overline{Q_D}$.

Voltage LOW

V_Q = max. 0.3 V

Voltage HIGH

	V_{p1} = 24 V ± 10%	V_{p1} = 24 V ± 25%
Loadability	6 D.U.	4 D.U.

Loadability at V_{p1} = 24 V ± 10%

- Each output can be loaded with one trigger input of a NIC50.
- The outputs Q_A, Q_B, $\overline{Q_B}$, Q_C and $\overline{Q_C}$ can be loaded with 6 D.U. plus one trigger input of a next DCD50 (except T_{B_1}, and T_{B_2}) or with 4 D.U. plus one base input of a PSR50.
- For further output data and maximum pulse repetition frequency, see table on next page.

Wiring capacitance at each output: C_W = max. 150 pF

Note - For proper inhibiting of the trigger gate of the second flip-flop in the DCD50 the load at the inhibiting output must not exceed the load at the trigger input by more than 2 D.U.

divider of	input		max. p.r.f. (kHz)			available output (D.U.)							
	terminal	required (D.U.)	without resistor *) **)	with 43 kΩ *) **)	with 82 kΩ *) **)	Q_A	$\overline{Q_A}$	Q_B	$\overline{Q_B}$	Q_C	$\overline{Q_C}$	Q_D	$\overline{Q_D}$
2	21	–	30			6	6						
	9	–	30							6	6		
	7-8	–	30									6	6
	18	3		30 18				6	6				
		2			22 12.5			6	6				
		1	12 6					6	6				
3	8-18	3		30 18				6	6			3	6
		2			22 12.5			6	6			4	6
		1	12 6					6	6			5	6
4	9	–	30							6	6	6	6
	21	–		30		6	3	6	6				
					24	6	4	6	6				
			12			6	5	6	6				
5	8-18	3		30 18				6	6	6	6	3	6
		2			22 12.5			6	6	6	6	4	6
		1	12 6					6	6	6	6	5	6
6	21	–		30		6	3	6	6			3	6
					24	6	4	6	6			4	6
			12			6	5	6	6			5	6
8	21	–	30			6	6			6	6	6	6
9	8-18	3		30 18		6	6	6	6	6	6	3	6
		2			22 12.5	6	6	6	6	6	6	4	6
		1	12 6			6	6	6	6	6	6	5	6
10	21	–		30		6	3	6	6	6	6	3	6
					24	6	4	6	6	6	6	4	6
			12			6	5	6	6	6	6	5	6
12	9	–			30	6	4	6	6	6	6	4	6
			24			6	5	6	6	6	6	5	6
16	21	–	30***)			6	6	6	6	6	6	6	5
				30		6	3	6	6	6	6	6	6
					24	6	4	6	6	6	6	6	6
			12			6	5	6	6	6	6	6	6

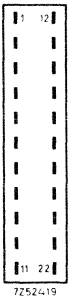
*) Input pulses according to "Time data".
**) Input pulses with $\frac{1}{2}$ T wave form.
***) Second flip-flop (B) is last in chain.

Preset switch

For decoding the DCD50 in preset programmed counting systems use has to be made of the decoding switch 1248N, catalogue number 4311 027 82221.

Note that:

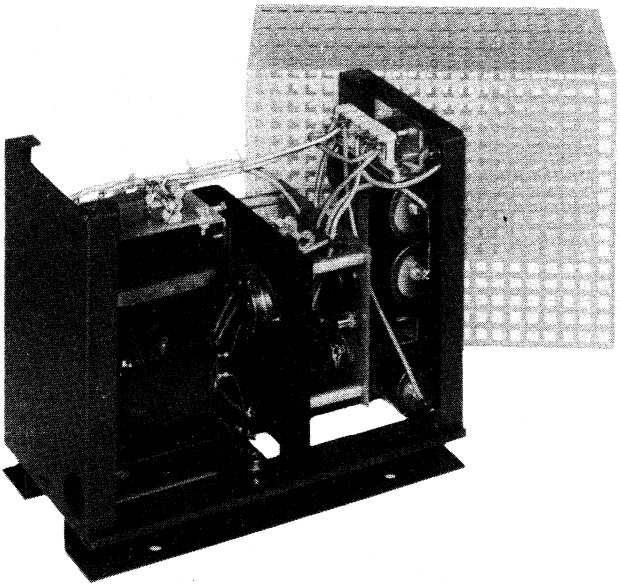
- the outputs of the DCD50 have to be connected to the switch inputs as given below
- the internal resistance of the switch (terminal 12) has to be left floating.



1 = not connected	12 = floating
2 = not connected	13 = not connected
3 = not connected	14 = not connected
4 = $\overline{Q_D}$	15 = $\overline{Q_A}$
5 = Q_D	16 = Q_A
6 = output (pole)	17 = output (pole)
7 = Q_B	18 = Q_C
8 = $\overline{Q_B}$	19 = $\overline{Q_C}$
9 = not connected	20 = not connected
10 = not connected	21 = not connected
11 = not connected	22 = not connected

Note - The output (pole) of the decoding switch may directly be connected to one of the inputs of a NOR in the 4.NOR51 unit.

POWER SUPPLY UNIT
for 50-Series direct display counters



RZ 24599-2

TECHNICAL PERFORMANCE

Operating ambient temperature range	−25 to +65 °C

The unit is provided with a temperature fuse (F1).

Input data

Input voltage	110, 120, 130, 220, 230, 240 V_{ac}, +10%, −15%
Input frequency	45 to 65 Hz

Output data

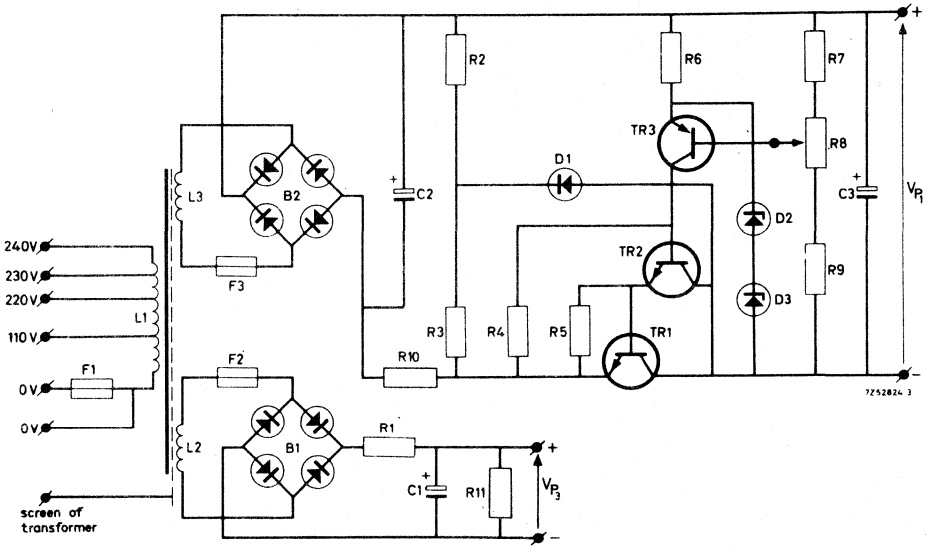
Logic supply (V_{P1})

Output voltage	+24 V ± 5%
Output current	0 to 250 mA
Internal resistance	0.5 Ω
Ripple voltage	10 mV_{rms}
Temperature coefficient	1 mV/deg C (typical value)
Fusing	easy replaceable fuse (630 mA slow, F3)

Provided with automatic short-circuit protection

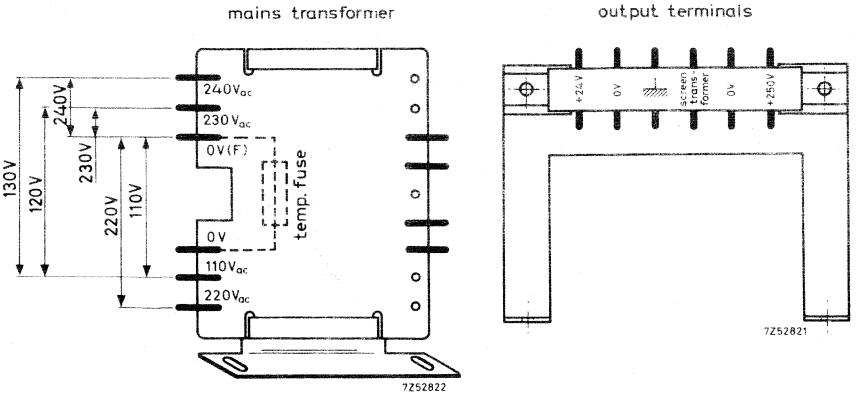
Numerical indicator tube supply (V_{P3})

Output voltage	+250 V ± 18%
Output current	max. 40 mA
Fusing	easy replaceable fuse (100 mA slow, F2)



Circuit diagram

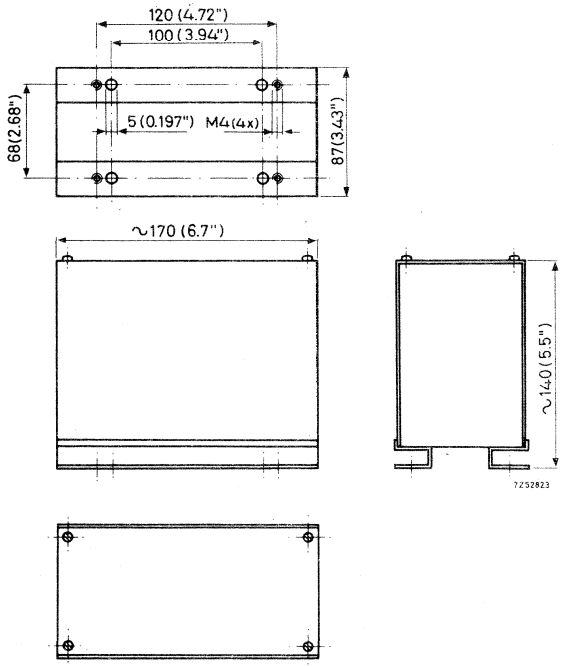
Terminal location



Note - Both input and output terminals are suitable for direct soldered connections.

MECHANICAL DATA

Housing	steel
Cover	perforated steel



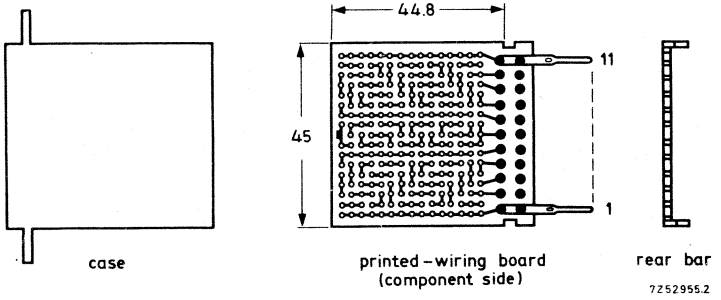
Dimensions in mm, inch values between brackets

EMPTY CASE ASSEMBLY

Function	Empty case assembly for non-standard circuits

DESCRIPTION

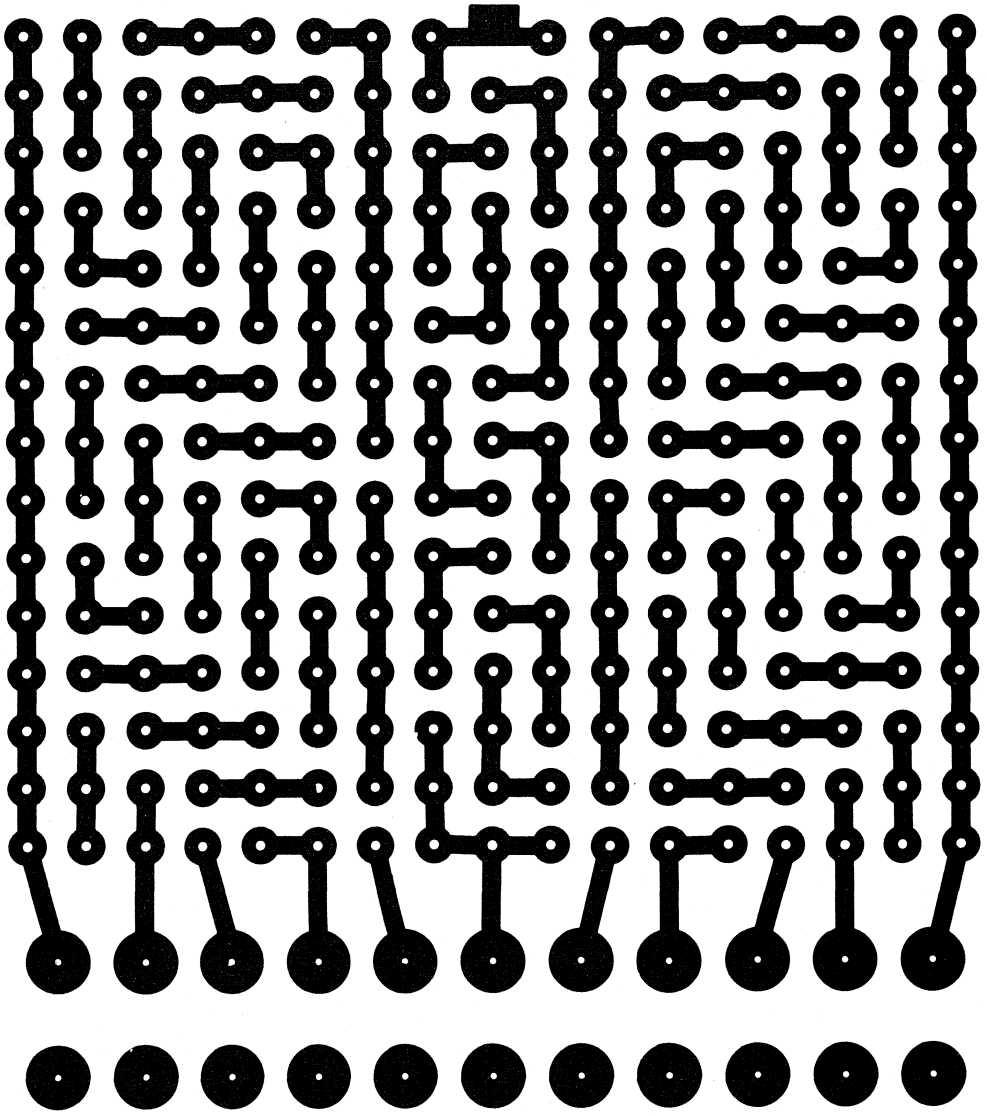
For non-standard circuit configurations an empty case assembly comprising a plastic case, a general purpose printed-wiring board and a rear bar is available in the 50-Series.
With these items non-standard circuits can be built in a technology similar to that of all auxiliary modules in the range.



Dimensions in mm

Printed-wiring board material	glass-epoxy with 254 plated-through holes
hole diameter	$0.8\ ^{+0.2}_{-0.05}$ mm
grid pitch	2.54 mm (0.1 inch)
contacts	11; similar to those of all other 50-Series modules

Note: On the next page the lay-out of the printed wiring (component side) is shown on a scale 3:1, which can be used as an aid for the designer.



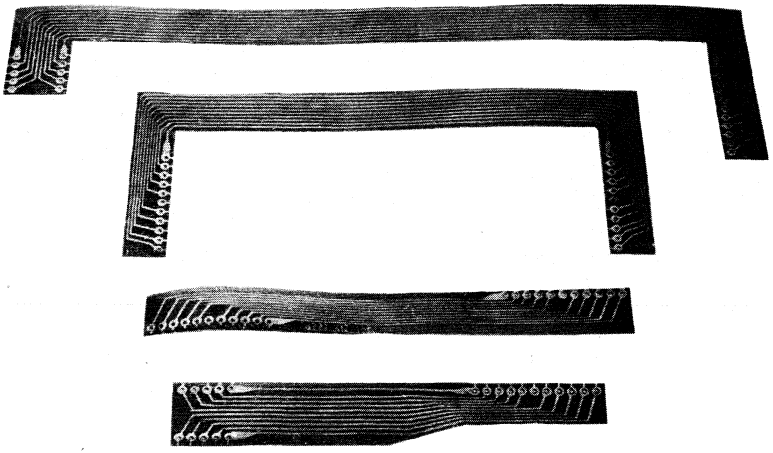
Lay-out of printed wiring (component side); scale 3 : 1

Accessories for counter modules 50-Series

MOUNTING ACCESSORIES

For mounting accessories the sections "INTRODUCTION" and "CONSTRUCTION" of 50-Series, General should be consulted.

FLEXIBLE PRINTED WIRING



RZ 28179-3

The use of flexible printed wiring considerably shortens the time required to wire the modules, while allowing a neat and simple construction. Four types are available:

- Type HCS50, catalogue number 8222 412 10291, for interconnecting the ten output terminals of counters NIC50 or RIC50 to the corresponding terminals of the thumbwheel switches, when the modules are mounted on a horizontal axis
- Type HSS50, catalogue number 8222 412 10301, for interconnection between thumbwheel switches mounted on a horizontal axis
- Type VCS50, catalogue number 8222 412 10310 for interconnecting counters NIC50 and RIC50 and the thumbwheel switches, when these modules are mounted on a vertical axis
- Type VSS50, catalogue number 8222 412 10320 for interconnection between thumbwheel switches mounted on a vertical axis.

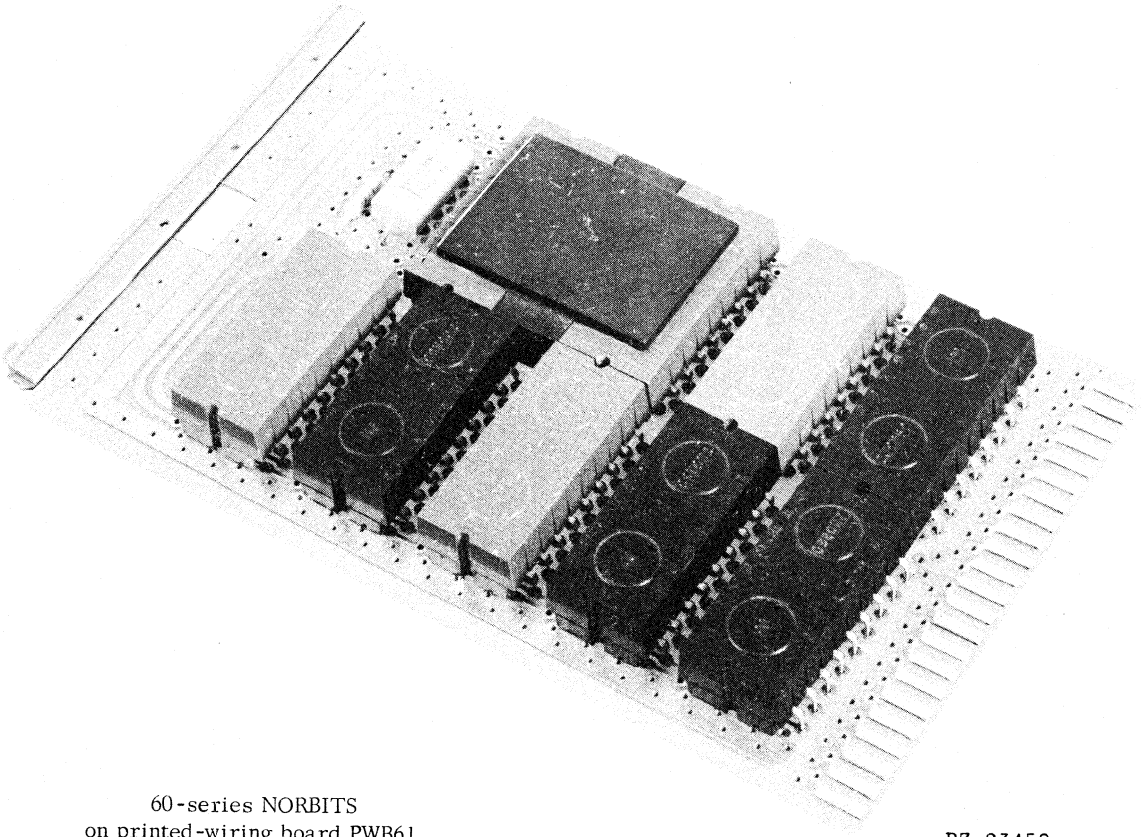
More complex installations, with combinations of vertical and horizontal mounting can be covered with the above four types of flexible printed wiring.

STICKERS

Stickers are drawing symbols of 50-Series modules printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings.
The stickers are available in sheets. Each sticker can be separately detached from the sheet, without cutting.

sheet with modules of type	catalogue number for 50 sheets
NIC50 (4x) + SU50 (8x)	4322 026 70260
LRD50 (3x) + PSR50 (2x) + 3.NOR50 (3x) + 4.NOR51 (2x)	70270
RIC50 (4x) + SU50 (8x)	70430
MID50 (8x) + SID50 (4x)	70440
PDU50A (9x) + PDU50B (3x) DCD50	71910 71920

NORbits 60-Series, 61-Series



60-series NORBITS
on printed-wiring board PWB61

RZ 23458

60-Series NORbits

INTRODUCTION

The 60-Series, which uses NOR logic as a basis of operation, represents an important advance in static switching devices for industrial control systems. It comprises 7 circuit blocks having the following features in common:

- Single rail 24 V ± 25% supply, allowing the use of an inexpensive power supply - which helps to keep the cost down, particularly in small systems.
- Transfer moulded cases, giving optimum protection.
- Rigid terminals spaced at 0,2 in. pitch, permitting a variety of interconnection methods to be used (dip soldering, hand soldering, miniwire wrapping).
- Exceptionally good noise immunity.
- Easy to understand level logic, making it possible to carry out system tests with only a d.c. voltmeter.
- Silicon semiconductors throughout, ensuring reliable operation down to −10 °C and up to +70 °C.
- Low price.

Compatible input and output devices as well as a full range of mounting accessories are available.

The 60-Series comprises the following types:

2.NOR 60	Dual 4-input NOR gate
4.NOR 60	Quadruple 2x2 + 2x3 input NOR gate
2.IA 60	Dual Inverter Amplifier
2.LPA 60	Dual Low Power Amplifier
TU.60	Timer Unit
2.SF 60	Dual input Switch Filter
PA 60	Power Amplifier
HPA60	High Power Amplifier
GLD60	Grounded Load Driver

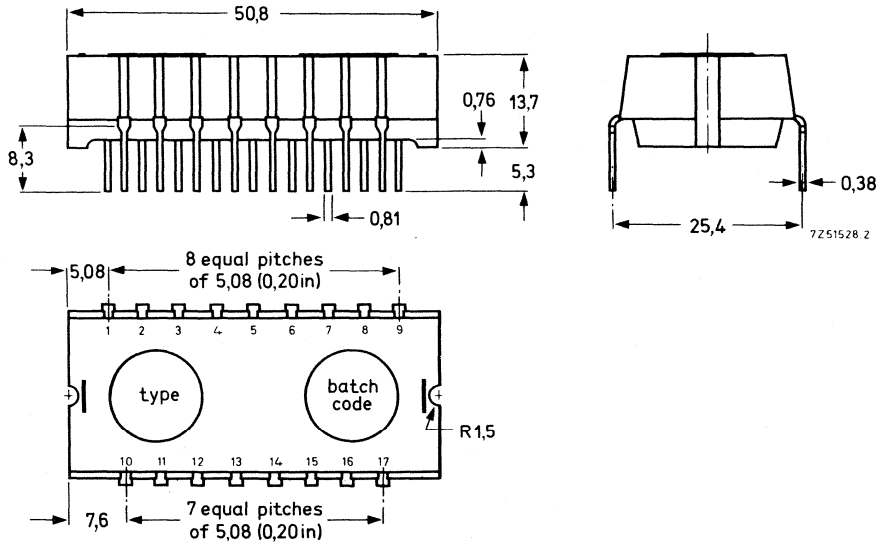
CONSTRUCTION

The circuit elements are housed in a transfer moulded encapsulation. The dimensions are as shown below. The pin connections for each unit are shown on the relevant data sheets. Pin numbering is moulded on both top and bottom of the unit. All pins are also accessible from the top of the unit to facilitate test requirements.

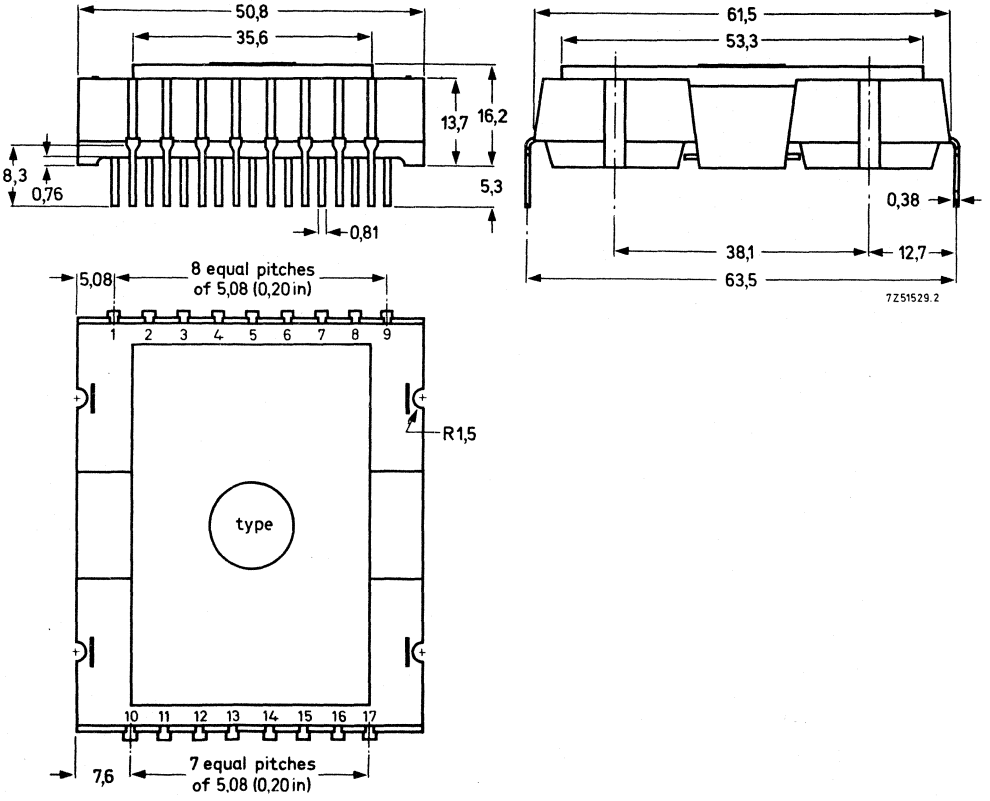
Mounting

The units may be mounted on printed-wiring boards, and a range of these is available with suitable metal mounting chassis. They may also be clamped in the moulded Universal Mounting Chassis UMC 60 or fixed with 3 mm screws.

Dimensions in mm (inch equivalents within brackets)



Size A (types 2.NOR60, 4.NOR60, 2.IA60, 2.LPA60, 2.SF60, TU60, GLD60)



Size B (types PA60 and HPA60)

Terminals	suitable for soldering and Miniwrap
Wrap tool	Gardner Denver, bit number 506633
Wrap wire size	0.3 mm (0.012" = 28 U.S. gauge = 30 s.w.g.)
Weight, size A	30 g approx.
size B	85 g approx.
Colour coding	see data sheets of the units

TEST SPECIFICATIONS

All units meet the following test specifications:

Test	IEC 68	MIL-STD-202C
Dry heat life test	56 days at max. diss. max. temp. check at: 0-10/14d-56d.	Meth. 108A, Cond. D; check at 0-10/ 14d-56d.
Long-term damp heat non operating	Test C, 56 days check at 0-10/14d-56d.	Meth. 103B, Cond. D; check at 0-10/ 14d-56d.
Long-term damp heat operating	Test C, 56d. min., diss., check at 0-10/14d-56d.	ditto
Temp. cycle-test	Test Na, 30 min., 2-3 min in between; preferred: -40 °C; +85 °C	Meth. 107B, Cond. A: moderate temp.
Vibration	Test Fb; 10-500-10 Hz 1 octave/min ; ampl. 0.75 mm max.; 10 g max. 3 x 3 hrs.	Meth. 204A, Cond. A: 10-500-10 Hz: 15 min ampl. 0.75 max; 10 g max., 3 x 3 hrs.
Shock	-	Meth. 202B, 3 blows 50 g.
Robustness of terminations	Test $U_A + U_B$	Meth. 211A + (B or C)
Solderability + solder heat	Test T; at 0 hr and at 56d; no electr. test	Meth. 210, at 0 hr and at 56d; no electr. test
Corrosion resistance	1% SO_2 solution, 95% R.H., 35 °C, 1 day. Recovery 27 days.	

CHARACTERISTICS AND DEFINITIONS

AMBIENT TEMPERATURE LIMITS

Storage	T_{amb} = -40 °C to +85 °C
Operating	T_{amb} = -10 °C to +70 °C

SUPPLY VOLTAGE (V_S)

Single rail, +24 $V_{d.c.}$ ± 25% (18 to 30 V) or
+12 $V_{d.c.}$ ± 5% (11,4 to 12,6 V) at reduced ratings

LOGIC LEVELS

The operation of the "60"-series is based on positive logic, i.e. "1" level is a positive voltage that is more positive than "0" level, and "0" level is independent of supply voltage.
Logic "1" depends upon supply and loading of the output of the logic functional block.

Levels with V_S = 24 V ± 25%	Levels with V_S = 12 V ± 5%
0 V < "0" < +0.3 V	0 V < "0" < +0,3 V
11,4 V < "1" < V_S	8,3 V < "1" < V_S

D.C. NOISE IMMUNITY

"0" level Immunity: A d.c. voltage of +1 V with respect to the 0-volt line, applied to any one input (the other inputs floating) will not cause a change of output voltage.

"1" level Immunity:

a. With a supply voltage of 24 V ± 25%:
A variation of 2 V of the "1" input level will not cause a unit to change its output voltage.

b. With a supply voltage of 12 V ± 5%:
A variation of 0,25 V of the "1" input level will not cause a unit to change its output voltage.

DRIVE UNIT: Drive required on one input of a NOR 60 (with all other inputs returned to 0-volt line) to bring the output at "0" level (less than +0,3 V).

FAN OUT: Number of drive units that can be delivered by a logic function without exceeding the "1" level limits as defined above.
The fan out actually indicates the number of NOR gates that can be driven into saturation (thereby bringing the respective outputs at "0" level).

INPUT AND OUTPUT DATA

EXTENSION OF THE DRIVE UNIT CONCEPT

System design is greatly simplified by expression of the input requirements and fan out capabilities of the various units in integral multiples of the D.U. To check that the loadability of a particular unit is not exceeded, simply add the number of D.U.'s present at its output.

LOADING TABLE

The loading table shows the input requirements and output capability of the various units expressed in D.U.'s.

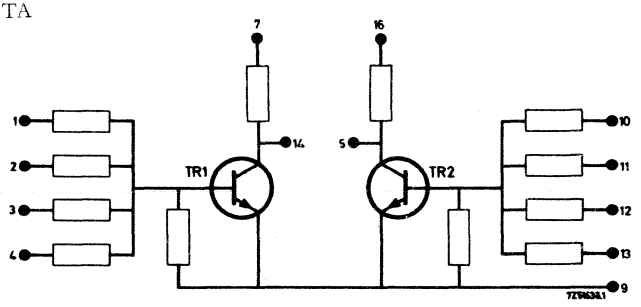
unit	input	V_S = 24 V ±25% output	V_S = 12 V ±5% output
2.NOR 60, per function	1 D.U.	6 D.U.	4 D.U.
4.NOR 60, per function	1 D.U.	6 D.U.	4 D.U.
2.IA 60, per function	2 D.U.	20 D.U.	13 D.U.
2.IA 60, connected as Low Power Amp.	2 D.U.	$R_{load} \geq 300\ \Omega$	$R_{load} \geq 150\ \Omega$
2.LPA 60 per function	2 D.U.	$R_{load} \geq 300\ \Omega$	$R_{load} \geq 150\ \Omega$
PA 60	1 D.U.	$R_{load} \geq 30\ \Omega$	$R_{load} \geq 13\ \Omega$
HPA60	1 D.U.	$R_{load} \geq 13,5\ \Omega$	$R_{load} \geq 6\ \Omega$
TU 60	1 D.U.	5 D.U.	3 D.U.
2.SF 60, per filter	100 $V_{d.c.}$	2 D.U.	2 D.U.
GLD 60 NOR function	1 D.U.	6 D.U.	-
GLD function	2 D.U.	900 D.U.	-

For matching non standard input signals to 60-Series inputs as well as matching non standard loads, the data sheets of the units give impedances and current requirements.

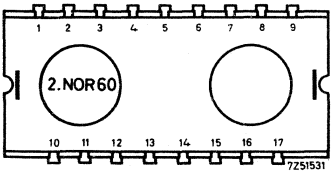
DUAL FOUR INPUT NOR GATE

Function	dual NOR (positive logic)
Case	size: A; colour: black

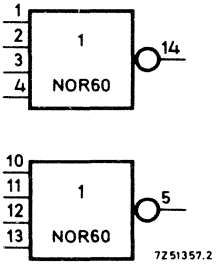
CIRCUIT DATA



Circuit diagram



Terminal location



Drawing symbols

1, 2, 3, 4	= input NOR 1
5	= output NOR 2
6	= n.c.
7	= for supply NOR 1 (V_S)
8	= n.c.
9	= 0 V common
10, 11, 12, 13	= input NOR 2
14	= output NOR 1
15	= n.c.
16	= for supply NOR 2 (V_S)
17	= n.c.

The unit contains two identical transistor-resistor NOR circuits. Each circuit has 4 inputs. If any input of a NOR is at "1" level the output of that NOR will be at "0" level.

CHARACTERISTICS

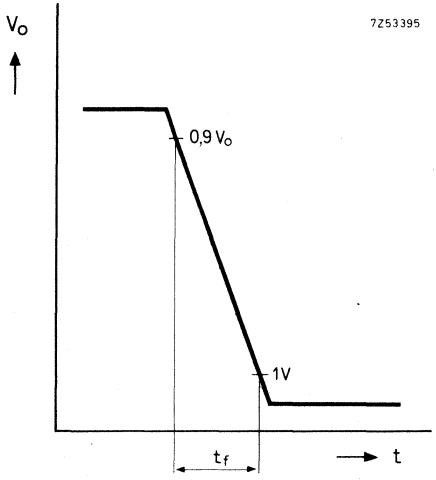
	at V_S = 24 V ± 25%	at V_S = 12 V ± 5%
Supply current at V_S nom	3,5 mA	1,75 mA
at V_S max	≤ 4,8 mA	≤ 1,95 mA
Input requirement	1 D.U.	1 D.U.
Output capability	6 D.U.	4 D.U.

	single input	two paralleled inputs	three paralleled inputs	four paralleled inputs
→ Input impedance [1]	90 kΩ	50 kΩ	35 kΩ	30 kΩ
Input current for "0" output [1][2]	0,13 mA	0,125 mA	0,.11 mA	0,1 mA

Switching speed

Fall time defined below $t_f \leq 1,25\ \mu s$

Fall delay time defined below $t_{fd} \leq 6\ \mu s$



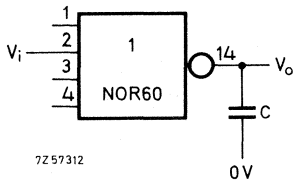


Fig. A

The fall time t_f is defined as the time required for the output voltage V_o to change from 90% of its full value to 1 V after application of a step input, the output being loaded with C = 200 pF (see Fig. A).

1) Unused inputs returned to 0-volt line.
2) At V_S = 30 V,

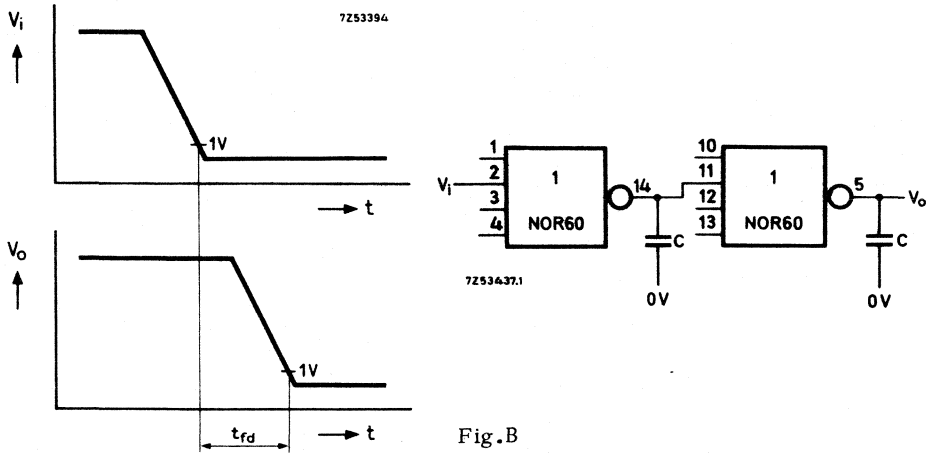


Fig.B

The fall delay time t_{fd} is defined as the time between the 1 V points of the negative-going input and output voltages of two cascaded NORs, each being loaded with C = 200 pF (see Fig.B).

LIMITING VALUES (Destruction may occur when these values are exceeded)

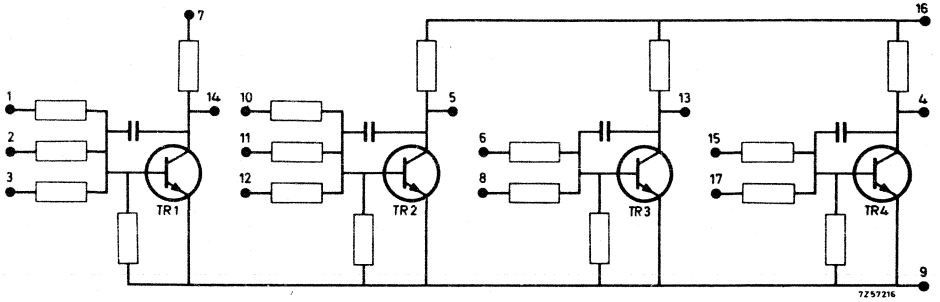
Supply voltage	V_S	max. 30	$V_{d.c.}$
		min. 0	V
Positive transient on V_S		max. 10	V during 10 μs
Positive input voltage	$+V_i$	max. 90	V
Negative input voltage	$-V_i$	max. 18	V

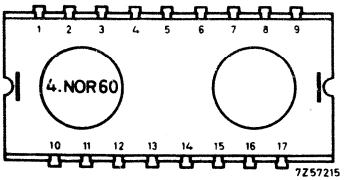
QUADRUPLE 2×2 + 2×3 INPUT NOR GATE

Function — quadruple NOR (positive logic)

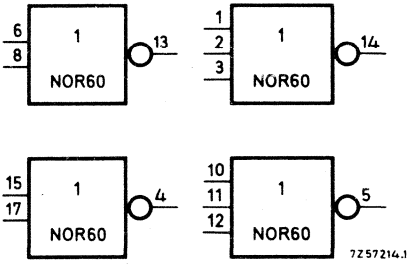
Case — size: A; colour: black

CIRCUIT DATA





Terminal location



Drawing symbols

1, 2, 3 = input NOR 1
4 = output NOR 4
5 = output NOR 2
6, 8 = input NOR 3
7 = for supply NOR 1 (V_S)
9 = 0 V common
10, 11, 12 = input NOR 2
13 = output NOR 3
14 = output NOR 1
15, 17 = input NOR 4
16 = for supply NOR 2, 3, 4 (V_S)

The unit contains two identical 2-input and two identical 3-input NOR circuits. If any input of a NOR is at "1" level the output of that NOR will be at "0" level.

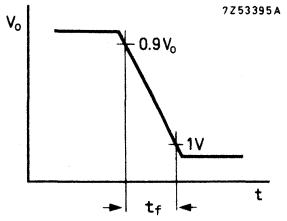
CHARACTERISTICS

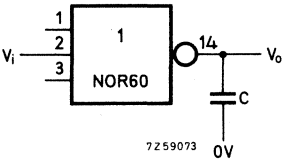
	at V_S = 24 V ±25%	at V_S = 12 V ±5%
Supply current at $V_{S\,nom}$	3,5 mA	1,75 mA
at $V_{S\,max}$	≤ 4,8 mA	≤ 1,95 mA
Input requirement	1 D.U.	1 D.U.
Output capability	6 D.U.	4 D.U.

	single input	two paralleled inputs	three paralleled inputs
Input impedance [1])	90 kΩ	50 kΩ	35 kΩ
Input current for "0" output [1])[2])	0,13 mA	0,125 mA	0,11 mA

Switching speed

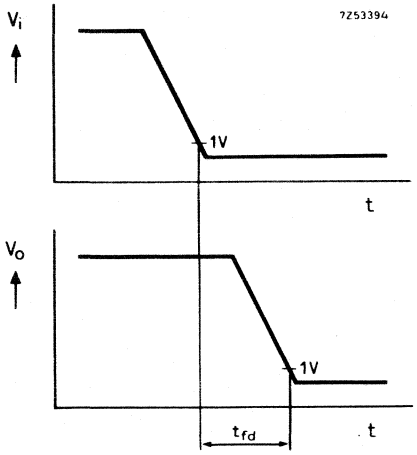
Fall time defined below	t_f ≤ 14 μs
Fall delay time defined below	t_{fd} ≤ 26 μs





The fall time t_f is defined as the time required for the output voltage V_O to change from 90% of its full value to 1 V after application of a step input, the output being loaded with C = 200 pF (see Fig. A).

[1]) Not used inputs returned to 0-volt line.
[2]) At V_S = 30 V.



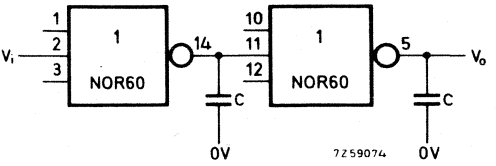


Fig.B

The fall delay time t_{fd} is defined as the time betweeb the 1 V points of the negative-going input and output voltages of two cascaded NORs, each being loaded with C = 200 pF (see Fig.B).

LIMITING VALUES (Destruction may occur when these values are exceeded)

Supply voltage	V_S	max. 30 V min. 0 V	$V_{d.c.}$
Positive transient on V_S		max. 10 V for 10 μs	
Positive input voltage	$+V_i$	max. 90 V	
Negative input voltage	$-V_i$	max. 24 V	

DUAL INVERTER AMPLIFIER

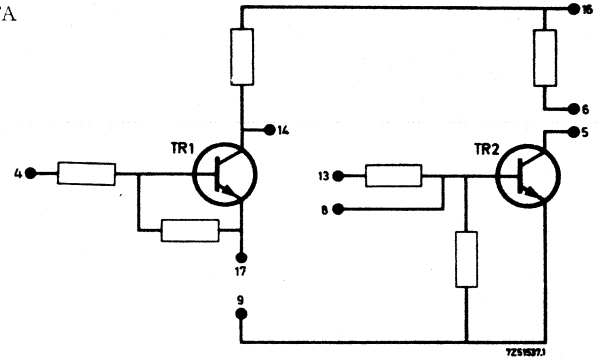
Function

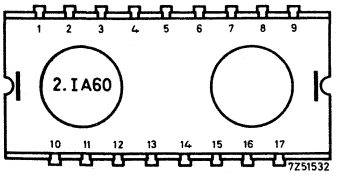
The unit comprises two identical Inverter Amplifiers. Use as a single inverting Low Power Amplifier is feasible.

Case

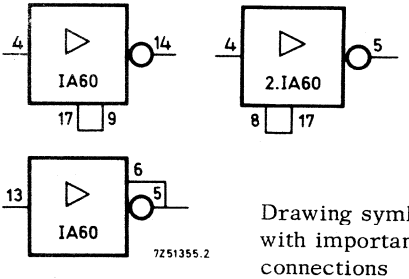
Size:A; colour: blue

CIRCUIT DATA





Terminal location



Drawing symbols with important connections

1, 2, 3 = n.c.
4 = input IA 1
5 = output IA 2
6 = collector resistor IA 2
7 = n.c.
8 = base of IA 2 transistor
9 = 0 V common
10, 11, 12 = n.c.
13 = input IA 2
14 = output IA 1
15 = n.c.
16 = for supply (V_S)
17 = emitter of IA 1 transistor

To obtain the dual I.A., pin 17 should be connected to pin 9 and pin 6 to pin 5.
A "1" level input (pin 4 or 13) will cause a "0" level output (pin 14 or 5-6 respectively).
To obtain the inverting L.P.A., pin 17 should be connected to pin 8 and the load connected between pins 5 and 16. When pin 4 is at "1" level, pin 5 will be at "0" level.

Notes to the load of the L.P.A.

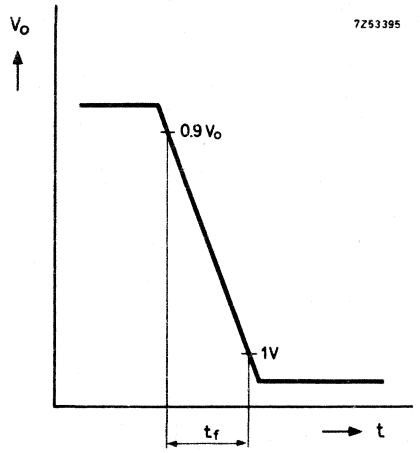
1. Care should be taken that the value of a varying load should not drop below the specified minimum.
2. Incandescent lamps have a "cold" resistance that is only a fraction of the value calculated from nominal voltage and current, so that turning on of the lamp may cause a surge current. It is advisable to use a pre-heating quiescent current to eliminate destructive surge currents.
3. Inductive loads will cause large voltage peaks upon switching off. To avoid destruction the load should be provided with a flywheeling diode, type BAX12. The anode should be connected to pin 5, the cathode to pin 16 (positive supply).

CHARACTERISTICS

	at V_S = 24 V ±25%		at V_S = 12 V ±5%	
	per I.A.	as L.P.A.	per I.A.	as L.P.A.
Supply current at $V_{S\,nom}$	10,9 mA	10,9 mA I_{load} = 0 mA	5,5 mA	5,5 mA I_{load} = 0 mA
Supply current at V_S max and "1" input	≤ 15,5 mA	≤ 114 mA R_{load} = 300 Ω	≤ 6,5 mA	≤ 89,9 mA R_{load} = 150 Ω
Input requirement	2 D.U.	2 D.U.	2 D.U.	2 D.U.
Output capability	20 D.U.	140 D.U. [1]	13 D.U.	
Minimum load resistance		300 Ω [1]		150 Ω [1]

Input impedance		45 kΩ
Input current for "0" output of I.A. at V_S = 30 V		0,285 mA
Switching speed		
Fall time defined below	t_f	≤ 1 μs
Fall delay time defined below	t_{fd}	≤ 3 μs

[1]) This load is permissible only if the input switched between "0" and "1" levels by a preceding 60 Series unit or other true digital input, avoiding excessive dissipation during transitions.



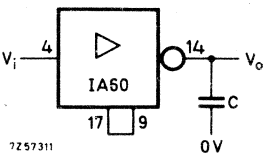
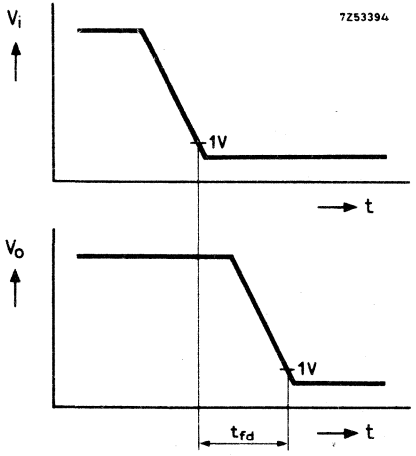


Fig.A

The fall time t_f is defined as the time required for the output voltage V_O to change from 90% of its full value to 1 V, after application of a step input, the output being loaded with C = 200 pF (see Fig.A).



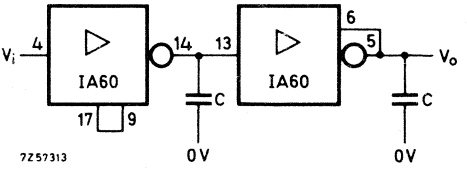


Fig.B

The fall delay time t_{fd} is defined as the time between the 1 V points of the negative-going input and output voltages of two cascaded Inverter Amplifiers, each being loaded with 200 pF (see Fig.B).

LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply voltage	V_s	max.	30	$V_{d.c.}$
		min.	0	V
Positive transient on V_s		max.	10	V during 10 μs
Positive input voltage	$+V_4$, $+V_{13}$	max.	70	V
Negative input voltage	$-V_4$, $-V_{13}$	max.	16	V
Positive voltage at pin 8	$+V_8$	max.	4	V via min. 500 Ω
Negative voltage at pin 8	$-V_8$	max.	5	V

DUAL LOW POWER AMPLIFIER

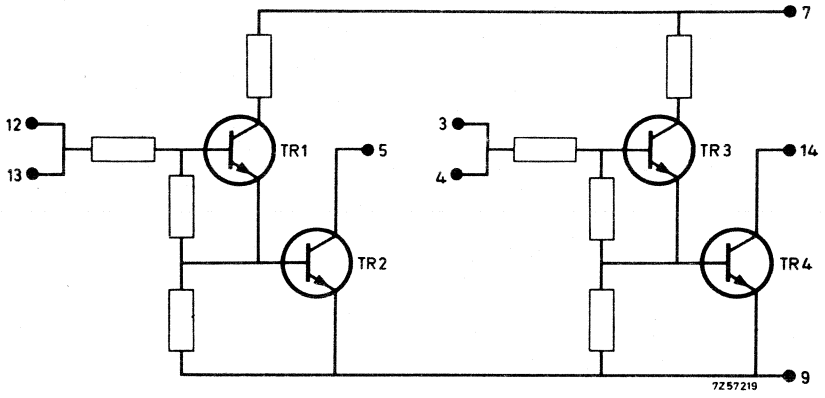
Function

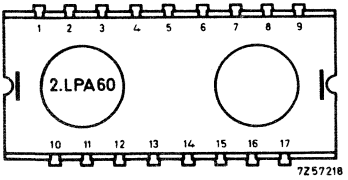
The unit comprises two identical inverting Low Power Amplifiers

Case

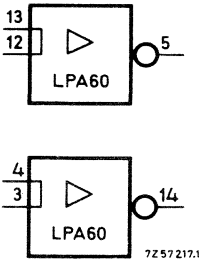
size: A; colour: blue

CIRCUIT DATA





Terminal location



Drawing symbols

1, 2	=	n.c.
3, 4	=	input LPA2
5	=	output LPA1
6	=	n.c.
7	=	for supply (V_S)
8	=	n.c.
9	=	0 V common
10, 11	=	n.c.
12, 13	=	input LPA1
14	=	output LPA2
15, 16, 17	=	n.c.

The load should be connected between pins 5 and 7 for LPA1 and between pins 14 and 7 for LPA2.
When the input (12/13 or 3/4) is at "1" level, the output (5 or 14) will be at less than 1 V. This being no true "0" level, it is not recommended to use an LPA as a logic operator.

Notes to the loading

1. Care should be taken that the value of a varying load should not drop below the specified minimum.
2. Incandescent lamps have a "cold" resistance that is only a fraction of the value calculated from nominal voltage and current, so that turning on of the lamp may cause a surge current. It is advisable to use a pre-heating quiescent current to eliminate destructive surge currents.
3. Inductive loads will cause large voltage peaks upon switching off. To avoid destruction the load should be provided with a flywheeling diode, type BAX12. The anode should be connected to pin 5 (14), the cathode to pin 7 (positive supply).

CHARACTERISTICS

	at V_S = 24 V ±25%	at V_S = 12 V ±5%
Supply current at $V_{S\,nom}$, I_{load} = 0 mA	8 mA	4 mA
Supply current at $V_{S\,max}$ and "1" input,		
R_{load} = 300 Ω	≤ 108 mA	–
R_{load} = 150 Ω	–	≤ 89.9 mA
Input requirement	2 D.U.	2 D.U.
Output capability	100 mA	80 mA
Min. load resistance	300 Ω	150 Ω

Input impedance		45 kΩ
Input current for "0" output at V_S = 30 V		0.285 mA
Output voltage at "1" input		< 1 V
Switching speed		
Fall time (Fig.A)	t_f	≤ 0.4 µs
Rise time (Fig.B and Fig.C)	t_r	≤ 2 µs
Storage time (Fig.B and Fig.C)	t_s	≤ 10 µs

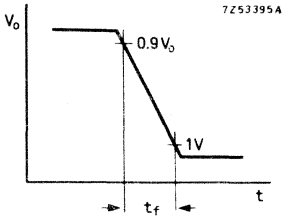


Fig.A

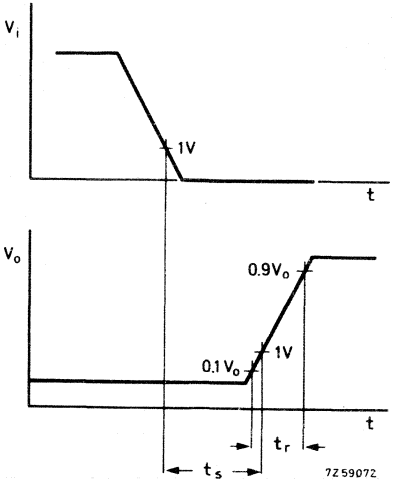


Fig.B

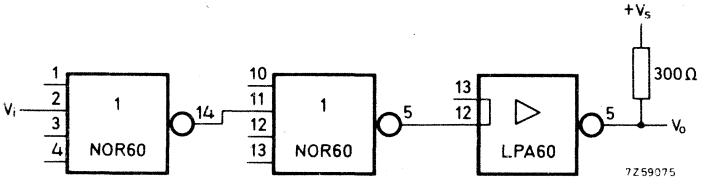


Fig.C

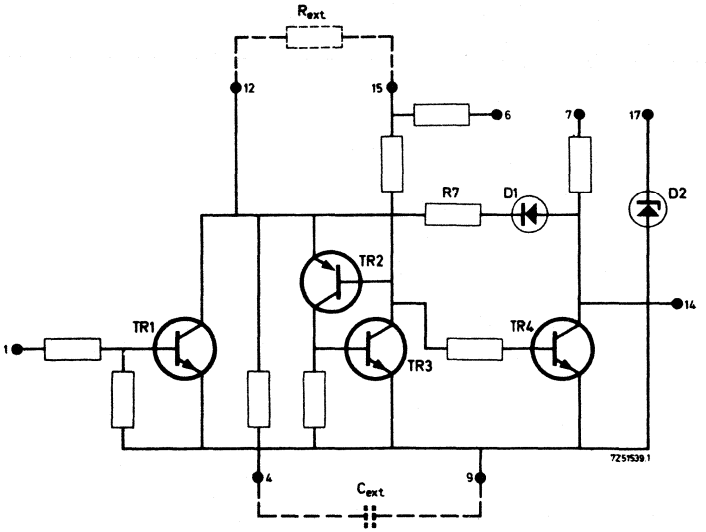
LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply voltage	V_s	max. 30 min. 0	$V_{d.c}$ V	
Positive transient on V_s		max. 10	V	for 10 μs
Positive input voltage	$+V_i$	max. 70	V	
Negative input voltage	$-V_i$	max. 16	V	

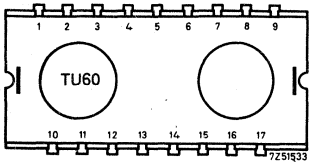
TIMER

Function	Gives an inverted output. The output of a "1" is delayed following a "0" input. No delay occurs when the input returns to "1"
Case	Size: A; colour: red

CIRCUIT DATA

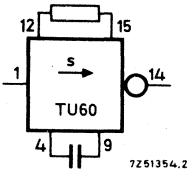


With the input at "1" the capacitor (C_{ext}) is discharged. When the input goes to "0", TR_1 ceases to conduct so that the capacitor is allowed to slowly charge until the base potential of TR_2 is exceeded. TR_2 starts to conduct and provides base current for TR_3, which speeds the turn-on of TR_2. TR_4 ceases to conduct and the output level changes from "0" to "1". Positive feedback is provided via D_1 and R_7.



Terminal location

1	= input	10, 11	= n.c.
2, 3	= n.c.	12	= for external resistor
4	= for external capacitor	13	= n.c.
5	= n.c.	14	= output
6	= see instructions below	15	= for external resistor
7	= positive supply	16	= n.c.
8	= n.c.	17	= see instructions below
9	= 0 V common		



Drawing symbol with significant connections

Instructions for connection of the supply

When V_S = 24 V ±25% : connect 6 and 7,
connect 15 and 17.

When V_S = 12 V ±5% : connect 15 and 7,
do not connect 6 and 7.

CHARACTERISTICS

	at V_S = 24 V ±25%	at V_S = 12 V ±5%
Supply current at $V_{S\,nom}$	6.9 mA	1.9 mA
at $V_{S\,max}$	10.1 mA	2.1 mA
Input requirement	1 D.U.	1 D.U.
Output capability	5 D.U.	3 D.U.

Input impedance	90 kΩ
Input current for "0" output, at V_S = 30 V	0.125 mA
External resistance	R_{ext} min. 100 kΩ, max. 1 MΩ
Leakage current of external capacitor when connected between	
pins 4 and 9	max. 100 nA at 10 V
pins 15(+) and 4	max. 100 µA at 25 V

Delay time (see Fig.A)	t_{delay}	about R_{ext} C_{ext} s ($M\Omega$ x μF) [1]
Max. change of delay time with temperature (C_{ext} pins 4 and 9)		- 0,14 %/°C
Switching speed		
Fall time as defined below	t_f	$\leq$ 1 μs
Rise time as defined below	t_r	$\leq$ 6 μs
Timing requirements (see Fig.A)		
Set time	t_{set}	min. 11,9 C_{ext} ms (C_{ext} in μF)
Recovery time	t_{sec}	min. 11,9 C_{ext} ms
Start inhibit before end of delay	$t_{st\ inh}$	min. 18,9 C_{ext} ms
Inhibit duration	t_{inh}	min. 18,9 C_{ext} ms (A shorter t_{inh} gives a shorter delay)

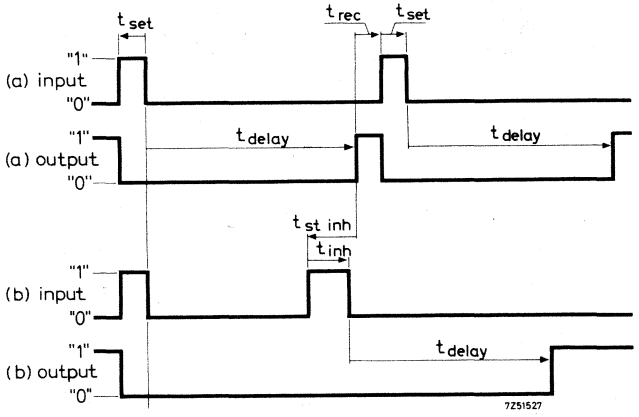


Fig.A

[1] For long delay times the 25 μF, 160 V_{rms} film capacitor, catalogue number 2222 325 50256 is recommended.

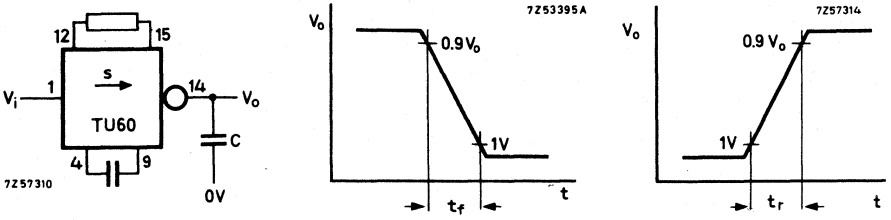


Fig.B

The fall time t_f is defined as the time required for the output voltage V_O to change from 90% of its full value to 1 V, after application of a step input and being loaded with C = 200 pF (see Fig.B).

The rise time t_r is defined as the time required for the output voltage V_O to change from 1 V to 90% of its full value, after application of a step input and being loaded with C = 200 pF (see Fig.B).

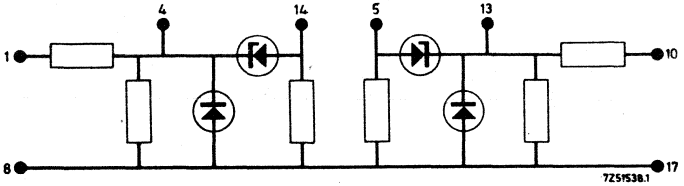
LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply	V_S	max. 30 $V_{d.c.}$ min. 0 V
Positive transient on V_S		max. 10 V for 10 µs
Positive input voltage	$+V_I$	max. 70 V
Negative input voltage	$-V_I$	max. 16 V
→ External resistance	R_{ext}	min. 820 Ω

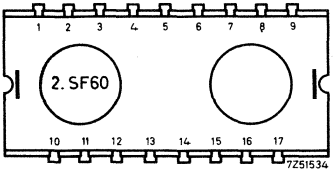
DUAL SWITCH FILTER

Function	Dual switch filter for eliminating the effects of contact bounce of mechanical switches
Case	size: A; colour: green

CIRCUIT DATA

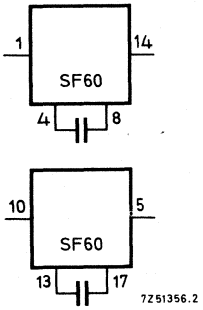


The circuit consists of two identical filters for minimising the effects of contact bounce and spurious interference on long leads between switch and system input. The switch filter also has the facility that 100 V are applied across the switch contacts, thus ensuring reliable switching.
The voltage divider enables the input to be presented with a high impedance load whilst the internal circuitry is presented with a lower impedance source. The time for which contact bounce is eliminated is determined by an external capacitor. The zener diode provides a threshold. The diode prevents that excessive base current is drawn from any driven NORBIT if a large negative voltage appears on the filter input. It also prevents that a reverse voltage is presented to the capacitor, which thus may be of a polarised type.



Terminal location

1	= input SF1	10	= input SF2
2, 3	= n.c.	11, 12	= n.c.
4	= for external capacitor of SF1	13	= for external capacitor of SF2
5	= output SF2	14	= output SF1
6, 7	= n.c.	15, 16	= n.c.
8	= 0 V common	17	= 0 V common (to be taken to central earth point)
9	= n.c.		



Drawing symbols with capacitor

Instructions

a. Capacitor working voltage ≥ 100 $V_{d.c.}$

b. Mount the unit as close as possible to the logic system input.

c. The common 0-volt line (8 or 17) must be returned to the central earth point of the system to avoid common impedance coupling.

CHARACTERISTICS (per filter)

Input voltage for "1" out	+100 V ±25%
Input current	< 3.3 mA
Input surge current peak	< 4.8 mA
Output capability	2 D.U.
Contact bounce elimination time	1,4 C ms (C in μF)

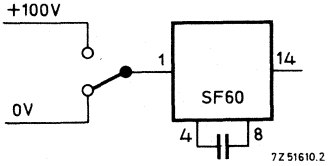


Fig.a

Switching speed (C in μF):

Turn-on time	41 C ms
Max. operating frequency with 1 : 1 mark to space ratio for circuit Fig.a	$\frac{6.3}{C}$ Hz
Ditto for Fig.b	$\frac{11.08}{C}$ Hz

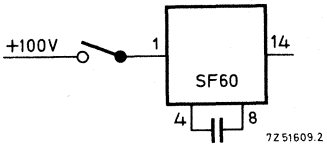


Fig.b

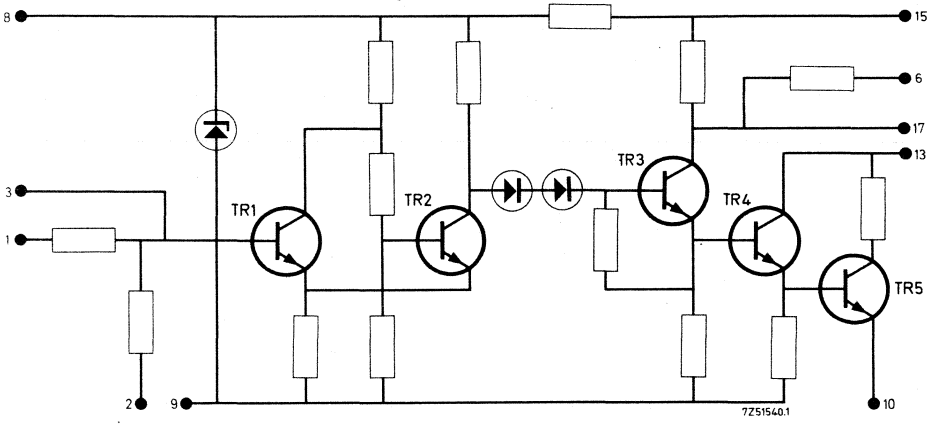
LIMITING VALUES (Destruction may occur if these values are exceeded)

Positive input voltage	$+V_1$, $+V_{10}$	max. 125 V
Negative input voltage	$-V_1$, $-V_{10}$	max. 100 V

POWER AMPLIFIER

Function	Power amplifier for load switching
Case	size: B; colour: blue

CIRCUIT DATA



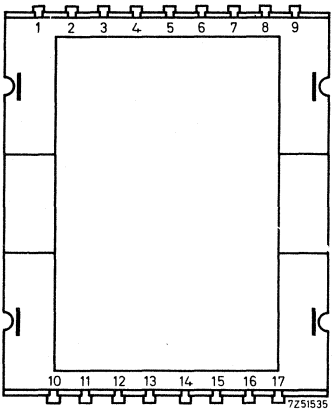
The power amplifier consists of a Schmitt trigger followed by a buffer + driver stage, which provides adequate drive to the power transistor under all conditions of permissible supply voltage and input signal. The load should be connected between pin 13 and + of power supply. A "1" input will switch on the load current.

Notes

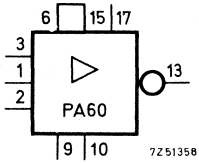
1. Observe rules for $R_{load\,min.}$
2. Incandescent lamps have a "cold" resistance that is only a fraction of the value calculated from voltage and current so that turning on of a lamp may cause a current surge. It is often advisable to use a preheating quiescent current to eliminate destructive surge currents.
3. Inductive loads will cause large voltage peaks at switching off. To avoid destruction of the output transistor the load should be shunted by a damping diode. By using diode type BAX12 a max. current of 1 A at 30 V in a load of 10 H can be switched off while secondary breakdown is avoided.
   (Connection of the diode: anode to pin 13, cathode to supply).

4. Pin 10 facilitates the connection of a 0 V load supply line which is separated from the 0 V logic supply line up to the power supply unit, by which means common wire impedance is avoided. Also, if a second power supply unit is used for the PA 60, common impedance with the 0 V logic supply line should be avoided in the connecting wire necessary between pin 9 (0 V logic supply) and pin 10 (0 V supply of PA 60).

Terminal location



1 = input
2 = base resistor of input transistor
3 = base of input transistor
4, 5 = n.c.
6 = +supply, connect to 15
7 = n.c.
8 = zener diode
9 = 0 V common
10 = 0 V output stage, see note 4
11, 12 = n.c.
13 = output (load between 13 and supply)
14 = n.c.
15 = +supply, connect to 6
16 = n.c.
17 = collector of TR3



Drawing symbol with one of the necessary connections

Additional instructions

a. If the input (pin 1) is driven by a standard "1" level from NOR 60, etc., connect pins 2 and 9.

b. If the supply voltage is 12 V ±5%, connect a resistor of 330 Ω between pin 6 and 8, and a resistor of 1.5 kΩ between 15 and 17; both resistors ±5%, $\frac{1}{4}$ W.

c. Wiring to pin 3 must be kept remote from the output circuitry.

d. When using pin 3 as a second input, the input resistor should be connected direct to the pin.

CHARACTERISTICS

	at V_S = 24 V ±25%	at V_S = 12 V ±5%
Supply current at $V_{S\,nom}$ excluding I_{load}	18.8 mA	15.1 mA
Supply current at $V_{S\,max}$ excluding I_{load}	< 26.2 mA	< 28.8 mA
Required load resistance	> 30 Ω	> 13 Ω
Required input	1 D.U.	1 D.U.

	at pin 1	at pin 3
For switching on load current		
input voltage, 2–9 connected	> 6 V	> 1.6 V [1]
input current, 2–9 connected	75 µA	75 µA
2–9 not connected [2]	30 µA	30 µA
For switching off load current		
input voltage, 2–9 not connected [2]	< 1.15 V	< 1.15 V
On-off input voltage difference		
2–9 not connected [2]	–	> 0.5 V

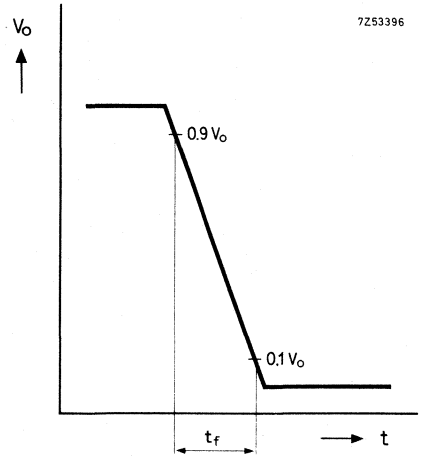
Switching speed

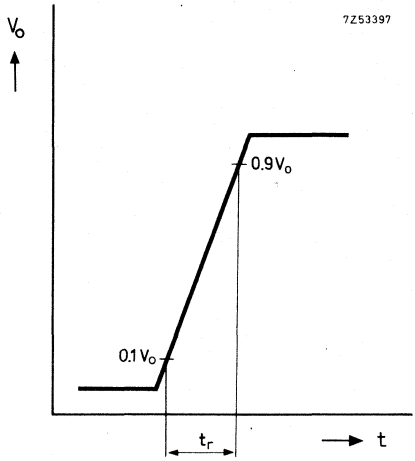
Fall time as defined below	$t_f \leq 1\ \mu s$
Rise time as defined below	$t_r \leq 5\ \mu s$

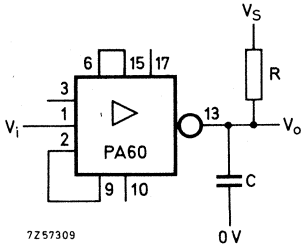
The fall time t_f is defined as the time required for the output voltage to change from 90% to 10% of its full value, after application of a step input, at a supply voltage V_S = 30 V and a load resistance R = 30 Ω shunted by C = 200 pF (see Figure).

The rise time t_r is defined as the time required for the output voltage to change from 10% to 90% of its full value, after application of a step input, at a supply voltage V_S = 30 V and a load resistance R = 30 Ω shunted by C = 200 pF (see Figure).

1) Via min. 500 Ω
2) Source resistance must not exceed 56 kΩ







LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply voltage(s)	V_S	max. 30	$V_{d.c.}$
		min. 0	V
Positive transient on V_S driver stage		max. 10	V during 10 μs
Positive transient on V_S power stage		max. 5	V during 10 μs
Voltage at pin 1 (pins 2 and 9 connected)			
positive	$+V_1$	max. 100	V
negative	$-V_1$	max. 15	V
Voltage at pin 3			
positive	$+V_3$	max. 5	V via min. 500 Ω
negative	$-V_3$	max. 4.5	V

HIGH POWER AMPLIFIER

Function	Power Amplifier for load switching
Case	Size: B; colour: black

CIRCUIT DATA

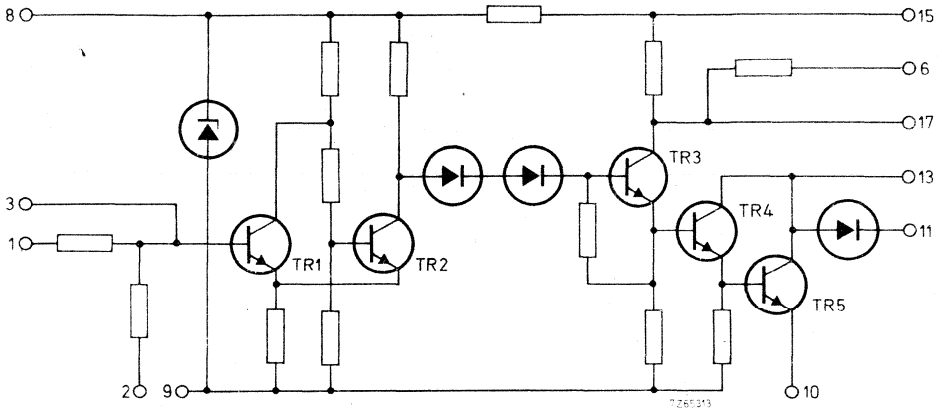


Fig. 1

The power amplifier consists of a Schmitt trigger followed by a buffer + driver stage, which provides adequate drive to the power transistor under all conditions of permissible supply voltage and input signal. The load should be connected between pin 13 and + of power supply. A "1" input will switch on the load current.

Notes:

1. Observe rules for $R_{load\ min}$.
2. Incandescent lamps have a "cold" resistance that is only a fraction of the value calculated from voltage and current so that turning on of a lamp may cause a current surge. It is often advisable to use a preheating quiescent current to eliminate destructive surge currents.
3. Inductive loads will cause large voltage peaks at switching off. To avoid destruction of output transistor the load should be shunted by a damping diode. By connecting terminal 11 to the supply line inductive loads up to a certain value can be handled by the internal diode.

4. Pin 10 serves to make a separate connection between a 0 V load supply line and the power supply unit to avoid common wire impedance with the 0 V logic supply line. Also, if a second supply unit is used for the HPA 60, common impedance with the 0 V logic supply line should be avoided in the interconnection between pins 9 (0 V logic supply) and 10 (0 V output stage).

Terminal location

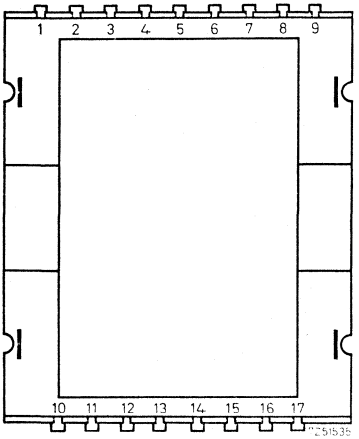


Fig. 2

1	= input
2	= base resistor of input transistor
3	= base of input transistor
4	= n.c.
5	= n.c.
6	= + supply, connect to 15
7	= n.c.
8	= zener diode
9	= 0 V logic supply
10	= 0 V output stage, see note 4
11	= damping diode
12	= n.c.
13	= output (load between 13 and supply)
14	= n.c.
15	= + supply, connect to 6
16	= n.c.
17	= collector of TR3

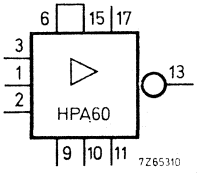


Fig. 3
Drawing symbol (one necessary interconnection indicated).

Additional instructions

a. If the input (pin 1) is driven by a standard "1" level from NOR 60, etc., connect pins 2 and 9.

b. If the supply voltage is 12 V ± 5%, connect a resistor of 330 Ω between pin 6 and 8, and a resistor of 1.5 kΩ between 15 and 17; both resistors ± 5%, $\frac{1}{4}$ W.

c. Wiring to pin 3 must be kept remote from the output circuitry.

d. When using pin 3 as a second input, the input resistor should be connected direct to the pin.

CHARACTERISTICS

	V_S = 24 V ± 25%	V_S = 12 V ± 5%
Supply current at V_S nom excluding I_{load}	18.8 mA	15.1 mA
Supply current at V_S max excluding I_{load}	< 26.2 mA	< 28.8 mA
Required load resistance at T_{amb} = 45 to 70 °C	> 13.5 Ω	> 6 Ω
at T_{amb} < 45 °C	> 12 Ω	> 5 Ω
Required input	1 D.U.	1 D.U.
Voltage on pin 13, TR5 conducting	max. 2 V	max. 2 V

	at pin 1	at pin 3
For switching on load current		
input voltage, 2–9 connected	> 6 V	> 1.6 V [1]
input current, 2–9 connected	75 µA	75 µA
2–9 not connected [2]	30 µA	30 µA
For switching off load current		
input voltage, 2–9 not connected [2]	< 1.15 V	< 1.15 V
On-off input voltage difference		
2–9 not connected [2]	–	> 0.5 V

Switching speed	maximum	typical
Fall time, t_f	0.2 µs	0.05 µs
Rise time, t_r	4.2 µs	0.3 µs

The fall time t_f is defined as the time required for the output voltage to change from 90% to 10% of its full value, after application of a step input, under conditions as shown in Fig. 4 (See also Fig. 5).

The rise time t_r is defined as the time required for the output voltage to change from 10% to 90% of its full value, after application of a step input, under conditions as shown in Fig. 4 (See also Fig. 6).

1) Via min. 500 Ω.
2) Source resistance must not exceed 56 kΩ.

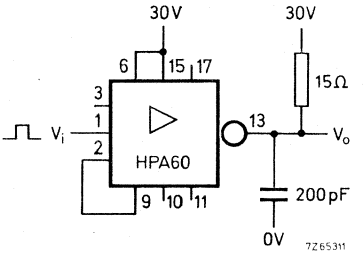


Fig. 4

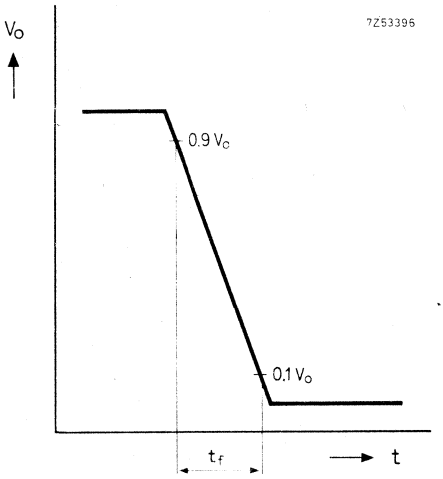


Fig. 5

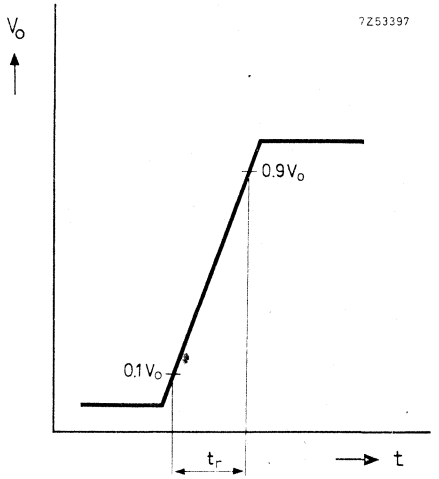


Fig. 6

By connecting terminal 11 to the supply line the following inductive loads can be handled by the internal damping diode:

R_L = 15 Ω	$L_L \leq$ 10 H
R_L = 20 Ω	$L_L \leq$ 14 H
R_L = 30 Ω	no restriction

Switch-off delay time for R_L = 30 Ω and L_L = 10 H is 770 ms.

LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply voltage, V_S	max. 30 V d.c.
Positive transient on driver stage (pin 6 and 15)	max. 10 V for 10 μs
Positive voltage on power stage, pin 13	max. 55 V
Voltage at pin 1 (2–9 connected)	
positive	max. 100 V
negative	max. 15 V
Voltage at pin 3	
positive	max. 5 V via min. 500 Ω
negative	max. 4.5 V
Output current	5 A for 20 ms

OVERLOAD PROTECTION

Protection measures must be taken in applications in which overloading of the HPA 60 may occur, e.g. short circuiting of the load. The operating time of a fuse is far too slow to provide adequate protection in such cases, therefore another method must be used. The protection circuit described here uses a 2.IA 60 connected as a memory element, and serves well in many HPA 60 applications.
It will operate at a load current of 3 A. Removing one of two series-connected diodes will bring the "fault" condition of load current down to 2 A. Finer control of the load current level at which the protection circuit will operate may be achieved by replacing the resistor R by a wire-wound potentiometer.

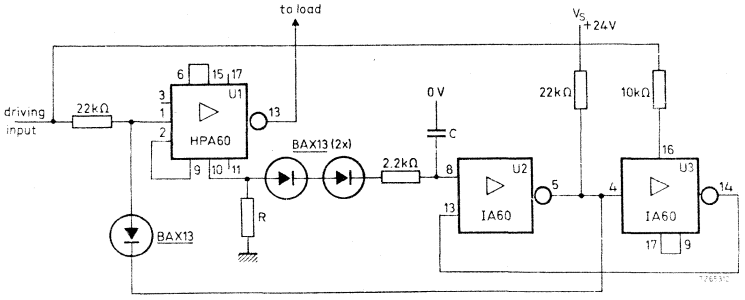


Fig.7

R = 0,39 Ω (2 W)
C = 100 nF

Load current information is provided by resistor R, and is fed to U2 (pin 8) via the series-connected diodes.
The capacitor C prevents the circuit from operating on transient currents of up to 5 A. If the load current is too high for the HPA 60, the output of U2, at pin 5, goes LOW. This LOW is fed back to U1, pin 1 , via the BAX13 diode. A LOW at the input of the HPA 60 switches it off.

When the overload is removed, the protection circuit remains in the fault condition because the memory element is still "set". The protection circuit can only be "reset" by removing the logic signal from the driving input, since U3 is fed with the HPA 60 driving input via pin 16.

The circuit shown here requires 6 D.U.

GROUNDED LOAD DRIVER

Function: - a 2 input power amplifier for switching d.c. loads, connected with one side to ground (GLD)
- a 2 input NOR gate
- monitor circuit for twin channel logic systems with fault display.

Case: Norbit block size A, colour black.

CIRCUIT DATA

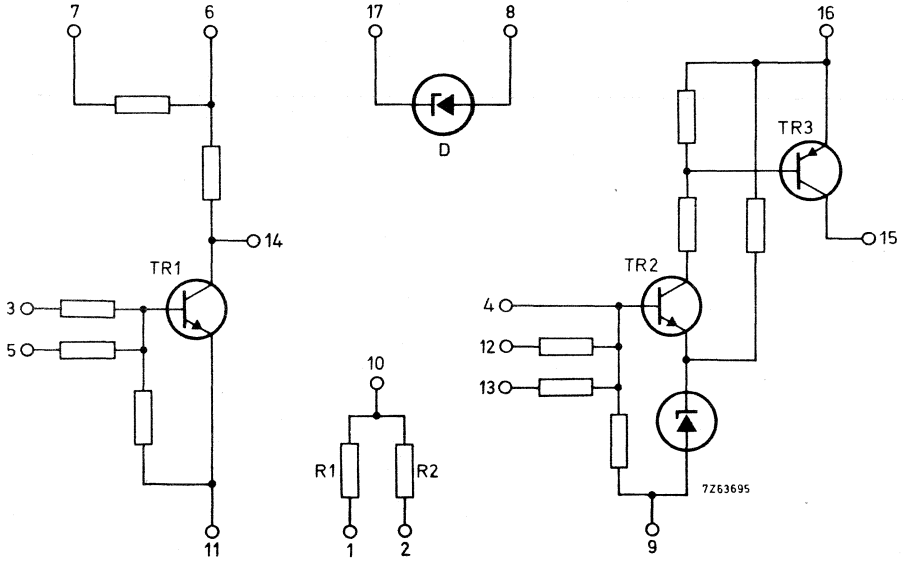


Fig. 1

The unit comprises two main circuits and auxiliary networks:
- A NOR gate with two inputs each requiring 1 D.U.. The output capability is 6 D.U..
- A grounded load driver (GLD) consisting of an input stage with two inputs and a PNP output stage. The load should be connected between the output terminal and 0 V common. A "1" input signal will switch on the load current.
- A voltage regulator diode (D) to couple the NOR to the GLD, or to isolate the load of the GLD from the resistance network (R1 and R2) when the complete unit is applied as a monitor circuit for twin channel logic systems with fault display.

Terminal location

1 = R1
2 = R2
3 = input NOR
4 = auxiliary input GLD
5 = input NOR
6 = positive supply V_S for NOR
7 = auxiliary supply
8 = voltage regulator diode, anode
9 = 0 V common GLD
10 = R1, R2
11 = emitter TR1, 0 V if used as NOR
12 = input GLD
13 = input GLD
14 = output NOR
15 = output GLD
16 = positive supply V_S for GLD
17 = voltage regulator diode, cathode

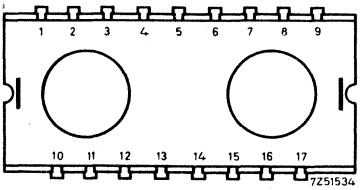


Fig. 2

Drawing symbols

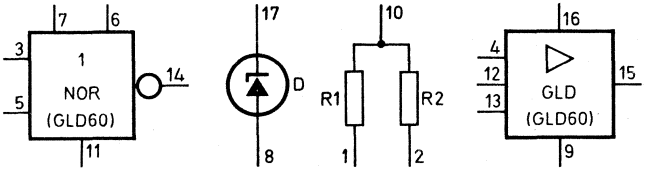


Fig. 3 NOR function auxiliary circuits GLD function

CHARACTERISTICS

7Z63686

	NOR (supply to pin 6)	GLD
Power supply voltage (V_S)	+24 V ±25%	+24 V ±25%
current	nom. 3,2 mA max. 4,1 mA	nom. 14,2 mA + I_{load} max. 19,1 mA + I_{load}
Input requirements, per terminal	1 D.U.	2 D.U.
Output capability	6 D.U.	900 D.U.
at maximum load resistance		3 kΩ
Minimum load resistance,		
- driven by signal on pins 12 and 13		75 Ω *) at T_{amb} = 45 °C 86 Ω *) at T_{amb} = 70 °C
- driven by NOR via D on pin 4 (supply to pins 7 and 16, connect pin 8 to 4, pin 14 to 17, pin 11 to 10, pin 12 or 13 to 0 V)		120 Ω *)

*) For use with incandescent lamps, series and/or bleed resistors might be required to avoid high inrush currents in connection with their "cold" resistance. To limit large voltage peaks at switching of inductive loads these loads should be shunted by a damping diode, e.g. BAX12 (cathode to pin 15).

Resistor network

R1	3010 Ω
R2	1500 Ω

Voltage regulator diode

V_D	12 V

LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply voltage V_S	max. +30 V d.c. min. 0 V d.c.
Positive transient on V_S	max. +10 V for 10 µs
Input voltage	
NOR (pins 3, 5)	max. +70 V min. −15 V
GLD (pins 12, 13)	max. +70 V min. − 4 V
Input current GLD (pin 4)	max. +20 mA *)
Output surge current	max. 1 A for 20 ms

APPLICATION INFORMATION

A GLD60 as a grounded load amplifier

1. The GLD 60 makes it possible to drive loads (relays, magnetic valves etc.) of which one side has been connected to ground, Fig. 4 illustrates also the suitability of the unit for systems which from the point of safety require that the load is not activated in case of short circuit to ground of the output.

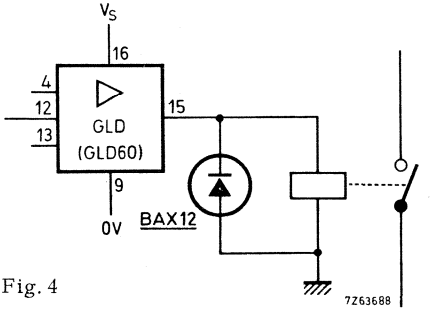


Fig. 4

2. High power grounded load drive. Fig. 5 shows how higher loads can be driven. This circuit permits load resistances down to 8, 6 Ω (corresponding to a load current of 3, 5 A at V_S = 30 V). The BDY60 is mounted on an aluminium heatsink of 150 cm^2, thickness 2 mm. For inductive loads a flywheel diode D (BYX30/50) is required.

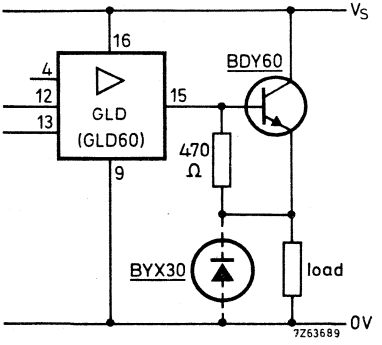


Fig. 5

*) Care should be taken not to apply a voltage > 1 V without current limiting resistance.

3. Short circuit protection of the GLD60.
If the load is short-circuited, the output transistor of the GLD60 can be damaged. This is prevented if the circuit depicted in Fig. 6 is applied. Too high a load current starts the BRY39 conducting. Consequently the input of the NOR goes "high" and its output "low", biasing input 4 of the GLD "low", in this way overruling the existing "high" on the system inputs. Once the BRY39 has started conducting, it will continue to do so until the push button is pressed.

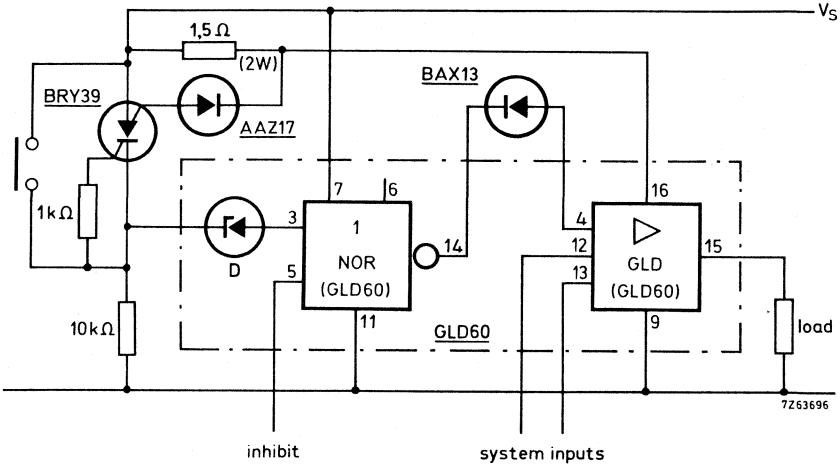


Fig. 6

B Monitoring and safeguarding twin channel systems

Fig. 7 shows the circuit build-up of a process control in which malfunctioning of one of the parallel identical logic systems or of the monitoring/safeguarding circuit causes an indication or switching to safe condition of the process to be controlled.
When the identical logic systems function properly their outputs are equal because their input conditions are identical. The equality of the outputs is monitored by the combination "2 x GLD60". Where parts of this monitoring combination are used in the channels before the point of comparison, they should be completely independent so that malfunction of one part in one channel cannot cause malfunction of the other part in the other channel. Consequently malfunction in this part of the monitoring combination will occur in one channel only and will have the same effect as malfunction of one of the logic systems. Similar considerations apply to the input connections of both logic systems.
Output V_{0A} can be used for power switching, and as an input condition for additional twin-channels (e.g. B_1 and B_2) in case the total control system comprises more twin channels.

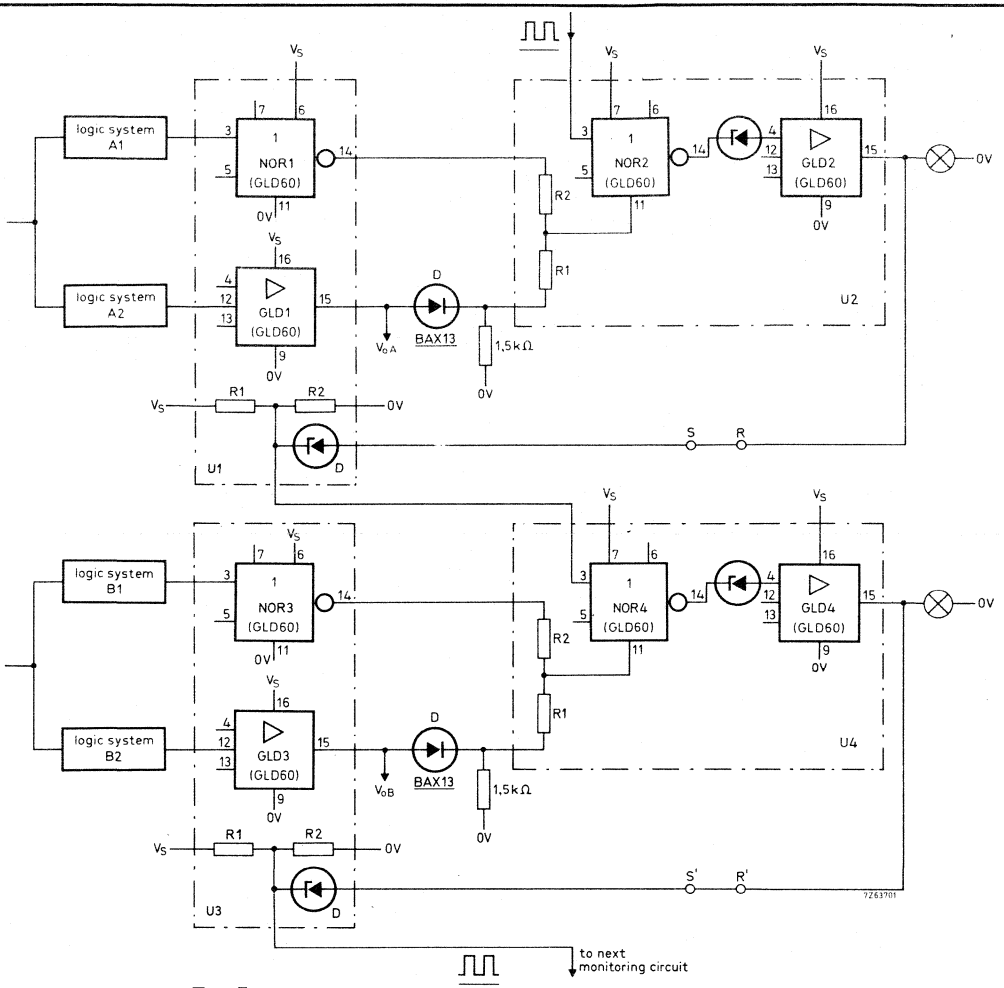


Fig.7

The actual circuit for comparing the outputs should be self-safeguarding which means that a malfunction should cause a fault indication, i.e. the part of the monitoring circuit between comparison circuit and pilot lamp has also to be monitored for malfunction. This is done by feeding a square wave to the input of this part, which is therefore monitored in a dynamic way. The output will alternate between on and off at the frequency of the square wave.

Malfunction of one of the components will cause a continuous on or off at the output. This also means that the pilot lamp is continuously monitored. Correct functioning of the whole system causes the pilot lamp to flicker (low square wave frequency e.g. 2 Hz) or to burn dimly (high square wave frequency e.g. 10 kHz).

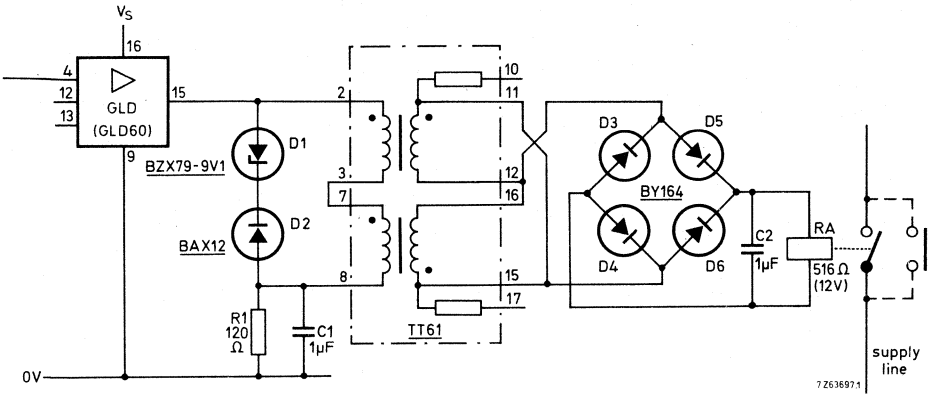


Fig. 8

The high frequency square wave output can also be fed via a transformer to a rectifier, see Fig. 8. Thus only a square wave output will cause a d.c. voltage which can be used to activate a relay. Any malfunction in the whole system will cause the relay to fall off and thereby switch the system to be controlled to a safe condition.

Note that if only one twin channel system has to be monitored or safeguarded the resistor of 1,5 kΩ and external diode BAX13 (Fig. 7) can be replaced by R2 and the voltage regulator diode inside unit U1.

The square wave interrogating signal fed to the monitor circuit should be symmetrical and vary between $V_S/3$ and V_S. Fig. 9 shows a suitable generator. The symmetry and the frequency are adjusted by means of the 10 kΩ potentiometer and the capacitor C respectively. Cycle time T = 1,5C ms approximately (C in μF).

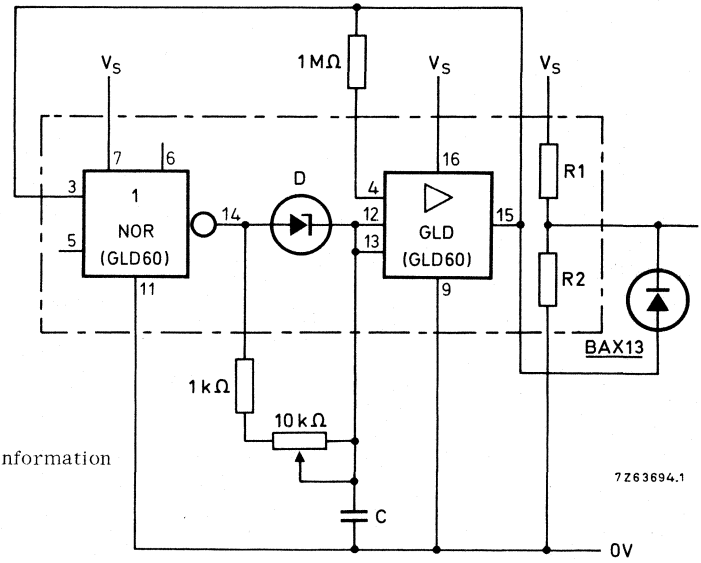


Fig. 9
Extended application information is given in A.I. 348.

61-Series NORbits

INTRODUCTION

The units of the 61-Series have been designed as an extension to the NORbit range in order to facilitate using NORbits in thyristorized power control circuits. By doing so, designers can cut system costs considerably: for one thing, the number of external components necessary will be reduced to a bare minimum, for another, mounting costs can be kept low as all units are housed in the NORbit size A encapsulation, and thus fit into a UMC60 chassis or can be fixed on the special printed-wiring boards for the 60-Series.
Furthermore, all units in the 61-Series offer the same outstanding features as those of the 60-Series, the chief ones being:

- high noise immunity
- rugged encapsulation with rigid terminals
- ample accessories
- single-rail 24 V ± 25% supply (except the DOA61)

The following units are available:

2.NOR61	Dual NOR-gate with diode-resistor networks
RSA61	Rectifier and synchronization assembly
UPA61	Universal power amplifier
DOA61	Differential amplifier
TT61	Dual thyristor trigger transformer.

For extended application information, see Application Book over the "61-Series".

Wiring Layout Stickers for the 61-Series are available under catalogue number 4322 026 71981.

UNIVERSAL POWER AMPLIFIER

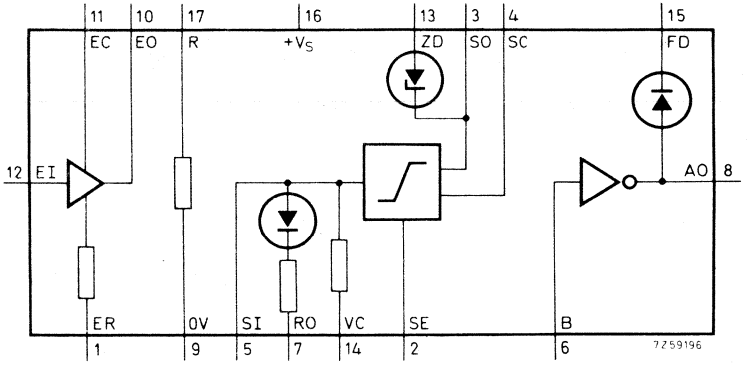
Function

1. D.C. switching amplifier.
2. Power oscillator for driving thyristor trigger transformers.
3. Phase shift module.
4. Current source for linear capacitor discharging.

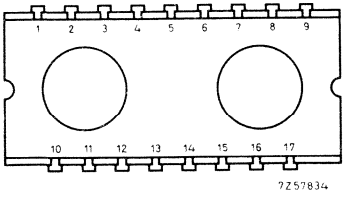
Case

Size: A; Colour: black.

CIRCUIT DATA



Quick reference circuit diagram

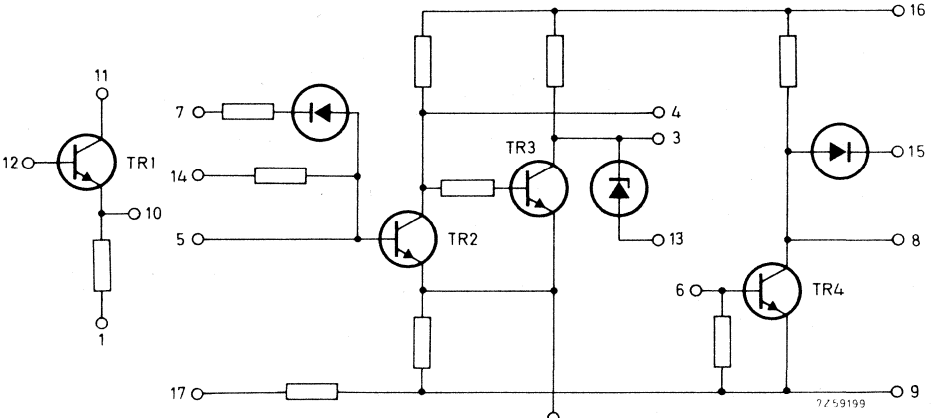


Terminal location

1 = emitter resistance follower
2 = emitter output Schmitt trigger
3 = output Schmitt trigger
4 = complementary output Schmitt trigger
5 = Schmitt trigger base input
6 = power stage base input
7 = oscillator feedback input
8 = power stage output
9 = 0 V common
10 = output emitter follower
11 = collector emitter follower
12 = base emitter follower
13 = restored "0" output Schmitt trigger
14 = input Schmitt trigger
15 = damping diode power stage
16 = supply voltage $+V_S$
17 = auxiliary resistor

Notes

1. For applications as a power amplifier with a min. permissible load resistance of 90 Ω, connect pin 13 to pin 6. A "1" at pin 14 will switch on the load between pins 8 and 16.
2. For applications as a power amplifier with a min. permissible load resistance of 30 Ω, connect pin 12, 13, 17 and 1 together, connect pin 10 to 6, and connect pin 11 to V_S via a resistor of 330 Ω, (2, 5 W).
   A "1" at pin 14 will switch on the load between pin 8 and 16.
3. The load should be connected between pins 8 and 16. To avoid destruction resulting from large voltage peaks occurring at switching off of inductive loads, the damping diode in the circuit block has to be connected across the load (15 to 16).
4. Incandescent lamps have a "cold" resistance that is only a fraction of the value calculated from nominal voltage and current, so that turning on of the lamp may cause a surge current. It is advisable to use a pre-heating quiescent current to eliminate destructive surge currents.



Circuit diagram

CHARACTERISTICS

Pins 6 and 13 connected, unless otherwise specified.

Supply	at V_S = +24 V ± 25%	at V_S = +12 V ± 5%
Supply current at I_{load} = 0 mA	≤ 110 mA	≤ 9 mA
Supply current at "1" input (pin 14) *) V_S = 30 V, R_{load} = 30 Ω	1100 mA	

*) Connections as in Note 2 above.

Input	at V_S = +24 V ± 25%	at V_S = +12 V ± 5%
Drive at pin 14 for switching on load current	2 D.U.	2 D.U.
Input impedance at pin 14	92 kΩ	92 kΩ
Input voltage for switching on load current at pin 5 **)	≥ 8.2 V	≥ 4 V
at pin 14	≥ 11.4 V	≥ 5.3 V
Input voltage for switching off load current at pin 5 **)	≤ 1.6 V	≤ 1 V
at pin 14	≤ 1.8 V	≤ 1.2 V
On-off input voltage difference, R_{source} = 2200 Ω, at pin 5	≤ 4.8 V	≤ 2.0 V
at pin 14	≤ 4.9 V	≤ 2.1 V
Max. source resistance for pin 5	250 kΩ	
for pin 14	200 kΩ	
Output		
Min. load resistance - connections Note 1	90 Ω	
- connections Note 2	30 Ω	
Output voltage at "1" input at min. load resistance - connections Note 1	≤ 0.3 V	
- connections Note 2	≤ 1.3 V	

Switching speed.

Switch off delay at 625 mA and 10 H with pin 15 connected to 16	t_d		480 ms
Fall time, connected as in Note 2	t_f	≤	0.5 μs
Rise time, R_L = 30 Ω, V_S = 30 V	t_r	≤	10 μs

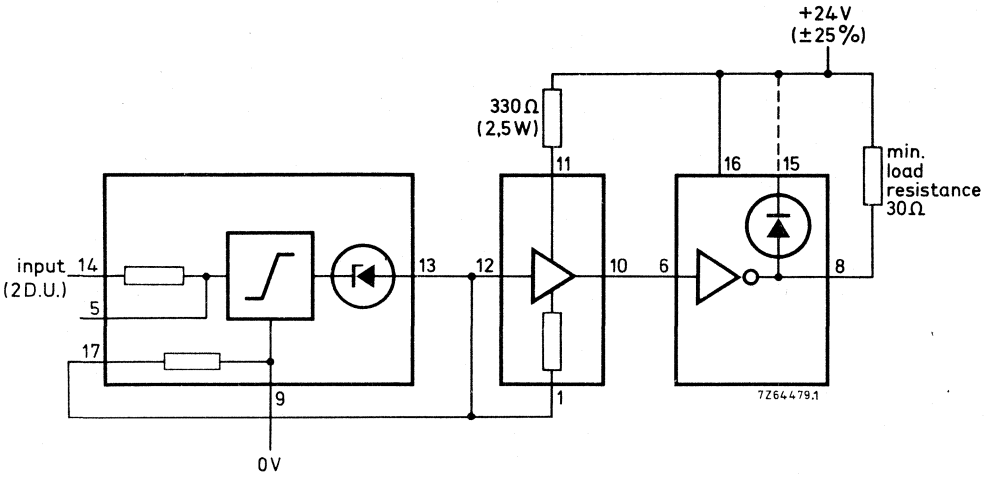
LIMITING VALUES

Supply voltage	V_S	max.	30 V
		min.	0 V
Positive transient on V_S, for 10 μs		max.	10 V
Input voltage at pin 14	$+V_{14}$	max.	70 V
	$-V_{14}$	min.	0 V
Input voltage at pin 5 via min. 2200 Ω	$+V_5$	max.	30 V
	$-V_5$	min.	0 V
Output current for 20 ms		max.	5 A
for 20 ms each second		max.	2 A

*) Connections as in Note 2
**) Via min. 2200 Ω

APPLICATION INFORMATION

UPA61 as 30 ohms load power amplifier.



DUAL TRIGGER TRANSFORMER

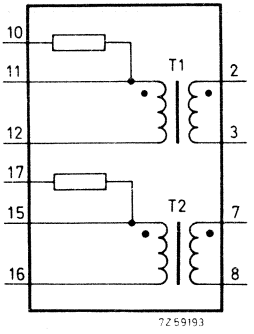
Function

Matching the pulse output from a power amplifier (e.g. UPA61) to thyristor gates.

Case

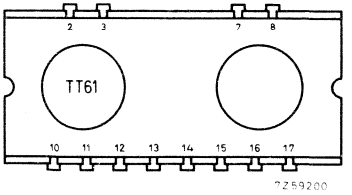
Size A; colour: black

CIRCUIT DATA



Circuit diagram

2. Secondary winding T_1 (cathode thyristor)
3. Secondary winding T_1 (gate thyristor)
7. Secondary winding T_2 (cathode thyristor)
8. Secondary winding T_2 (gate thyristor)
10. Resistance connected to primary winding T_1
11. Primary winding T_1 (driving source)
12. Primary winding T_1 ($+V_S$)
13. Not connected
14. Not connected
15. Primary winding T_2 (driving source)
16. Primary winding T_2 ($+V_S$)
17. Resistance connected to primary winding T_2



Terminal location

CHARACTERISTICS

→ Frequency range	3 to 50 kHz [1]
Turns ratio primary: secondary	3 : 1
Inductance of primary winding	≥2, 2 mH
Leakage inductance referred to primary (secondary short-circuited)	≤ 65 µH
Primary winding resistance at T_{amb} = 25 °C	≤ 4 Ω
Primary series resistor	82 Ω
Secondary winding resistance at T_{amb} = 25 °C	≤ 0, 6 Ω
Output pulse in response to step input, circuit of Fig. 3, R_{eq} = 15 Ω: rise time (from 0, 3 to 3 V) pulse duration, V_{pulse} = 3 V [1]	 ≤ 0, 6 µs ≥ 20 µs
Output current[2] at pins 2/3 (7/8) at T_{amb} = 25 °C in response to step input at pins 10/12 (16/17) (see Fig. 3): V_s = 18 V, R_{eq} = 15 Ω R_{eq} = 22 Ω V_s = 30 V, R_{eq} = 10 Ω R_{eq} = 15 Ω	 ≥200 mA ≥135 mA ≥425 mA ≥320 mA

LIMITING VALUES

Primary switched voltage across pins 10/12 (17/16)	max. 30 V [3]
Primary switched current no series resistor, duty cycle 1 : 3 max. 82 Ω internal, duty cycle 1 : 3 max. 39 Ω external, duty cycle 1 : 2 max.	 max. 800 mA max. 170 mA max. 200 mA
ET product per transformer primary at pins 11, 12 or 15, 16	600 Vµs
Peak pulse power per transformer for duty cycle 1:3, and T_{amb} = 25 °C [1]	17 W
D.C. test voltage between any pair of windings for 1 minute	4 kV
Continuous r.m.s. working voltage	max. 500 V

1) The minimum frequency has been specified with a view to core losses.
2) Minimum mean pulse magnitude over 20 µs.
3) If the UPA61 ceases to oscillate with the output transistor conducting, the primary series resistor may be damaged; circuit design must safeguard against this condition.

APPLICATION INFORMATION

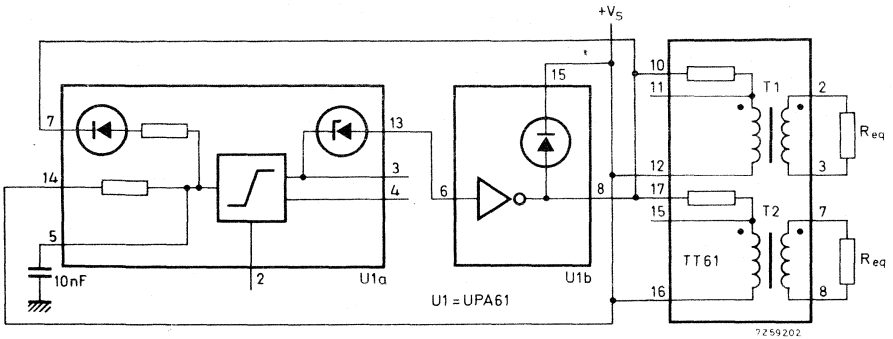


Fig. 3 Low power relaxation oscillator circuit (10 kHz)

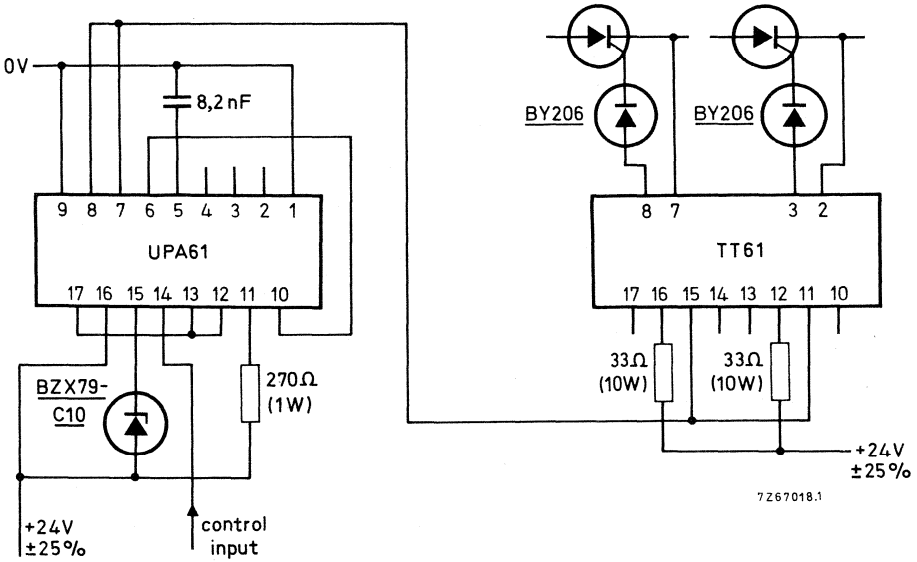


Fig. 4a High power relaxation oscillator circuit (10 kHz)

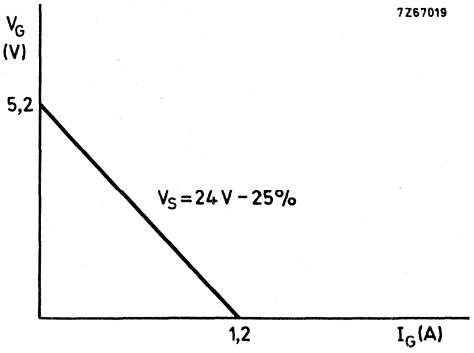


Fig. 4b Gate cathode thyristor voltage versus gate thyristor current

RECTIFIER AND SYNCHRONIZATION ASSEMBLY

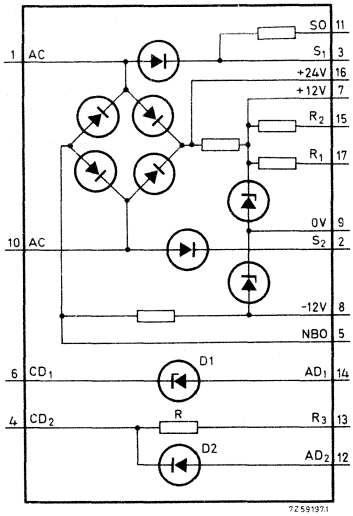
Function

- To provide an unregulated voltage of +24 V for Norbit systems
- To provide synchronization signals.
- To provide +12 V and −12 V (zener stabilized) for servo amplifiers.

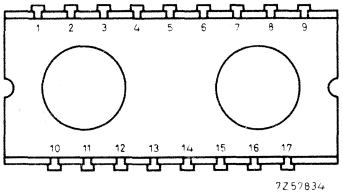
Case

Size: A; colour: black

CIRCUIT DATA



Circuit diagram



Terminal location

1 = A.C. input from supply transformer
2 = Synchronization voltage
3 = Synchronization voltage
4 = Cathode D_2
5 = Output rectifier bridge
6 = Cathode D_1
7 = +12 V output voltage
8 = −12 V output voltage
9 = 0 V from common supply
10 = A.C. input from supply transformer
11 = Synchronizing resistor output
12 = Anode D_2
13 = Resistor output cathode D_2
14 = Anode D_1
15 = +12 V, 150 kΩ source
16 = +24 V output voltage
17 = +12 V, 100 kΩ source

CHARACTERISTICS

Input

A.C. input voltage (r.m.s.)	2 x 20 V (+10, −15%)
A.C. input current	375 mA max.
Frequency	50 - 60 Hz
Source resistance	1 Ω min.
	4 Ω max.

Outputs

Pin number (9 connected to c.t. transformer)	Voltage	Current
16	+18 to +30 V	≤ 220 mA
7	+11 to +15 V	≤ 8 mA
8	−11 to −15 V	≤ 4 mA

In order to obtain the outputs specified, smoothing capacitors are required:

1. a 680 μF (−10, +50%), 40 V, capacitor connected between pins 16 and 9 to smooth the +24 V and +12 V.
2. a 100 μF (−10, +50%), 40 V, capacitor connected between pins 5 and 9 to smooth the −12 V.

Additional components

R : 2.2 kΩ; max. voltage 30 V r.m.s.

D2 : max. reverse voltage 30 V;
max. forward current 200 mA

D1 : nom. zener voltage 6.8 V;
max. dissipation 60 mW

LIMITING VALUES

Input voltage	2 x 22 V r.m.s.

APPLICATION INFORMATION

1. The output current of the −12 V output can be increased to 7 mA by connecting pin 4 to 5 and pin 8 to 13.
2. A mains synchronization signal is available at pin 11 when pins 3 and 2 are joined. The output at pins 2 and 3 takes the form of a zero voltage when the a.c. driving voltage passes through zero. At all other times a positive voltage is present on pins 2 and 3.

DUAL NOR-GATE WITH DIODE-RESISTOR NETWORKS

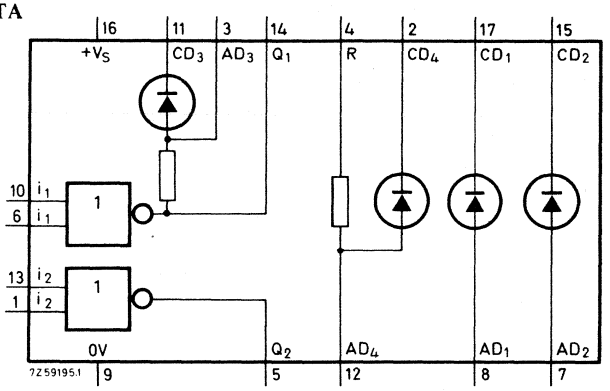
Function

Dual two-input transistor-resistor NOR-gate with diode gating facilities incorporated; specifically applicable as a d.c. counting/shifting stage.

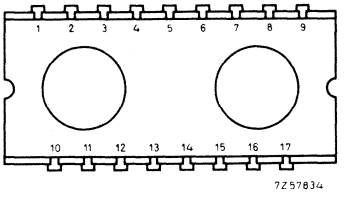
Case

Size: A; colour: black.

CIRCUIT DATA

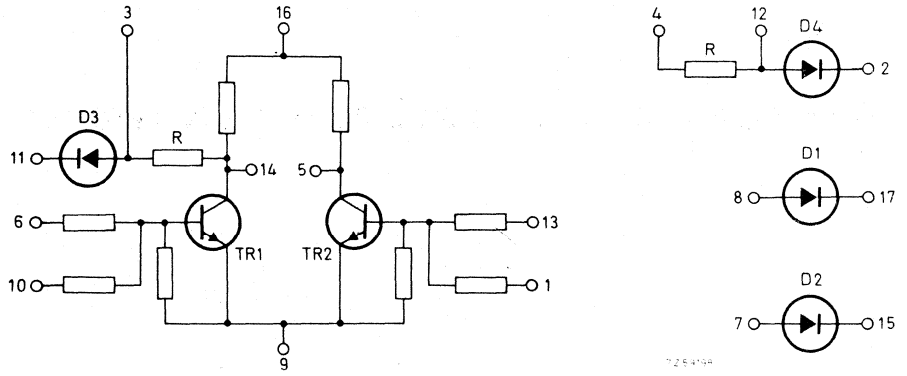


Quick reference circuit diagram



Terminal location

1 = Input NOR 2
2 = Cathode diode D_4
3 = Anode diode D_3
4 = Gate resistor
5 = Output NOR 2
6 = Input NOR 1
7 = Anode diode D_2
8 = Anode diode D_1
9 = 0 V common supply
10 = Input NOR 1
11 = Cathode diode D_3
12 = Anode diode D_4
13 = Input NOR 2
14 = Output NOR 1
15 = Cathode diode D_2
16 = $+V_S$ supply for NOR 1 and NOR 2
17 = Cathode diode D_1



Circuit diagram

CHARACTERISTICS

NOR-gate

	at V_S = 24 V ±25%	at V_S = 12 V ±5%
Supply current at V_S nom	5.6 mA	2.8 mA
at V_S max	7.2 mA	3.1 mA
Input requirement	2 D.U.	2 D.U.
Output capability	10 D.U.	6 D.U.

	pins 6, 13	pins 10, 1	pins 6, 10 and 13, 1 in parallel
Input impedance [1])	63 kΩ	47 kΩ	32 kΩ
Input current for "0" output [1]) [2])	92 μA	86 μA	75 μA

Switching speed

Fall time	$t_f \leq 1.5\ \mu s$
Fall delay time	$t_{fd} \leq 6\ \mu s$

Diode-resistor networks

Resistors R (22 kΩ) can be used as a load of 4 D.U. in a logic Norbit system.

[1]) Not used inputs returned to 0-volt line .
[2]) At V_S = 30 V

LIMITING VALUES

Supply voltage V_S	max.	+30	V
	min.	0	V
Positive transient on V_S	max.	10	V for 10 μs
Positive input voltage $+V_i$	max.	70	V
Negative input voltage $-V_i$	max.	15	V
Reverse voltage of diodes	max.	50	V
Forward current of diodes	max.	75	mA
Repetitive peak forward current of diodes	max.	150	mA
Dissipation of resistor R	max.	50	mW

DIFFERENTIAL AMPLIFIER

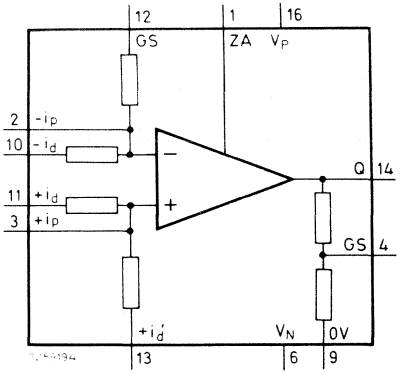
Function

Amplification, loop shaping and comparison with reference signals in analogue closed-loop systems. Many other applications are possible with the operational amplifier incorporated.

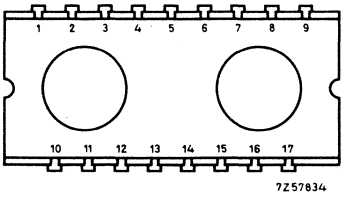
Case:

Size: A; colour: black

CIRCUIT DATA



Quick reference circuit diagram



Terminal location

1 = zero output voltage adjustment
2 = inverting input operational amplifier
3 = non-inverting input operational amplifier
4 = gain selection (100 x)
5 = n.c.
6 = negative supply voltage V_N
7 = n.c.
8 = n.c.
9 = 0 V common
10 = inverting input difference amplifier
11 = non-inverting input difference amplifier
12 = gain selection (10 x)
13 = 100 kΩ non-inverting input operational amplifier
14 = output and gain selection
15 = n.c.
16 = positive supply voltage V_p
17 = n.c.

CHARACTERISTICS

Ambient temperature range

Operating	0 to +70 °C
Storage	-40 to +85 °C

Power Supply

Supply voltages	V_p = +12 V V_N = -12 V	V_p = +15 V V_N = -15 V
Supply currents for I load = 0 mA	I_p = 2.2 mA I_N = 2.2 mA	I_p = 2.7 mA I_N = 2.7 mA

The circuit has been protected against reverse connection of supply voltages.

Voltage gain

With feedback, from input (pin 10) to output (pin 14)	
a. pin 12 connected to pin 14	10 x
b. pin 12 connected to pin 4	100 x
Without feedback, from input (between pins 2 and 3) to output (pin 14) - typical	32 000 | 45 000

Frequency response

The operational amplifier has a frequency response of 6 dB/oct, with unity gain bandwidth (for small signals)	1 MHz
3 dB down frequency for gains of 10 and 100 (at rated output voltage swing)	10 kHz

Rejection ratio

Connected as a difference amplifier with gain of 10 (inputs pin 10 and 11)	
- of supply voltage variations	to be established
- of common mode signals	to be established

Input

Minimum input voltage range, when connected as a difference amplifier with a gain of 10 (input pins 10 and 11)

common mode	± 7 V	± 10 V
differential voltage (for zero common mode voltage)	± 17 V	± 20 V

Circuit has been protected against too high voltages between the inputs of the operational amplifier.

Input resistance

-inverting input (pin 10)	10 kΩ
-non-inverting input (pin 11)	110 kΩ

Input voltage offset

Initial offset can be adjusted to zero with a potentiometer of 100 kΩ connected between 0 V line and positive supply voltage and the wiper connected to pin 1.

Equivalent input voltage offset drift with temperature (typ.)	10 μV/degC

Output

Minimum output voltage swing

at R_L = 10 kΩ	± 9 V	± 11 V
at R_L = 2 kΩ	± 7 V	± 9 V
Output current	≥ 5 mA	≥ 6 mA

Output resistance	
for a gain of 10	≤ 0,3 Ω
for a gain of 100	≤ 3 Ω
Maximum capacitive load	1 nF
Slewing rate (change of output voltage in response to step input voltage)	to be established

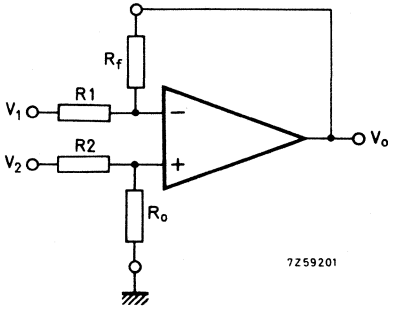
The output may be shorted to earth for any length of time.

APPLICATION INFORMATION

As shown, the DOA61 consists of an operational amplifier and feedback networks for closed loop gains of 10 and 100 times. Other gains can be obtained by applying one or more external resistors.

According to operational amplifier theory the transfer function of an amplifier with feedback networks as shown in the circuit diagram is given by

$$V_o = V_2 \frac{R_o}{R_1} \cdot \frac{R_1 + R_f}{R_o + R_2} - V_1 \frac{R_f}{R_1}$$ (See circuit below)



For $\frac{R_o}{R_2} = \frac{R_f}{R_1}$ the function can be simplified to: $V_o = \frac{R_f}{R_1} (V_2 - V_1)$

Networks incorporated into the circuit block are providing a difference amplifier, with a gain of 10 x.

Accessories for NORbits

SURVEY

MODULES

TT60 2722 032 00051	Dual thyristor trigger transformer for producing, in conjunction with a PA60, two pulse currents of up to 400 mA.	
	Turns ratio pr. : sec. : sec.	3 : 1 : 1
	Dimensions (incl. pins)	34 x 34 x 49 mm
DCT61 9360 000 40000	Direct current transformer provides the linear conversion of a high d.c. current to a low d.c. voltage.	
	Input current range	0 to 160 A
	Output voltage range	0 to 15 V
	Dimensions	80 x 30 x 56 mm
SIM60 4322 026 38301	Logic simulator for 60-Series NORbits	
	Supply voltage	117/220/240 V; 50 or 60 Hz
	Housing	attaché case, 415 x 310 x 95 mm

POWER SUPPLY UNITS

LSU60 4322 000 01000 4322 000 01010	Power supply unit for small logic systems with 60-Series NORbits, to be built in chassis UMC60.	
	Input 01000 version	220 V, 45-400 Hz
	Input 01010 version	110 V, 45-400 Hz
	Output (d.c.)	150 mA, >18 V; 0 mA, <30 V
	Board dimensions	90 x 83 mm
PSU60 2722 151 00041 PSU61 2722 151 00051	Power supply units for 60-Series NORbits.	
	Input	240 V, 47-440 Hz
	Output (d.c.)	500 mA, >18 V; 0 mA, <30 V
	Extra d.c. output PSU61	100 V, 25 mA
	Dimensions	146 x 76 x 77 mm

MAINS FILTERS

MF 0,5 A 9390 213 00002	Mains filter for control systems consuming less than 0,5 A a.c.	
	Attenuation 0,1 - 10 MHz	50 dB
	A.C. limits	250 V, 0,5 A
	Dimensions	88 x 38 x 39 mm
MF 2,4 A 9390 253 30142	Mains filter for control systems consuming less than 2,4 A a.c.	
	Attenuation 0,5 - 10 MHz	40 dB
	A.C. limits	250 V, 2,4 A
	Dimensions	105 x 62 x 44 mm

CHASSIS AND HOLDERS

BB60 9390 198 00002	Breadboard block to hold 1 size A unit and to interlock with other BB60 blocks for easy assembly of circuits for teaching purposes.	
	Dimensions	56 x 38 x 14 mm
UMC60 4322 026 38330	Universal mounting chassis for 6 size A or 3 size B blocks or combination.	
	Material	plastic
	Dimensions	245 x 95 x 28 mm

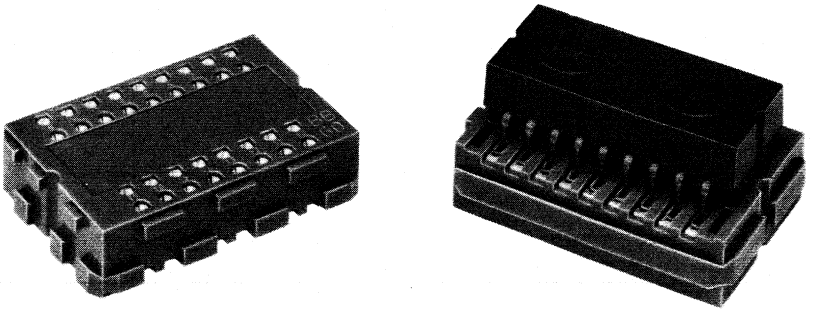
PRINTED–WIRING BOARDS

GPB60 4322 026 38600	Experimenters' printed-wiring boards	
GPB60/P 4322 026 38610	Material GPB60	glass-epoxy
	Material GPB60/P	phenol paper
	Accommodation	10 size A or 4 size B blocks
	Mating connector	F045 (0.2")
PWB60 4322 026 38790	Experimenters' printed-wiring board provided with 0 V tracks	
PWB60/P 4322 026 38800	Material PWB60	glass-epoxy
	Material PWB60/P	phenol paper
	Accommodation	10 size A blocks
	Mating connector	F047, F050, F053 (0.156")
PWB61 4322 026 38810	Experimenters' printed-wiring board provided with 0 V tracks	
	Material PWB61	glass-epoxy
	Material PWB61/P	phenol paper
	Accommodation	10 size A blocks
	Mating connector	F045 (0.2")
PWB62 4322 026 38780	Printed-wiring board with complete F054 connector, with 0 V and + tracks	
	Material	glass-epoxy
	Accommodation	4 size A or 2 size B blocks
PWB63 4322 026 73750	Printed-wiring board for use in UMC60.	
	Material	glass-epoxy
	Accommodation	6 size A or 3 size B blocks

STICKERS (drawing symbols on self-adhesive transparent material)

4322 026 36481	50 sheets of stickers for 60-Series Norbits (without 4.NOR60).
4322 026 71941	50 sheets of stickers for 60-Series Norbits (without 4.NOR60).
4322 026 71961	50 sheets of stickers for 60-Series Norbits (incl. TT60).
4322 026 71971	50 sheets of wiring layout stickers for 60-Series Norbits. Actual-size pin distances.
4322 026 71981	50 sheets of wiring layout stickers for 61-Series Norbits. Actual-size pin distances.

BREADBOARD BLOCK
for 60-series NORBITS

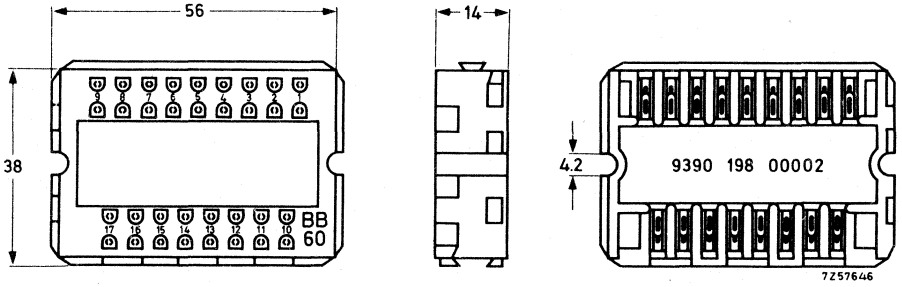


RZ 27447-18

APPLICATION

The "Breadboard Block", BB60, has been produced as an aid to 60-Series logic system design. Each block takes one size A unit from the 60-Series, and each block can be firmly locked on any of its edges to another BB60 block, thus a breadboard base can be built up to accommodate any size and complexity of logic circuit, interconnections being simply made with hook-up wire plugged into cup-shaped contacts. The BB60 blocks are ideal as experimenting and teaching aids. For instance, with four units 4. NOR60, one unit TU60 and one unit 2. LPA60 mounted on a base of six blocks BB60, it is easy to realize a large number of instructive logic circuits. Such a base of six blocks can be mounted in the Universal Mounting Chassis UMC60.

DESCRIPTION



(Dimensions in mm)

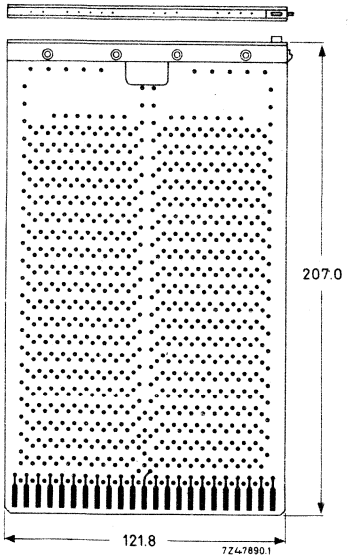
The right figure shows the underneath of the block with the 2 x 17 soldering lugs; the 60-Series units can be soldered directly onto these lugs. In the top view the cup-shaped contacts are visible; interconnecting wires or discrete components such as resistors can be plugged in on this side. There are two contacts for each terminal of a 60-Series unit, which facilitates multiple connections.

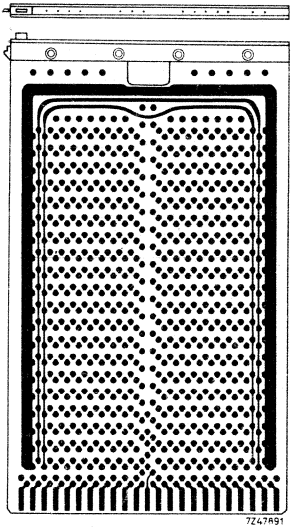
Body material	rigid grey plastic
Contacts	cup shaped, silver plated, suited for wires up to 1 mm diameter
Weight	20 g
Delivery	in packs of six, plus six sheets of wiring lay-out stickers for the 60-Series units.

The stickers are drawing symbols on self-adhesive transparent material, and they can be stuck to the top side of the breadboard blocks or be used for circuit drawings. The catalogue No. of a sheet is 9399 269 15301.

EXPERIMENTERS' PRINTED-WIRING BOARD

Experimenters' printed-wiring board (with extractor) with plated-through holes suitable for 60-Series NORbits.





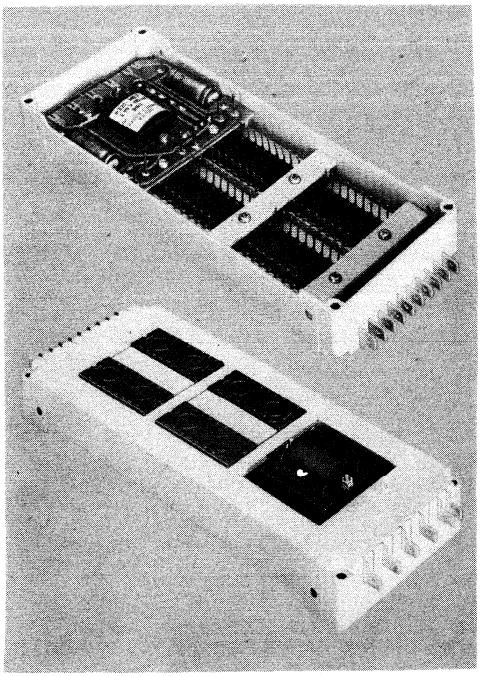
Accommodation of NORbits

size A + size B (HPA60)	
10	0
8	1
6	2
3	3
0	4

Material of version GPB 60	glass-epoxy
of version GPB 60/P	phenol paper
Hole diameter	1,2 mm
Contacts	2x23, gold plated, pitch 0,2"
Mating connector	2422 020 52591 (type F045)

For more information, see Application Note "Printed-wiring boards for 60-Series Norbit Assemblies", No. 32/522/BE.

LOGIC SUPPLY UNIT



RZ 27077-11
RZ 27077-8

LSU60 mounted in UMC60

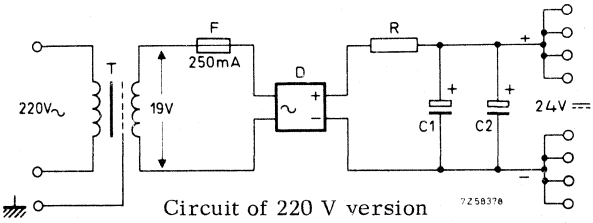
APPLICATION

The LSU60 is a power supply unit for small systems with 60-series NORbits. It is intended to be mounted in the universal mounting chassis UMC60. There is a version for 220 V mains (4332 000 01000) and one for 110 V mains (4332 000 01010).

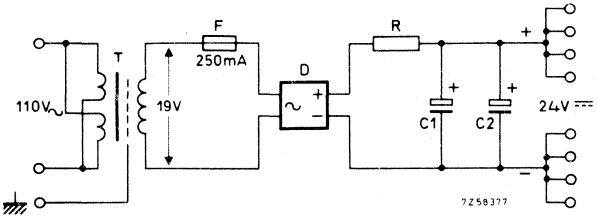
DESCRIPTION

The unit takes the same place as a size B Norbit block (HPA60). To mount the unit in the UMC60, the material between the two adjacent size A holes in the chassis should be removed, after which the unit can be fixed with 4 self-tapping screws.
Slots in the board of the LSU60 facilitate the connection of the input voltage and the output voltage to the Fastons of the UMC60, for external connection to the chassis. The other three pairs of output terminals are soldering tags intended for connection to Norbit blocks on the chassis. A 250 mA fuse (F) is inserted in the secondary part of the circuit. Its catalogue number is 4822 253 20011.

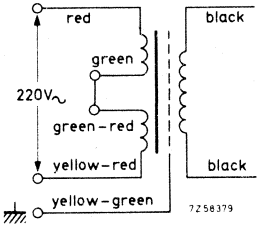
Circuit



Circuit of 220 V version



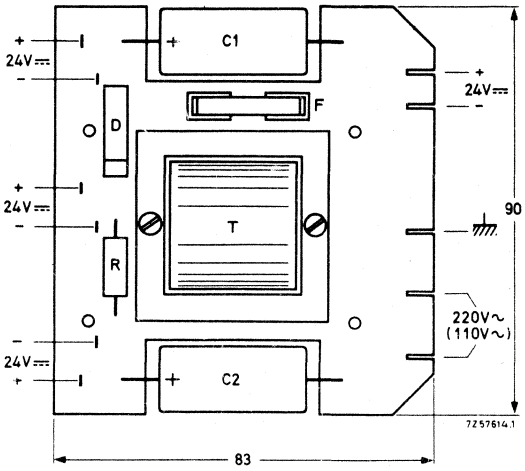
Circuit of 110 V version



Transformer of 110 V version changed for 220 V.

Outline and connections

Dimensions in mm



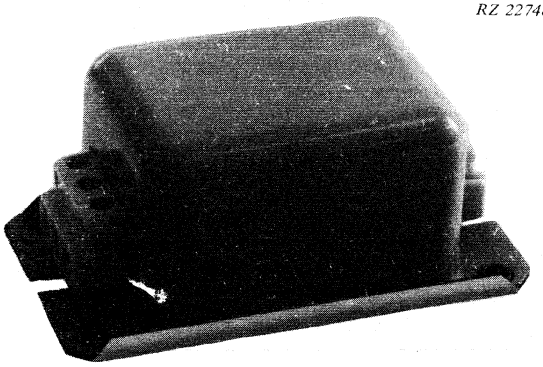
Weight approx 250 g

ELECTRICAL DATA

Input voltage	
version 4332 000 01000	220 V a.c., +10%, −15%
version 4332 000 01010	110 V a.c., +10%, −15%
Input frequency	45 to 400 Hz
Output voltage at 0 mA	< 30 V d.c.
at 150 mA	> 18 V d.c.
Temperature range	−10 to +70 °C
Test voltage for 1 min,	
across input terminals and earth	2 kV r.m.s.
across output terminals and earth	2 kV r.m.s.

0.5 A MAINS FILTER

RZ 22748-2



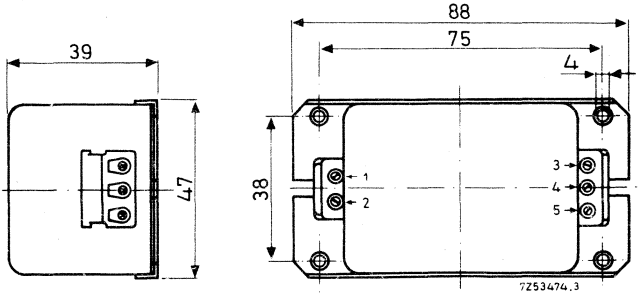
APPLICATION

This mains filter is intended for use between mains supply connection terminals and the mains inputs of control systems consuming less than 0.5 Amp. to provide an attenuation of 50 dB for frequencies between 100 kHz and 10 MHz.

CONSTRUCTION

Unit is potted in a metal housing.

Dimensions in mm



Weight: 280 g

TECHNICAL PERFORMANCE

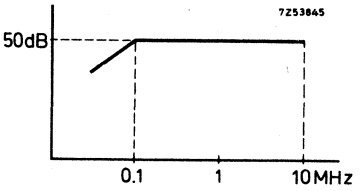
Maximum a.c. input voltage	250 V
Maximum a.c. current at T_{amb} = 40 °C	0,75 A
at T_{amb} = 70 °C	0,5 A
Maximum surge current (20% duty cycle)	2,5 A
Insulation resistance between terminals and case	> 5 MΩ
Test voltages	
a) for 1 min. across terminals and case	3500 V d.c.
b) for 2 s across terminals 1 and 2, or 3 and 5	1625 V d.c.
c) for 2 s across terminals 3 and 4, or 4 and 5	1800 V a.c., 50 Hz
Operating temperature range	−25 to +70 °C
Storage temperature range	−25 to +85 °C

TEST SPECIFICATIONS

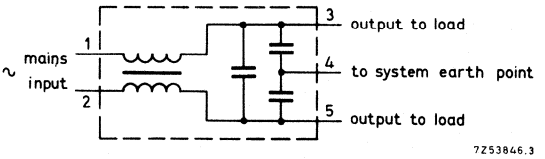
The filter has been designed to meet the tests of MIL-STD-202D

1. Thermal shock test according to method 107B, 5 cycles from −25 to +85 °C
2. Moisture resistance test according to method 106B
3. Humidity test according to method 103B, condition D 40 °C, 90 to 95% R.H.

Attenuation



Circuit diagram



2,4 A MAINS FILTER

APPLICATION

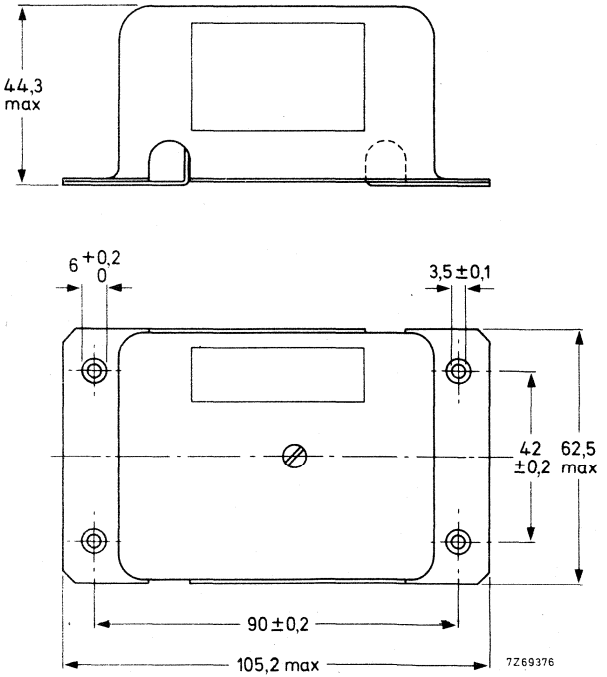
This mains filter can be used:
- either between mains supply connection terminals and the mains inputs of control systems, to suppress malfunctioning by transients,
- or between transient-generating equipment and its supply, to prevent high-frequency interference entering into the mains.

The attenuation for frequencies between 0,5 and 10 MHz, at 2,4 A supply current is 40 dB.

CONSTRUCTION

The unit is encapsulated in a metal housing.

Dimensions in mm

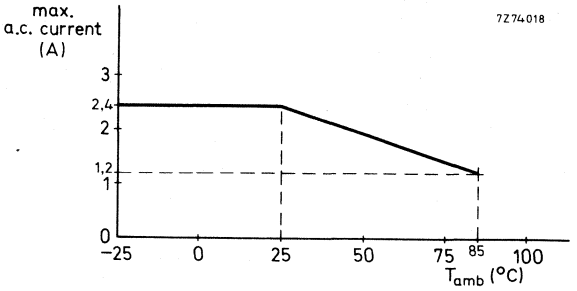


Weight: 275 g

ELECTRICAL DATA

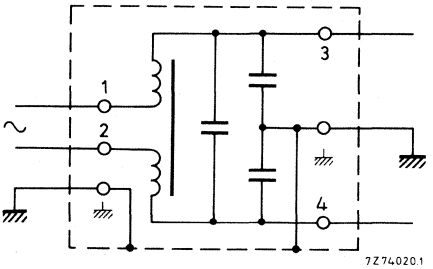
The values given below apply only to filters which are used in earthed installations.

Maximum input voltage	250 V a.c.
Maximum current at T_{amb} = 25 °C	2,4 A a.c.
at T_{amb} = 85 °C	1,2 A a.c.



Repetitive peak current, 50 Hz	≤ 10 A
Non-repetitive peak current for 2 s	≤ 10 A
Impedance at 2,4 A	0,925 Ω
Insulation resistance between terminals and case	> 5 MΩ
Test voltage	
for 2 s between terminals and case	2700 V d.c.
for 2 s between input or output terminals	1625 V d.c.
Attenuation between 0,5 and 10 MHz	> 40 dB

Circuit diagram



Operating and storage temperature range −25 to + 85 °C

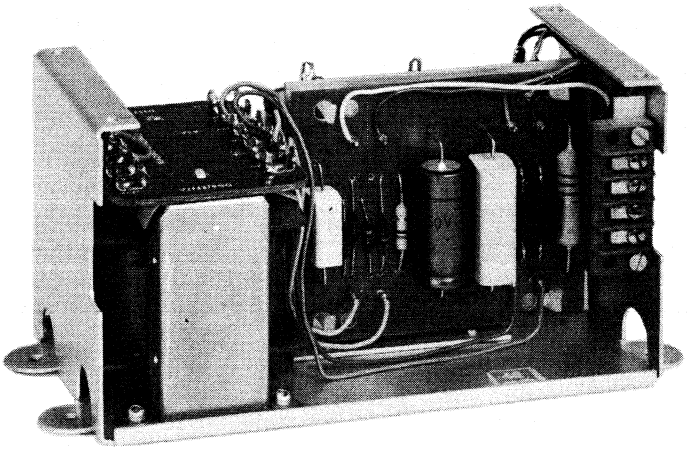
TEST SPECIFICATIONS

The filter meets the tests of MIL-STD-202E:

- thermal shock test according to method 107D, 5 cycles from −25 to + 85 °C
- moisture resistance test according to method 106D

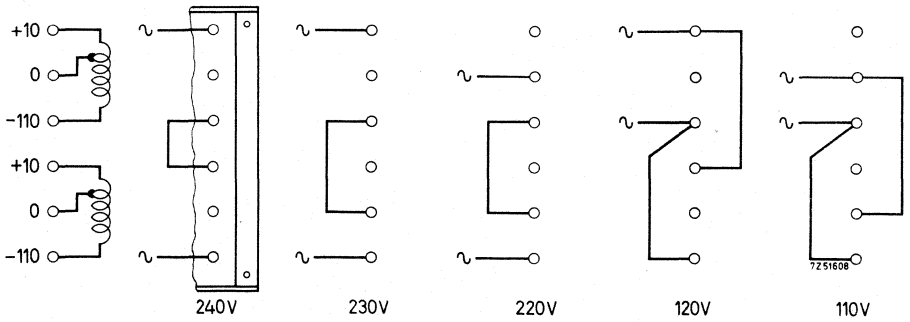
The capacitor used meets the requirements of VDE 0560-7.

POWER SUPPLY UNITS
for 60-series NORBITS

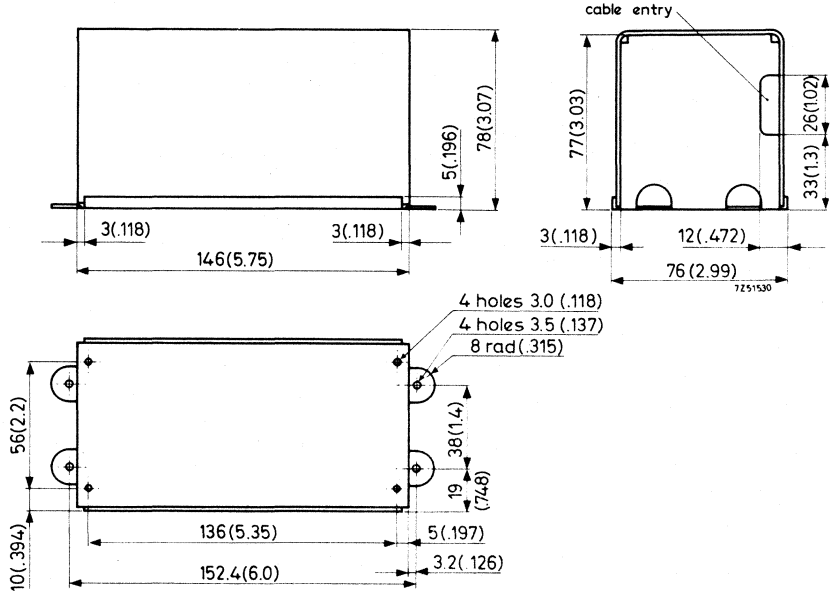


(Cap removed from unit.) RZ 23469-1

Input voltage	240, 230, 220, 120 or 100 V_{ac}, +10%, -15%
Input frequency	47 to 440 Hz
Output	< 30 V at 0 mA, > 18 V at 500 mA (for logic supply)
Additional output PSU 61	+100 V ±25% at 0 to 25 mA (for Switch Filters)
Operating ambient temperature	-10 to +60 °C
Test voltage between windings	2 kV



Input facilities of mains transformer



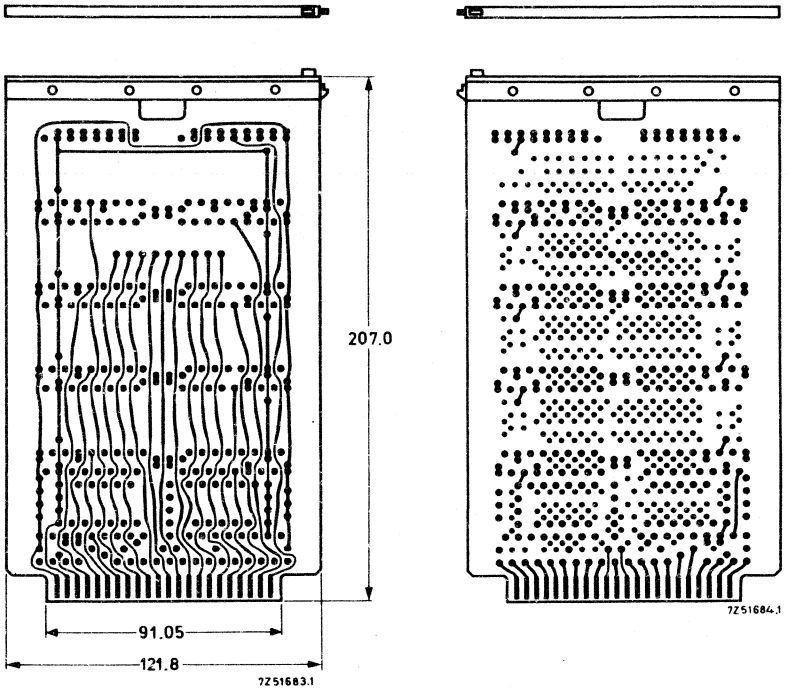
Dimensions in mm, inch values between brackets.

Case: aluminium

Weight: approx. 1000 g

EXPERIMENTERS' PRINTED-WIRING BOARDS for 60-series NORBITS

Experimenters' printed-wiring boards (with extractor) with plated-through holes, and 0-volt supply line tracks for pins 9 and 16.

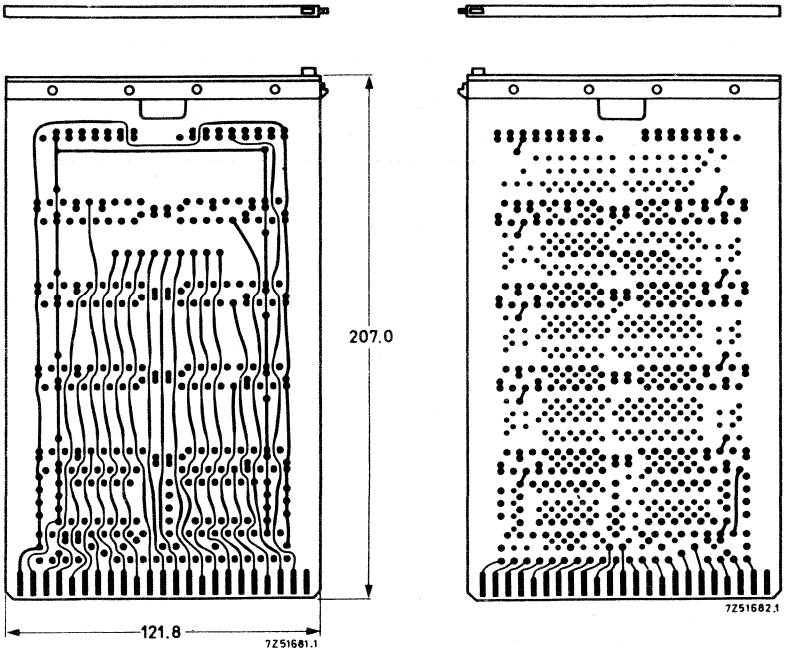


Accommodation	ten blocks size A
Material of version 4322 026 38790 of version 4322 026 38800	glass-epoxy (PWB 60) phenol paper (PWB 60/P)
Hole diameter	1.3 mm
Contacts	2x22, gold plated, pitch 0.156"
Mating connector	types F047, F050, F053

For more information, see Application Note "Printed-wiring boards for 60-series Norbit Assemblies", No. 32/522/BE.

EXPERIMENTERS' PRINTED-WIRING BOARDS
for 60-series NORBITS

Experimenters' printed-wiring boards (with extractor) with plated-through holes, and 0-volt supply line tracks for pins 9 and 16.



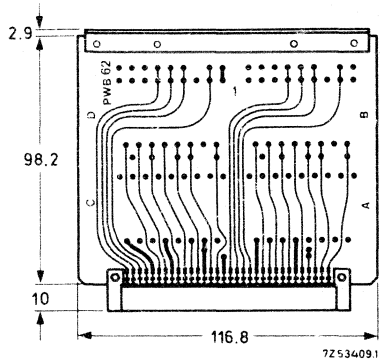
Accommodation	ten blocks size A
Material of version 4322 026 38810 of version 4322 026 38820	glass-epoxy (PWB 61) phenol paper (PWB 61/P)
Hole diameter	1.3 mm
Contacts	2x23, gold plated, pitch 0.2"
Mating connector	2422 020 52591 (type F045)

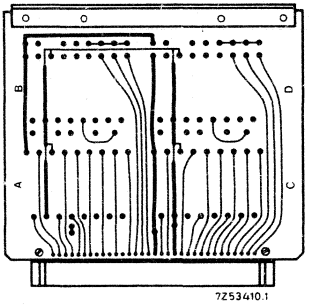
For more information, see Application Note "Printed-wiring boards for 60-series Norbit Assemblies", No. 32/522/BE.

PRINTED—WIRING BOARD
for 60—series NORBITS

Printed-wiring board with plated-through holes, extractor and complete F054 connector, of which the female part has been soldered to the board. All terminals of any Norbit mounted on the board are brought out. The 0-volt pins and the positive supply pins have been tracked together for all Norbits.

The board is especially useful for systems where a small number of types (board + blocks) is essential with a view to replacement.





Accommodation	size A + size B (HPA60)
	4 | 0
	2 | 1
	0 | 2
Material	glass-epoxy
Hole diameter	1.2 mm
Connector	
type	F054 (2422 025 89082)
contacts	2 x 32
contact pitch	2,54 mm (0,1")
terminations	suitable for mini wire-wrapping

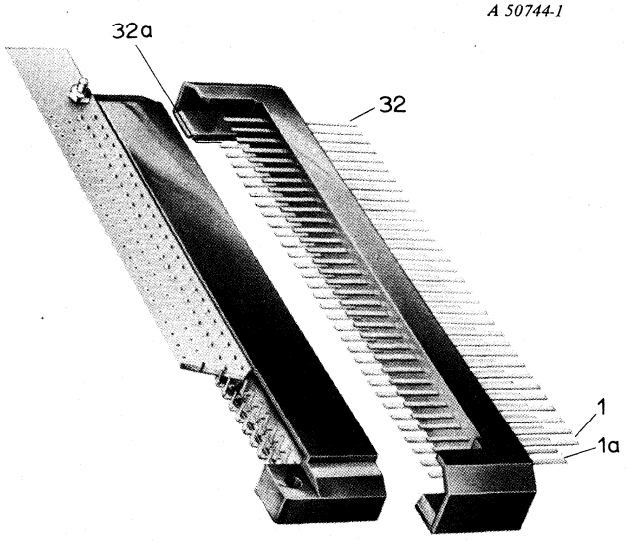
INTERCONNECTION DIAGRAM

The designer of an electronic circuit with Norbits mounted on PWB62 boards, can easily derive the necessary connecting instructions from the diagram depicted on the next page. With this diagram he can indicate the connections that are to be made. The diagram gives the numbers of the terminals of the circuit block, its position on the PWB62 and the numbers of the connector terminals (see photograph below).
The thin lines in the diagram represent the tracks of the printed circuit on the PWB62, so they indicate the interconnections between the Norbit terminals, and the connector pins.

All the designer has to do is to draw the connections which should be made by the wire man (see thick lines on the second diagram).

As an example we give an alarm circuit of which the designer has drawn the diagram in the upper part, and has indicated for the wire man on the lower part the external interconnections to be made. Moreover, outside the diagram the necessary connections to be made the supply with unit, the oscillator, switches, and so on, are indicated by the arrows.

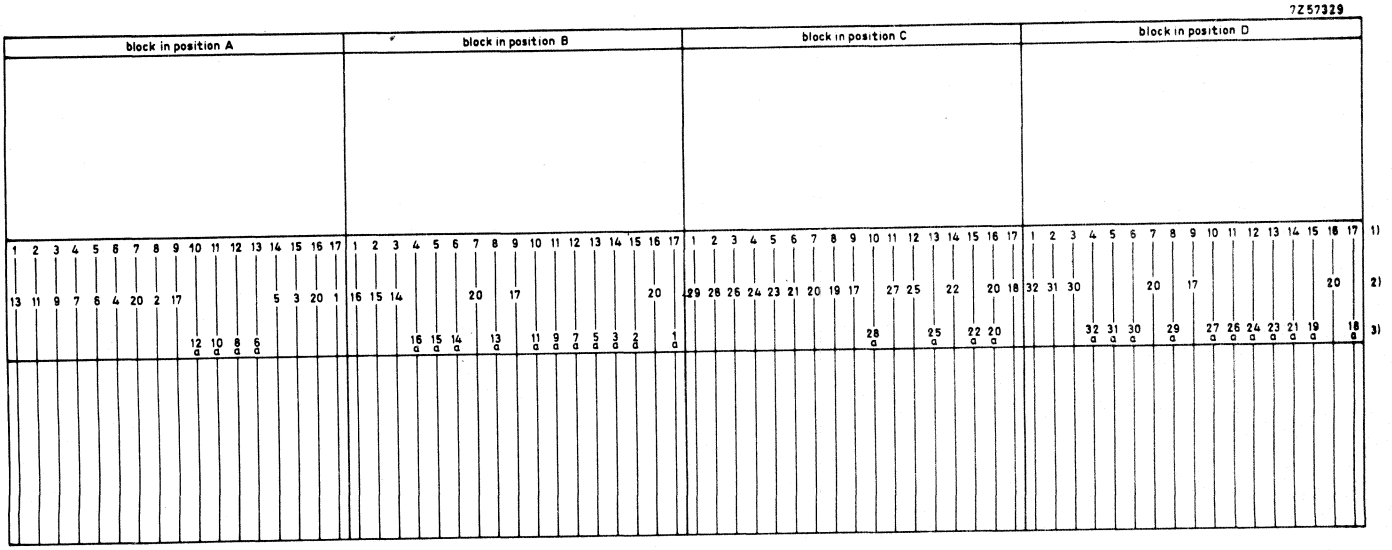
In this way the design engineer can draw the electronic circuit and the associated assembly instructions in one diagram.



Connector pin numbering as used in Interconnection Diagram.

Interconnection diagram (containing track data)

See example next page.

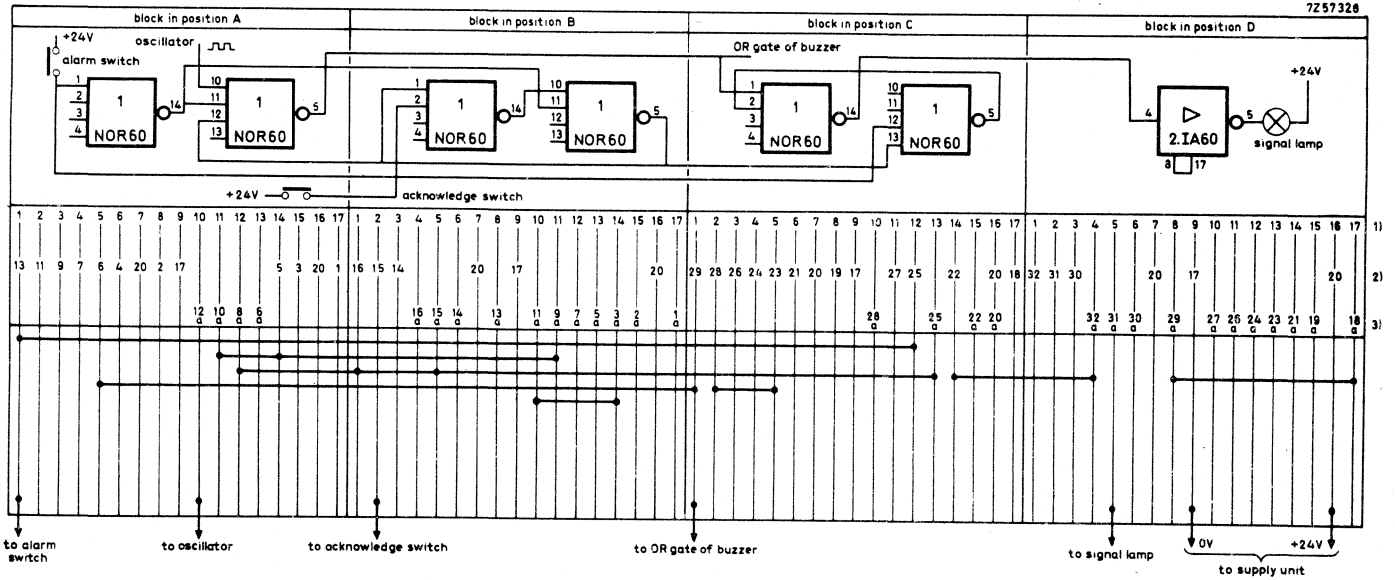


1) Terminal number of circuit block inserted in PWB62

2) Pin number of male F054 connector (see photograph) to which track on the "solder side" (bearing no type number) is connected.

3) Pin number of male F054 connector (see photograph) to which track on the "components side" (bearing type number) is connected.

Example

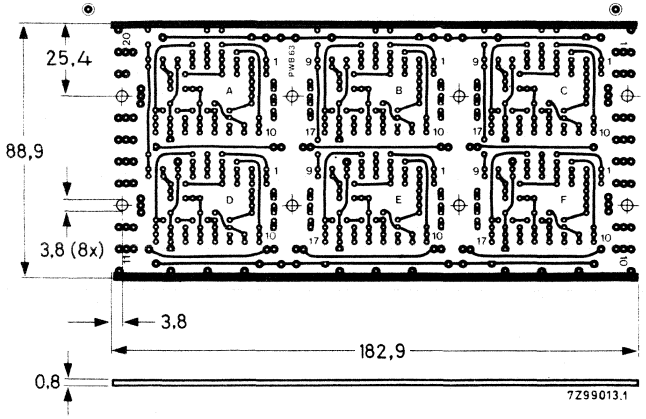


1) Terminal number of circuit block inserted in PWB62

2) Pin number of male F054 connector (se photograph) to which track on the "solder side" (bearing no type number) is connected

3) Pin number of male F054 connector (see photograph) to which track on the "components side" (bearing type number) is connected.

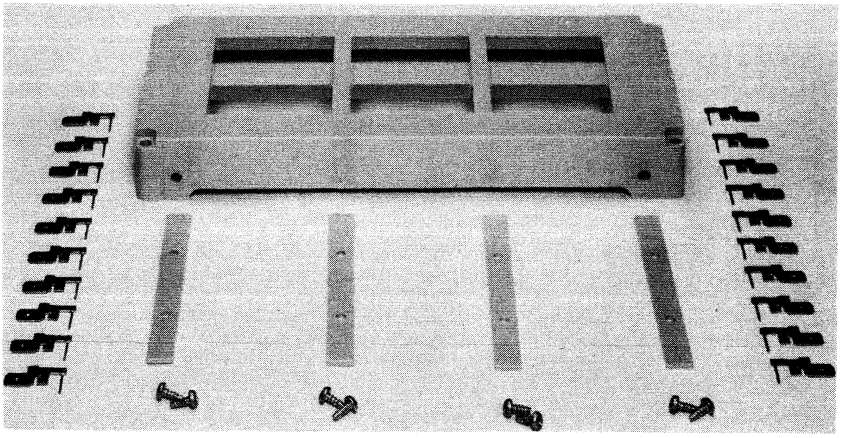
PRINTED-WIRING BOARD for UMC60



Single-sided printed-wiring board (with holes) intended for use in a Universal Mounting Chassis UMC 60.
Tracks have been laid such that only short jumpers need be used to obtain all kinds of logic functions with Norbits.

Accommodation (60-series blocks)	6 size A or 4 size A + 1 size B (IIPA60) or 2 size A + 2 size B or 3 size B
Material	glass-epoxy
Board thickness	0,8 mm
Hole diameter	1,2 mm

UNIVERSAL MOUNTING CHASSIS
for 60-series NORBITS



RZ 26441-7

APPLICATION

Low cost mounting facility for:

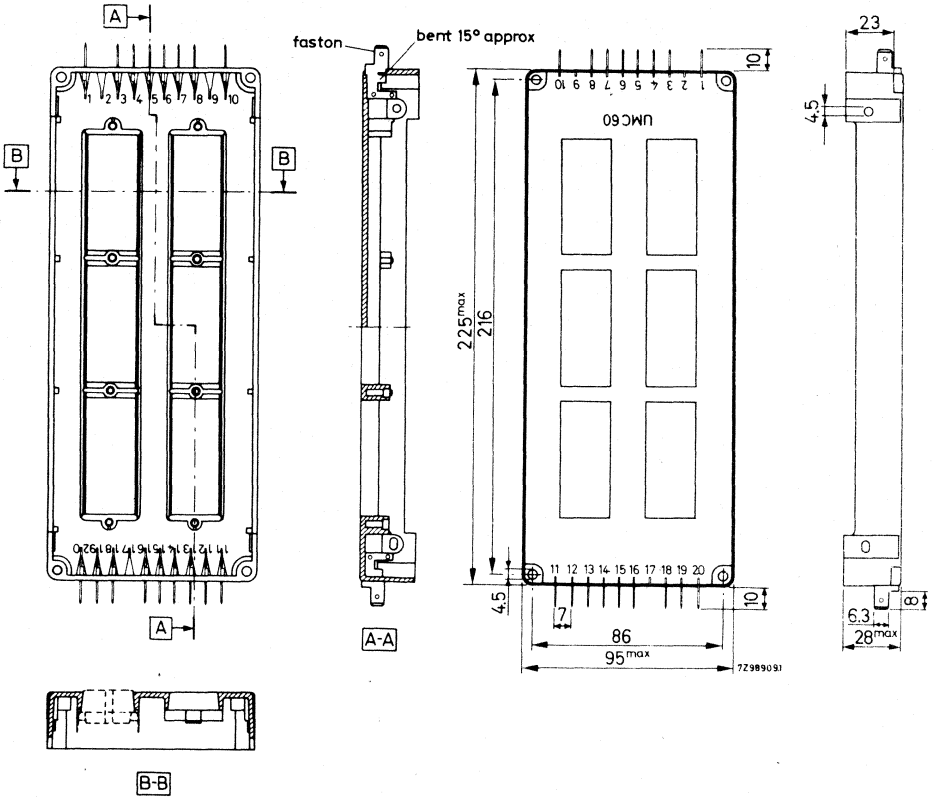
6 size A blocks,
or 4 size A blocks and 1 size B block (HPA60)
or 2 size A blocks and 2 size B blocks
or 3 size B blocks.

The chassis provides an alternative for mounting 60-series blocks on a printed-wiring board with connector.
Chassis can be bolted together side by side (Fig.4); they may also be stacked (Fig.5 and Fig.6) or hinged.

DESCRIPTION

The delivery includes a moulded polycarbonate chassis body, 4 moulded polycarbonate strips, 8 self-tapping screws and 20 standard 0.25 inch Fastons. Strips and screws are for clamping the circuit blocks into the holes in the chassis. The Fastons are for connections to the circuitry in the chassis.

To accommodate a size B block, it is necessary to remove the material between two size A holes, see Fig.1.
Interconnections between the terminal pins of the circuit blocks can be made by means of hand soldering or mini wire-wrapping; it is also feasible to use printed-wiring board PWB63 (catal. No. 4322 026 73750) in the chassis (see Fig.3).



Colour: grey

Dimensions in mm

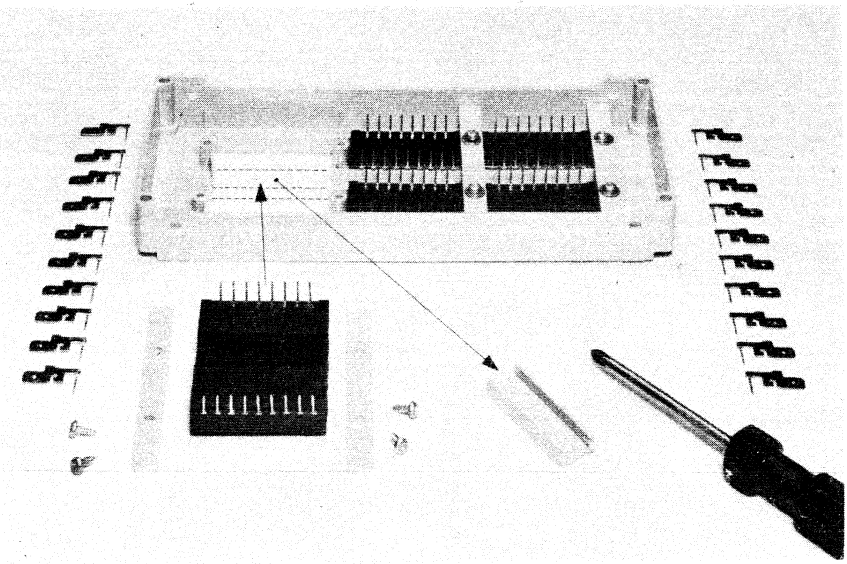
Weight: 150 g approx.

ASSEMBLY AND USE

The Fastons are brought in from the outside of a chassis and then fixed by bending the slotted part on the inside over about 15°

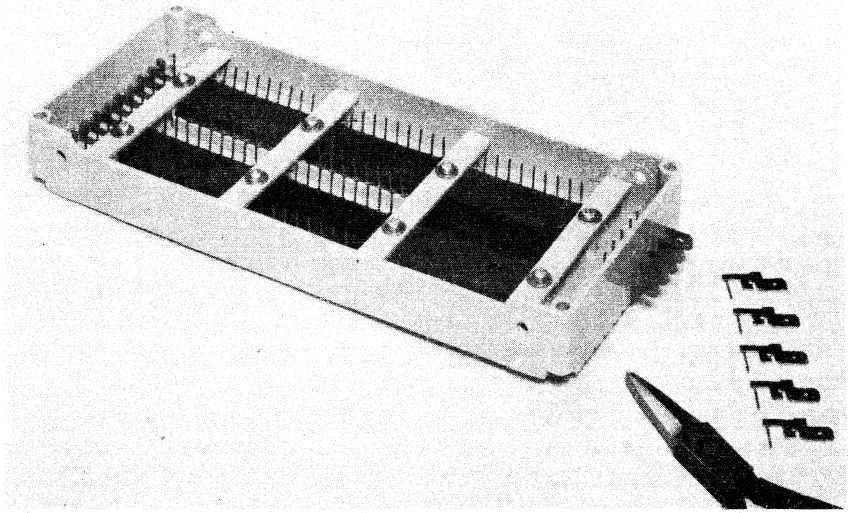
The blocks are clamped into the chassis with the strips and the self-tapping screws.

For fixing two or more chassis together, 4 mm bolts and nuts may be used.



RZ 26441-6

Fig.1



RZ 26441-5

Fig.2

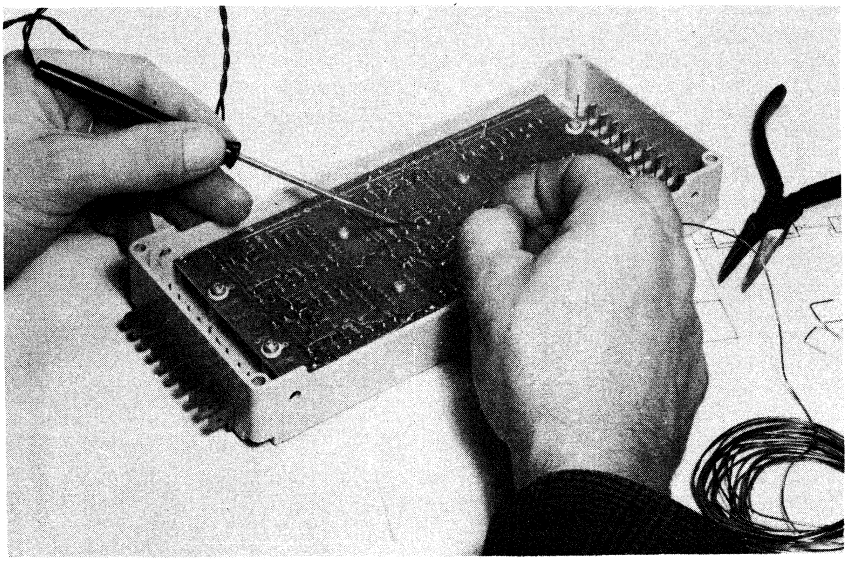


Fig.3 *RZ 26441-8*

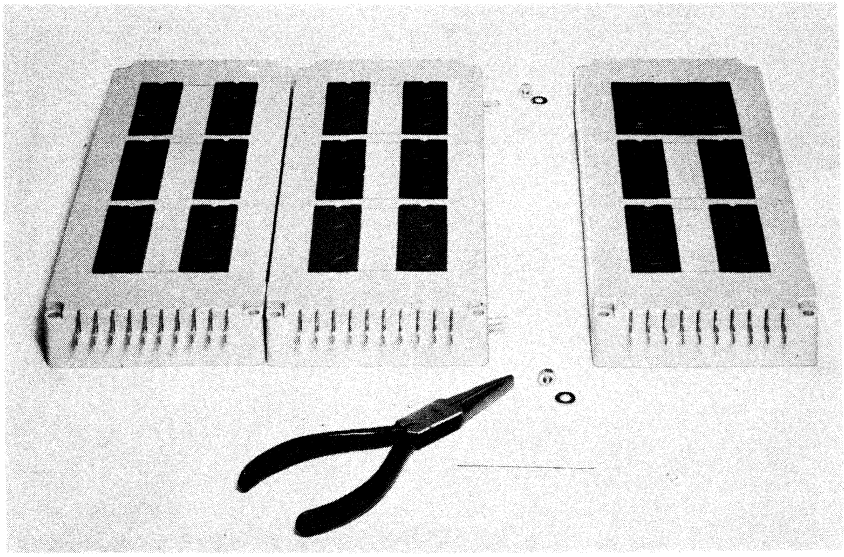


Fig.4 *RZ 26441-4*

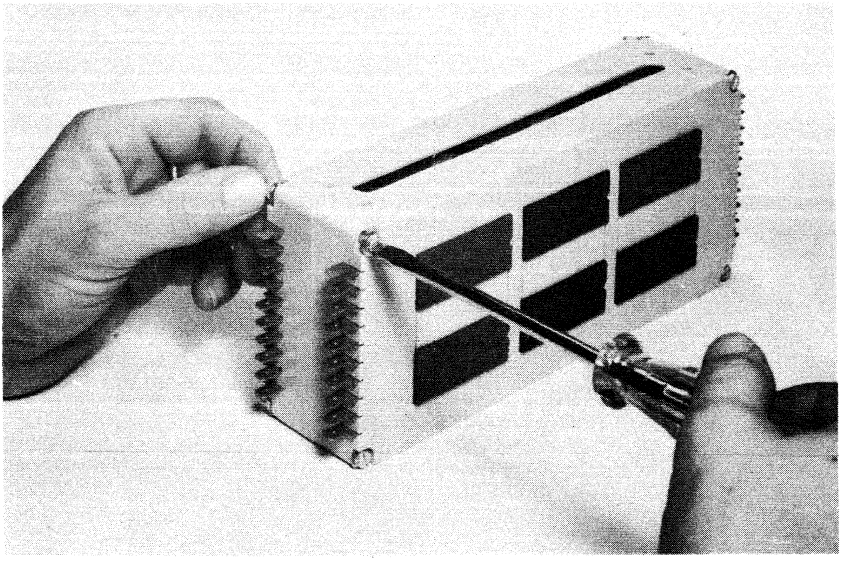


Fig.5 RZ 26441-9

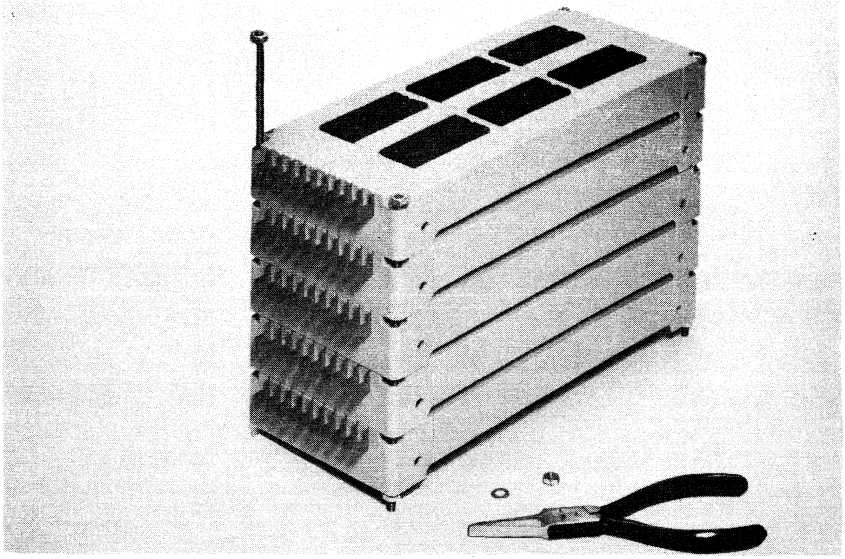
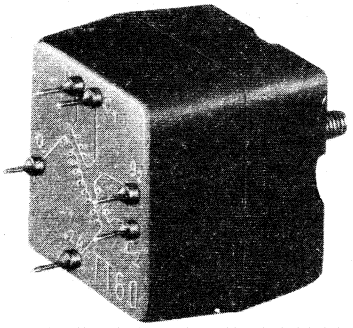


Fig.6 RZ 26441-10

THYRISTOR TRIGGER TRANSFORMER



A 51993

APPLICATION

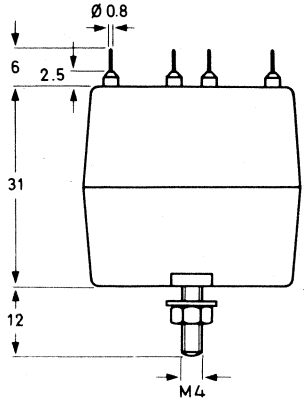
The TT60 can produce, in conjunction with the power amplifier UPA61, two pulse currents of up to 400 mA. This is sufficient gate current to trigger a pair of practically any type of thyristor.

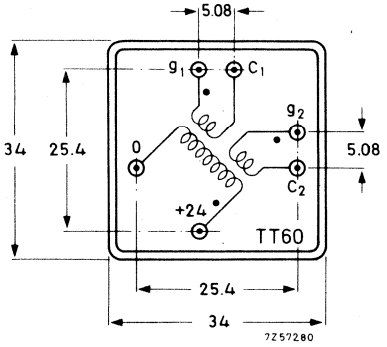
DESCRIPTION

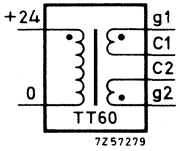
The transformer has been encapsulated in a mould.
A threaded stud permits the unit to be fixed to a support (This may be the thyristor heat sink, to obtain short gate and cathode leads).

For the hand soldering of wires to the pins 7 wire spirals, catal.No. 4022 220 64781, are packed with the transformer.

Dimensions in mm







Drawing symbol

Weight: 80 g approx.

TECHNICAL PERFORMANCE

Turns ratio primary : sec_1 : sec_2	3 : 1 : 1
Inductance of primary winding	≥ 6 mH
Leakage inductance referred to primary (both secondaries short-circuited)	≤ 18 μH
Primary winding resistance at T_{amb} = 25 °C	≤ 0.5 Ω
Secondary winding resistance at T_{amb} = 25 °C	≤ 0.1 Ω
Test voltage between the windings for 1 minute	5 kV

Output pulse in response to step input, circuit of Fig.A, R_{eq} = 13 Ω:	
rise time	≤ 0,75 μs
pulse duration	≥ 20 μs
Primary current (r.m.s.)	max. 600 mA
Primary switched current, duty cycle 1:4	max. 1800 mA
ET product primary	900 μVs
Operating ambient temperature	-10 to +85 °C
Storage temperature	-40 to +85 °C

APPLICATION INFORMATION

Pulse amplifier circuit

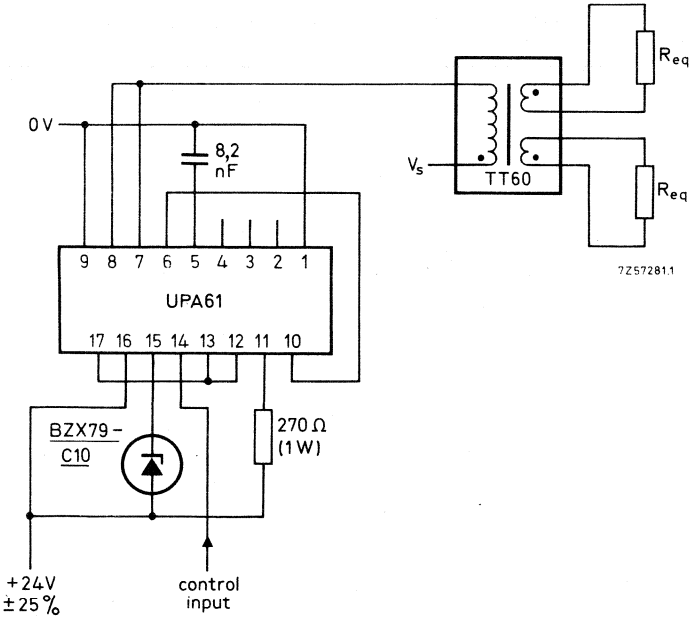


Fig. A

Power oscillator circuit

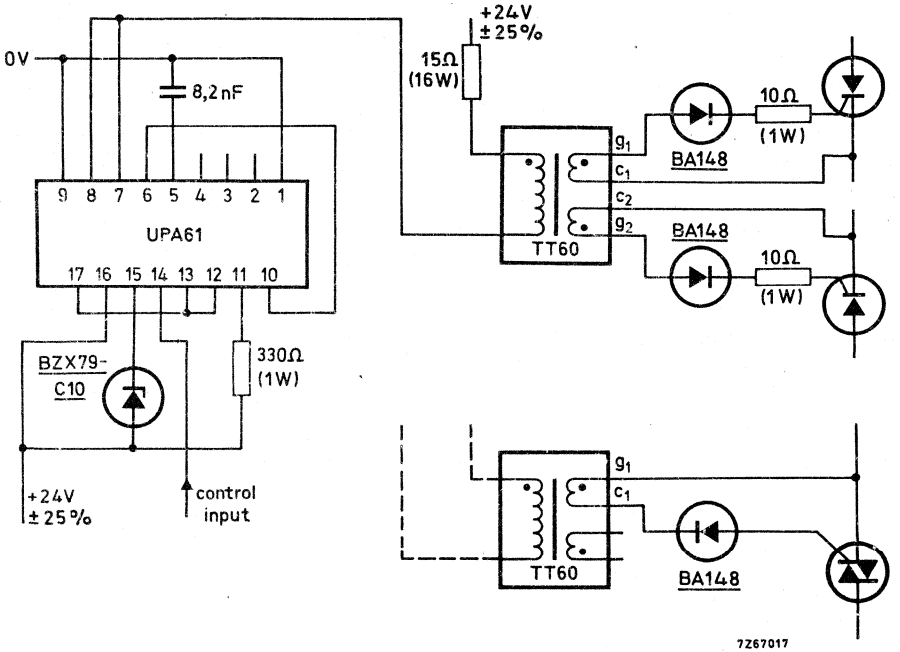


Fig. 8 shows the UPA61 as a 10 kHz power oscillator to trigger via TT60 a pair of thyristors or a triac.
Oscillation commences with a "high" (+ 12 V) on the control input (terminal 14 of the UPA61) ceasing when it becomes "low" (0 V).

DIRECT CURRENT TRANSFORMER

QUICK REFERENCE DATA	
Input current range	0 to 160 A
Output voltage range	0 to 15 V
Isolation voltage	5 kV
Sample frequency	5 kHz
Linearity	2%

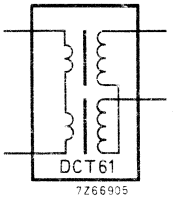
APPLICATION

When used in conjunction with the 60-series Norbit block UPA61 or GLD60 the DCT61 provides the linear conversion of a high d.c. current (up to 160A) to a low d.c. voltage (0 to 15 V) and also provides d.c. isolation between input and output.
The DCT61 is designed for use in d.c. power control circuits where it is necessary to supply information on the mains-connected d.c. load to the control circuit (low level) without forming a d.c. connection between the two parts. The ability to sample at high frequencies enables the DCT61 to produce the necessary supply information within one mains cycle (50/60 Hz).

DESCRIPTION

The DCT61 consists of two high-grade Ferroxcube toroids. Each toroid carries a secondary winding of 150 turns : these are connected in anti-series. The cores are encapsulated in a moulded body which is provided with two mounting holes. Connection to the secondary winding are made with 0,25 in Fastons.

The primary of the transformer is formed by passing the wire carrying the current to be measured through the aperture in the DCT61: the magnitude of this current will determine the number of primary turns required.



Symbol of the DCT61 with a primary winding.

MECHANICAL DATA

Dimensions (mm)

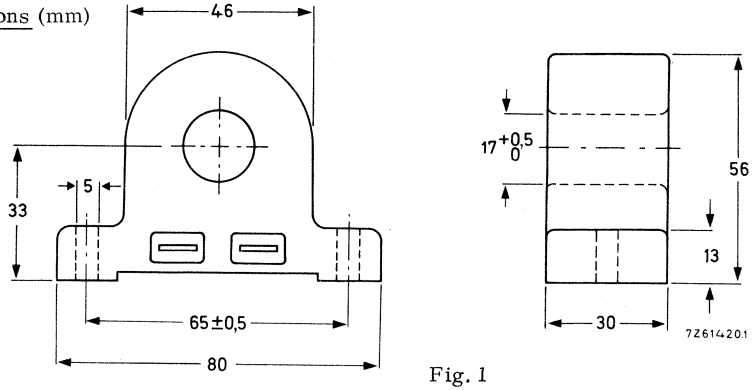


Fig. 1

Weight 155 g approximately

ELECTRICAL DATA

Ambient temperature range

Operating	−10 to + 70 °C
Storage	−40 to + 85 °C

	in conjunction with UPA61 (see Fig. 2a)	GLD60 (see Fig. 3a)
Primary input current	0 to 120 A	0 to 80 A
Primary input current with derated linearity (see Fig. 2b and 3b)	0 to 160 A	0 to 100 A
Test voltage	5 kV	
Sampling frequency	5 kHz	
Input/output linearity	2%	
Response time: trailing edge	1,4 ms	
leading edge	0,5 ms	
Output voltage (V_o)	0 to −12V	0 to +12 V
Output voltage variation due to supply voltage variation	0,4 %/%	
Output impedance	1 kΩ	
Load capability	10 kΩ	
Output ripple voltage, 5 kHz, on V_o (can be improved by adding extra filter network)	10%	

APPLICATION INFORMATION

Circuit of the d.c. current transformer with an supply voltage of −24 V

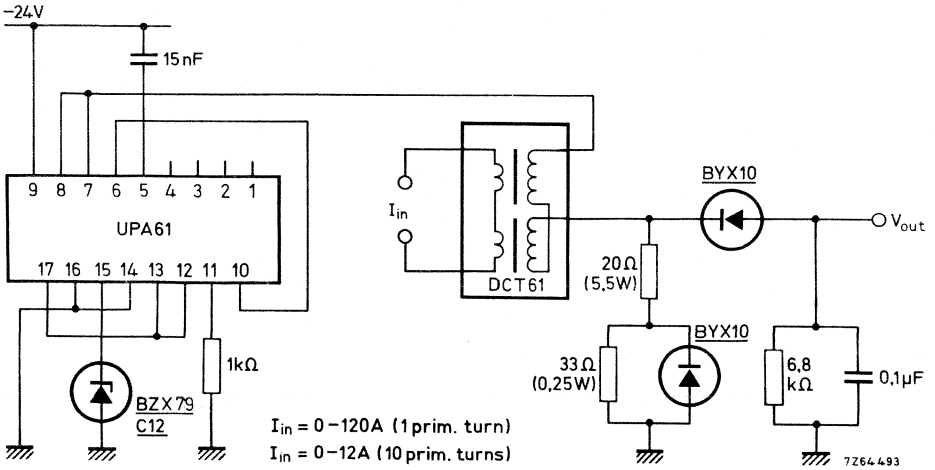


Fig. 2a Circuit of the DCT61 in conjunction with the UPA61.

Fig. 2b Variation of d.c. output voltage with d.c. input current.

Circuit of d.c. current transformer with an supply voltage of +24 V

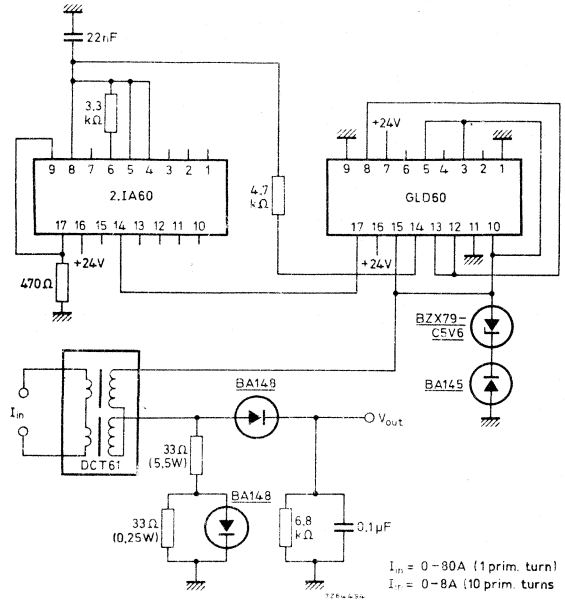


Fig. 3a Circuit of the DCT61 in conjunction with the GLD60.

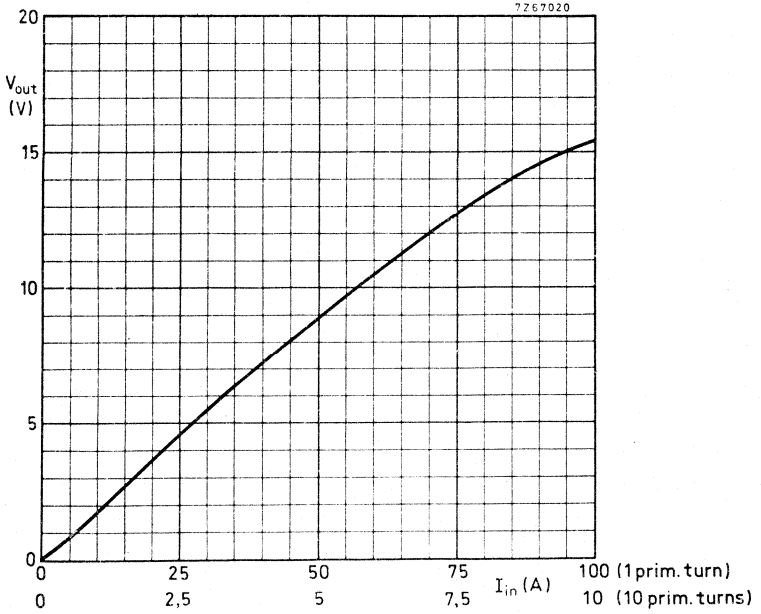
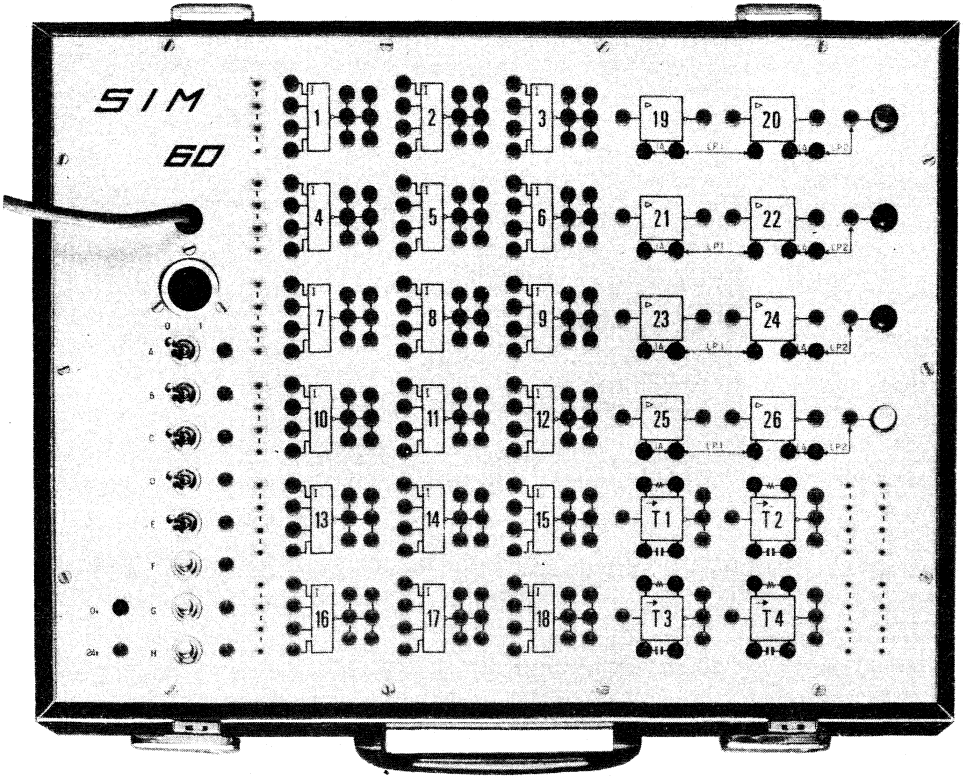


Fig. 3b Variation of d.c. output voltage with d.c. input current.

LOGIC SIMULATOR
for 60-Series NORbits

Purpose	logic system design simulation (breadboarding) and instruction
Supply voltage	117/220/240 V, 50 or 60 Hz
Housing	attaché case 415 x 310 x 95 mm
Weight	5, 5 kg

730806 - 19 - 01



DESCRIPTION

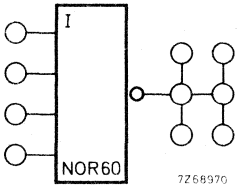
The SIM60 is a self-contained portable logic simulator, housed in a small light-weight attaché case, containing the following parts:

9 x	2. NOR60	5 x	toggle switch
4 x	2. IA60	3 x	push button
4 x	TU60	302 x	socket
1 x	power supply	10 x	patchcord, length 50 cm
4 x	indicator lamp	20 x	patchcord, length 30 cm
		10 x	patchcord, length 20 cm

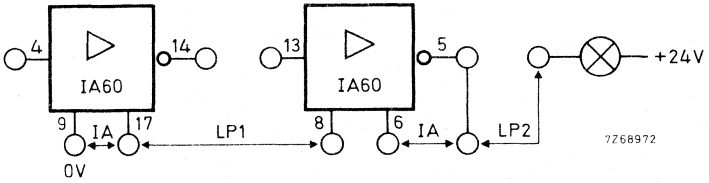
The circuit blocks are symbolized by rectangles and squares with adjoining input, output and auxiliary terminal sockets for patchcords. The fan-out of each block corresponds to the number of output sockets provided. Six groups of four auxiliary sockets (yellow) at the left and four groups at the right of the panel provide for concurrent application of signals to various control inputs.

Part description

2. NOR60 (see also relevant data sheet)
Units 1 to 18
18 NOR functions, each with 4 identical inputs and 6 paralleled output sockets.

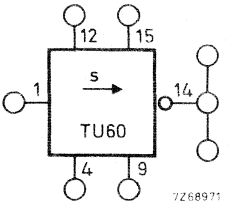


2. IA60 (see also relevant data sheet)
Units 19 to 26
8 inverting amplifiers:
Each 2. IA60 can be connected as an LPA60 to drive a load of 3 W at 24 V.



- To use the 2.IA60 as two inverting amplifiers, make the connections indicated by the arrows IA.
- To use the 2.IA60 as a single LPA60, make the connections indicated by the arrows LP1 and LP2.

TU 60 (see also relevant data sheet)
Units T1 to T4
Timer unit with 1 input and 3 paralleled output sockets. The time constant is determined by the resistance and capacitance connected externally between terminals 12-15 and 4-9, respectively.



Power supply (0 V, 24 V)

Suitable for operation from 117 V, 220 V or 240 V, 50 or 60 Hz, mains. Includes input cable and plug. Provides system 0 V and 24 V d.c. supply rails.

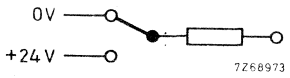
Indicator lamps

1 red
1 yellow
1 white
1 green

can be used as output indicators for LPA60, one side connected to +24 V

Toggle switches (A to E) and push buttons (F to H)

To simulate 1 or 0 input conditions and temporary 1 input signals, respectively.



output via internal current limiting resistance of 12 kΩ

Sockets

Colour indicates function:
Green = inputs
Red = outputs and 24 V
Black = other unit terminals and 0 V
Yellow = auxiliary sockets to multiply various signals

Note: The terminal socket marked '24 V' on the panel is connected directly to the +24 V supply rail, without current limiting resistor.

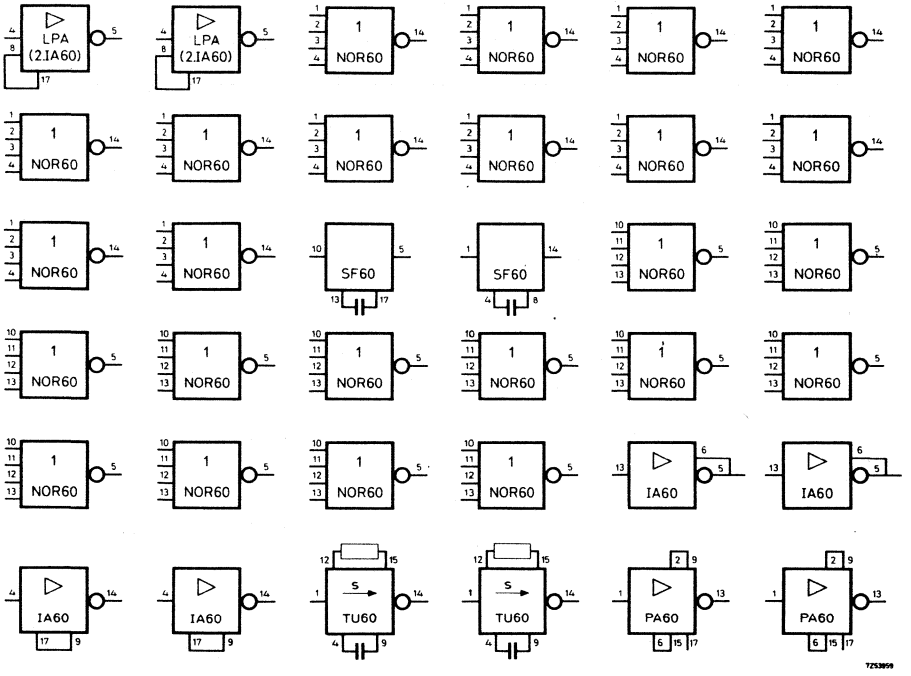
Application

Circuits for training purposes are given in Application Book "Control System Design Manual for 60-Series NORbits" under various headings.

CAUTION: Before plugging the SIM60 into the mains, be sure that the mains voltage selector on the panel is turned to the appropriate voltage.

STICKERS FOR THE 60-SERIES NORBITS

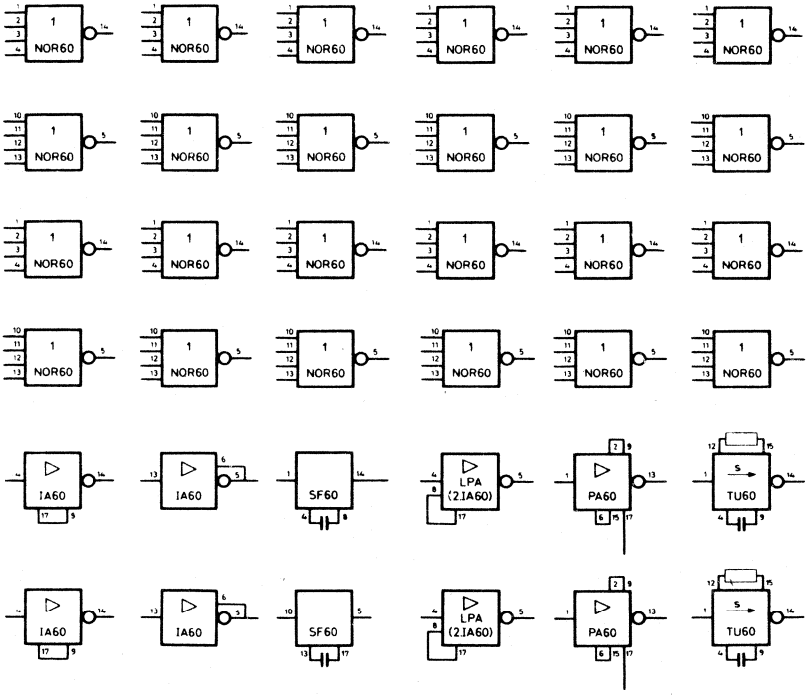
These are drawing symbols of NORBITS printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings.
The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number of 50 sheets: 4322 026 36481.



Sticker sheet without 4. NOR60 or TT60

STICKERS FOR THE 60-SERIES NORBITS

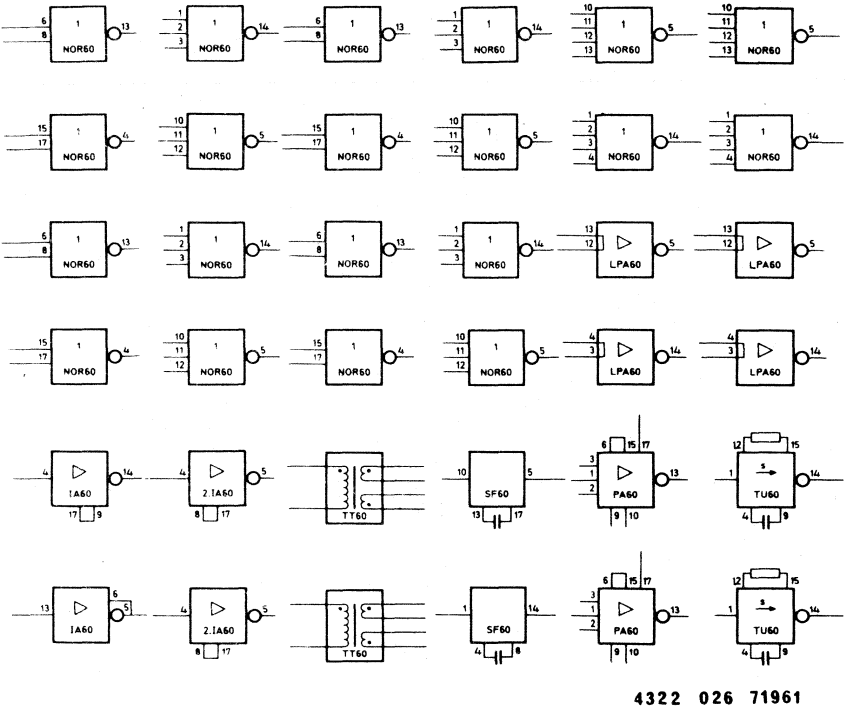
These are drawing symbols of NORBITS printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings.
The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71941.



Sticker sheet without 4. NOR60 or TT60

STICKERS FOR THE 60-SERIES NORBITS

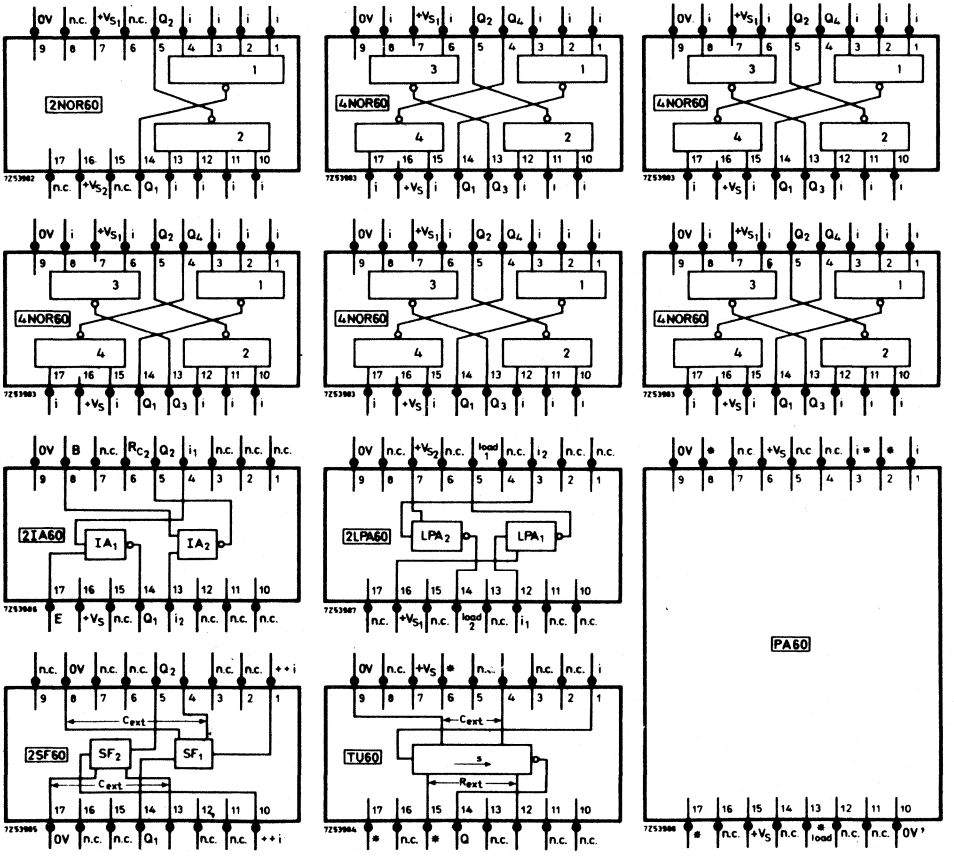
These are drawing symbols of NORBITS printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings.
The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71961.



Sticker sheet with 4. NOR60 and TT60

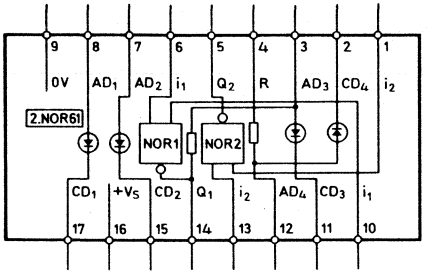
WIRING LAYOUT STICKERS
for the 60-series NORBITS

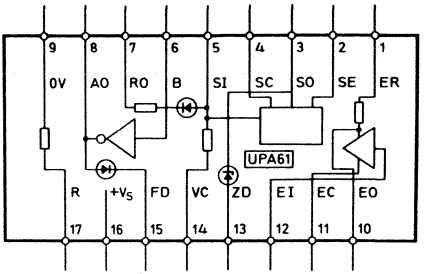
These are drawing symbols of 60-series blocks printed on self-adhesive, transparent material. They can be used for fast preparation of wiring layouts. All pin distances are actual size.
The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71971.

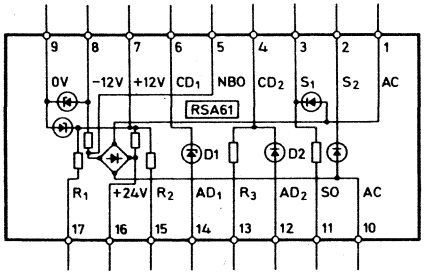


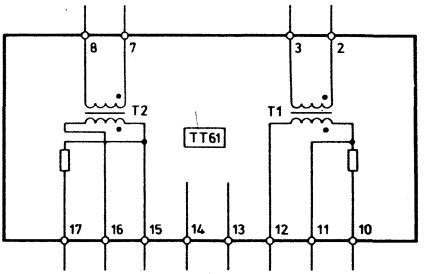
WIRING LAYOUT STICKERS
for the 61-Series NORBITS

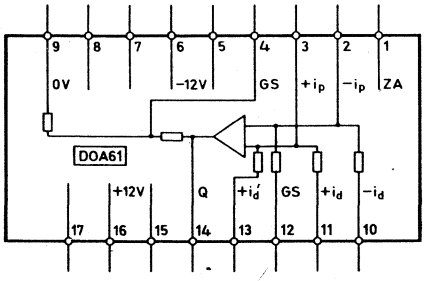
These are drawing symbols of 61-series blocks printed on self-adhesive,transparent material. They can be used for fast preparation of wiring layouts. All pin distances are actual size.
The stickers are available in sheets, each containing the five drawings shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71981.











Circuit blocks 90-Series

INTRODUCTION

The "90-Series" comprises a number of circuit blocks eminently suitable for use in industrial control systems.

As far as the environmental specification, the supply voltage and the encapsulation are concerned, the circuit blocks in this series are compatible with those of the 60-Series and they can therefore be successfully combined.

Operating on the principle of trigger logic (that is: the units are driven by voltage transients in contrast with those of the 60-Series which respond to voltage level), the 90-Series units allow the building of assemblies such as counters and shift registers simply and economically. They are so designed as to have a high noise immunity. However, care must be taken to avoid capacitive and inductive cross-talk between connecting wires.

Briefly, the features of the 90-Series are:

- Single rail 24 V $\pm$ 25 % supply, allowing the use of an inexpensive power supply, which helps to keep the cost down, particularly in small systems.
- Transfer moulded cases, giving optimum protection.
- Rigid terminals spaced at 0.2 in pitch, permitting a variety of interconnection methods to be used (dip soldering, hand soldering, mini wire-wrapping).
- Good noise immunity.
- Silicon semiconductors throughout, ensuring reliable operation down to $-10\ ^{o}C$ and up to $+70\ ^{o}C$.
- Usable with the large number of accessories of the 60-Series.
- Easy-to-use loading table for system design.

The 90-Series comprises the following types:

FF90	Flip-flop
2.TG90	Twin-trigger gate
PS90	Pulse shaper

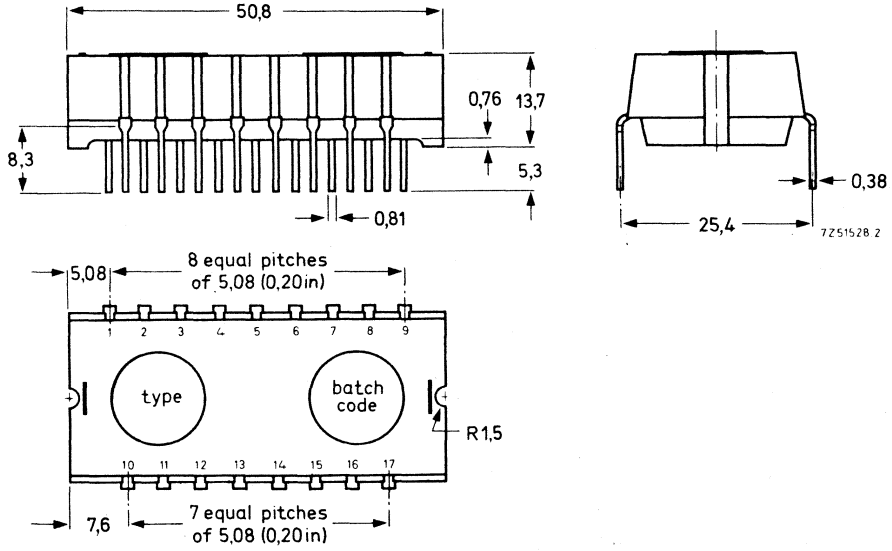
CONSTRUCTION

The circuit elements are housed in a transfer moulded encapsulation, which is identical to the "size A" block of the 60-series. The dimensions are as shown below. The pin connections for each unit are shown on the relevant data sheets. Pin numbering is moulded on both top and bottom of the unit. All pins are also accessible from the top of the unit to facilitate test requirements.

Mounting

The units may be mounted on printed-wiring boards, and a range of these is available with suitable metal housing chassis. They may also be clamped in the moulded Universal Mounting Chassis UMC 60 or fixed with 3 mm screws.

Dimensions in mm (inch equivalents within brackets)



TEST SPECIFICATIONS

All units meet the following test specifications:

Test	IEC 68	MIL-STD-202C
Dry heat life test	56 days at max. diss. max. temp. check at: 0-10/14d-56d.	Meth. 108A, Cond. D; check at 0-10/ 14d-56d.
Long-term damp heat non operating	Test C, 56 days check at 0-10/14 d-56d.	Meth. 103B, Cond. D; check at 0-10/ 14d-56d.
Long-term damp heat operating	Test C, 56d. min., diss., check at 0-10/14d-56d.	ditto
Temp. cycle-test	Test Na, 30 min., 2-3 min. in between; preferred: −40 °C; +85 °C and +125 °C.	Meth. 107B, Cond. A: moderate temp.
Vibration	Test Fb; 10-500-10 Hz 1 octave/min.; ampl. 0.75 mm max.; 10 g max. 3 x 3 hrs.	Meth. 204A, Cond. A: 10-500-10 Hz: 15 min. ampl. 0.75 max; 10 g max., 3 x 3 hrs.
Shock	-	Meth. 202B, 3 blows 50 g.
Robustness of terminations	Test $U_A + U_B$	Meth. 211A + (B or C)
Solderability + solder heat	Test T; at 0 hr and at 56d; no electr. test	Meth. 210, at 0 hr and at 56d; no electr. test

CHARACTERISTICS AND DEFINITIONS

AMBIENT TEMPERATURE LIMITS

Storage	T_{amb} = -40 °C to +85 °C
Operating	T_{amb} = -10 °C to +70 °C

SUPPLY VOLTAGE (V_S)

Single rail, +24 $V_{d.c.}$ ± 25% (18 to 30 V)

OUTPUT LEVEL

Logic '0'	0 to +0.3 V
Logic '1'	+12 to +30 V

TRIGGERING EDGE

The unit FF90 is driven by a negative-going transient (from "1" to "0" level). The maximum duration of the transient is, unless specified otherwise, 3 μs.

DRIVE UNIT (D.U.)

Drive required on Reset input of FF90 to bring output Q_1 to '1' level. [1])

ZERO UNIT (Z.U.)

Half the drive at '0' level required on one T terminal to trigger an FF90 unit.

FAN OUT

Number of drive units and zero units that can be delivered by a logic function, without exceeding the above defined limits for the logic levels.

---

[1]) This drive unit has also been specified as the drive required on one input of a NOR60 (with all other inputs returned to 0-volt line) to bring the output at '0' level.

INPUT AND OUTPUT DATA

System design is greatly simplified by expression of the input requirements and fan out capabilities of the various units in integral multiples of drive units (D.U.) and zero units (Z.U.). To check that the loadability of a particular unit is not exceeded simply add the number of D.U.'s or Z.U.'s present at its output.

FAN-OUT TABLE

The table shows the number D.U.'s and Z.U.'s, which can be delivered by the different units of the 90- and 60-series. The fan-outs are valid for a positive supply voltage of 24 V $\pm$ 25%.

unit	output capability		notes and instructions
	'1' level (D.U.)	'0' level (Z.U.)	
NOR of 2. NOR 60	6	12	2 inputs of the NOR must be connected in parallel. Signal must be derived from a chain of units that includes either a PS 90, an FF 90 or a TU 60.
2. IA 60; I.A. driven by an I.A.	20	50	Both the inverting and non-inverting connections can be used, but pins 5 and 6 must be interconnected. Signal must be derived from a chain of units that includes either a PS 90, an FF 90 or a TU 60.
NOR of 4. NOR 60	6	0	
LPA 60	-	0	No Z.U. available. Therefore, these units must not be used to drive an FF 90 or 2.TG90 directly.
PA 60	-	0	
TU 60	5	0	
SF 60	2	0	
PS 90	6	80	
FF 90	5	7	

FLIP-FLOP

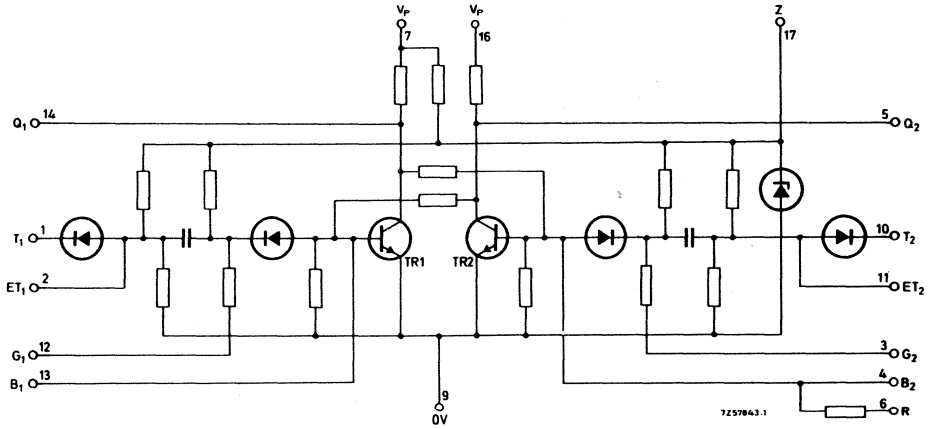
QUICK REFERENCE DATA	
Function	set-reset bistable multivibrator with trigger gates
Encapsulation	size: A block; colour: red
Max. counting speed (worst case)	5 kHz
Output capability	5 D.U., 7 Z.U.
Trigger input requirement	"1"-"0" edge of max. 3 μs; 2 Z.U.

APPLICATION

The FF90 has been intended to be used in counters, shift registers, etc.

DESCRIPTION

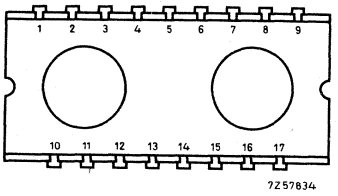
Circuit



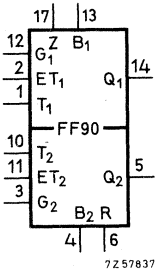
The unit comprises a set-reset bistable multivibrator which incorporates trigger gates. Switching is performed by applying a "1"-"0" edge of max. 3 μs at the trigger terminals (T_1 and T_2) which are controlled by gates (G_1 and G_2). The trigger inputs may be extended by the addition of external diodes to the extension terminals (ET_1 and ET_2) to provide an OR or inhibit facility. In addition, the circuit may be reset by applying a "1" level to the reset terminal (R) and may be set by applying a "1" level to the base of transistor 1 (B_1) via a resistor.

Green Binder, Tab 1

Terminal location



Drawing symbol



1 = T_1 = Trigger input 1
2 = ET_1 = Extension trigger input 1
3 = G_2 = Gate input 2
4 = B_2 = Transistor TR_2 base
5 = Q_2 = Output 2
6 = R = Reset
7 = V_p = For positive supply (connect to pin 16)
8 = Not connected
9 = 0 V = 0 V common
10 = T_2 = Trigger input 2
11 = ET_2 = Extension trigger input 2
12 = G_1 = Gate input 1
13 = B_1 = Transistor TR_1 base
14 = Q_1 = Output 1
15 = Not connected
16 = V_p = For positive supply (connect to pin 7)
17 = Z = Zener diode*

* Caution: With the supplies connected ensure that pin 16 is not accidentally connected to pin 17, otherwise the zener diode will be damaged.

ELECTRICAL DATA

Power supply

Voltage	+24 V ± 25%
Current	< 21 mA

Input requirements (see also "Switching times")

function	input terminal	input requirement		notes and instructions
		'1' level (D.U.)	'0' level (Z.U.)	
reset (put Q1 to '1')	R	1	0	The Set and Reset inputs may be expanded by using up to 3 suitable diodes at each input. Ensure that the cathode of each diode is connected to the input. If the Set or Reset facilities are used, inputs must be held at '0' (and not left open-circuited) except during the command period.
set (put Q2 to '1')	B1 via 82 kΩ resistor 2)	1	0	
gate	G_1, G_2	2	1	'1' or open-circuit closes gate. '0' opens gate.
gate	G_1, G_2 via a diode 1) 2)	0	1	'1' or open-circuit closes gate. '0' opens gate. Ensure that the anode of the diode is connected to the input.
trigger	T_1, T_2	0	2	Only a '1'-'0' edge occurring within 3 μs triggers the flip-flop. If T_1 and T_2 are interconnected, 4 Z.U. are required.
trigger	ET_1, ET_2 via a diode 1) 2)	0	2	Only a '1'-'0' edge occurring within 3 μs triggers the flip-flop. If ET_1 and ET_2 are interconnected, 4 Z.U. are required. Ensure that the anode of each diode is connected to the input.

1) Diodes type BAX 13, BAX 16 or BAX 78 can be used.

2) If external components are used, ensure that they are mounted as close as possible to the appropriate input.

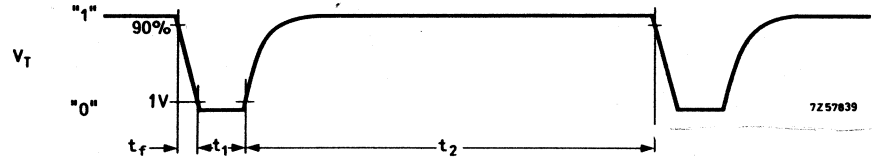
Output data

Output capability	5 D.U. and 7 Z.U.
Max. capacitive load	200 pF

Account must be taken of the load imposed by the gates when they are connected to the output terminals (Q_1, Q_2).

Switching times

Trigger



Max. fall time	t_{fmax}		3 μs
Min. pulse duration	t_{1min}		5 μs
Trigger recovery time	t_2	max.	99 μs
		typ.	73 μs

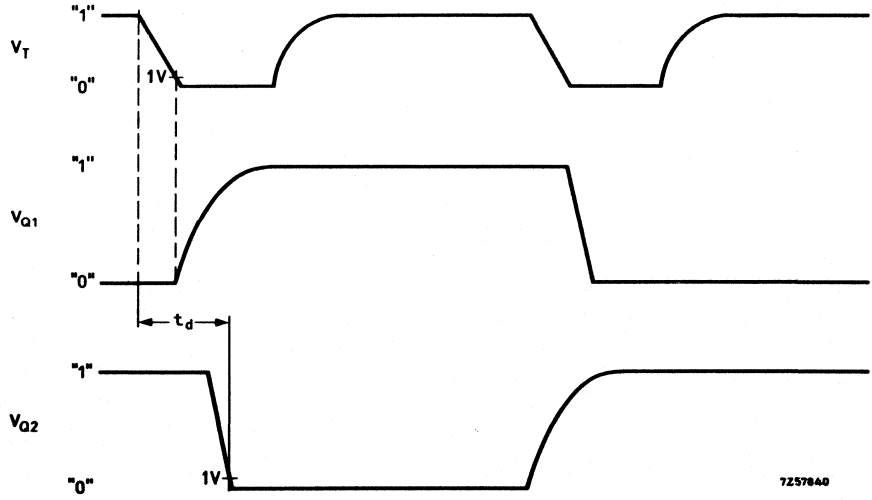
Gate

Gate recovery time	max.	137 μs
	typ.	100 μs

The signal at the gate must be present at least 137 μs (worst case) before the triggering edge is applied to T_1 or T_2. It is permitted to change the gate signal simultaneously with the triggering edge.

Switching delay

Delay between triggering edge and negative-going output.	t_d	max.	8 μs
		typ.	3 μs



Reset of Set: The appropriate terminal should be at a logical '1' for a minimum of 50 μs to reset or set the flip-flop.

Maximum Counting Speed (1 : 1 mark: space ratio) 5 kHz (worst case)

The worst case figure is related to the most disadvantageous connection or input condition that can be made.

APPLICATION INFORMATION

For connection as a divider of two connect pin 3 to pin 5 and pin 12 to pin 14.

More information is given in "Application Information 849, Counting and Shifting with 90-Series Modules."

TWIN-TRIGGER GATE

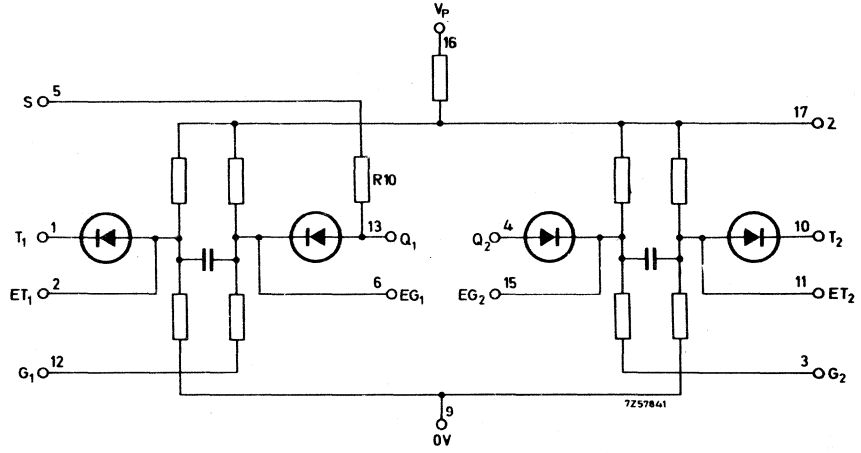
QUICK REFERENCE DATA	
Function	two trigger gates for use with FF90 only
Encapsulation	size: A block; colour: red
Output signal	suitable for triggering direct on transistor base of FF90 (B_1 and B_2)
Trigger input requirement	'1'-'0' edge of max. 3 μs; 2 Z.U.

APPLICATION

The 2.TG90 has been intended to provide two extra independent trigger gates for the FF90.

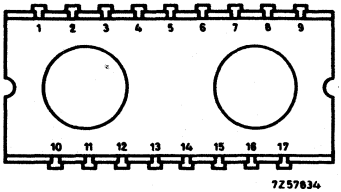
DESCRIPTION

Circuit

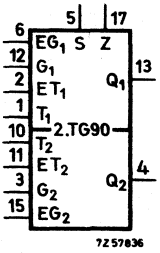


The unit comprises two gating circuits to perform extra independent trigger functions. The mode of operation is the same as for the trigger functions of the FF90. Switching is performed by applying a '1'-'0' edge of max. 3 μs at the trigger terminals (T1 and T2) which are controlled by gates (G_1 and G_2). The trigger inputs may be expanded by the addition of external diodes to the extension terminals (ET_1 and ET_2) to provide an OR or inhibit facility. The extra resistor (R_{10}), connected to terminal Q_1, provides the 'set' facility for the FF90.

Terminal location



Drawing symbol



1 = T_1 = Trigger input
2 = ET_1 = Extension trigger input 1
3 = G_2 = Gate input 2
4 = Q_2 = Output to B_2 (pin 4) of FF90
5 = S = Set terminal
6 = EG_1 = Extension gate input
8 = Not connected
9 = Not connected
9 = 0 V = 0 V common

10 = T_2 = Trigger input 2
11 = ET_2 = Extension trigger input 2
12 = G_1 = Gate input 1
13 = Q_1 = Output to B_1 (pin 13) of FF90
14 = Not connected
15 = EG_2 = Extension gate input
16 = V_P = For positive supply
17 = Z = Voltage reference terminal, connect to Z (pin 17) on FF90

ELECTRICAL DATA

Power supply

Voltage	+24 V ± 25%
Current	7.5 mA

Input requirements

function	input terminal	input requirement		notes and instructions
		'1' level (D.U.)	'0' level (Z.U.)	
set (put Q_2 of associated FF90 to '1')	S	1	0	The Set input may be expanded by using up to 3 suitable diodes on each input. Ensure that the cathode of each diode is connected to the input. If the Set facility is used, the input must be held at '0' (and not left open-circuited), except during the input period.
gate	G_1, G_2	2	1	'1' or open-circuit closes gate. '0' opens gate
gate	G_1, G_2 via diode 1) 2)	0	1	'1' or open-circuit closes gate. '0' opens gate. Ensure that the anode of the diode is connected to the input.
trigger	T_1, T_2	0	2	Only a '1'-'0' edge occurring within 3 μs triggers the flip-flop 3). If T_1 and T_2 are interconnected, 4 Z.U. are required.
trigger	ET_1, ET_2 via diode 1) 2)	0	2	Only a '1'-'0' edge occurring within 3 μs triggers the flip-flop 3). If ET_1 and ET_2 are interconnected, 4 Z.U. are required. A maximum of two diodes may be connected to each ET terminal. Ensure that the anode of each diode is connected to the input.

For notes see page 4.

Output data

The outputs Q_1, Q_2 are suitable only for use with one FF90; Q_1, Q_2 and Z of the 2.TG90 should be connected to B_1, B_2 and Z respectively of the FF90.
The inter-wiring capacitance should be limited at 50 pF (maximum). This capacitance will not be exceeded when a 2.TG90 is mounted next to an FF90.

1) Diodes type BAX 13, BAX 16 or BAX 78 can be used. Max. 2 diodes may be added.
2) If external components are used, ensure that they are mounted as close as possible to the appropriate input.
3) Switching times of the triggering signal are the same as for the FF90.

PULSE SHAPER

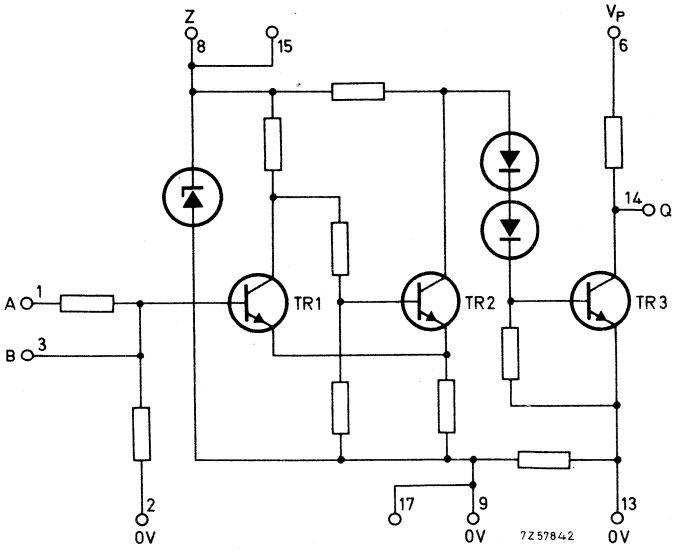
QUICK REFERENCE DATA	
Function	a. Driving the trigger inputs of one or more FF90 or 2.TG90 units b. Shaping signals to produce NORBIT 60 drive levels
Encapsulation	size: A block; colour: green
Output capability	6 D.U.; 40 Z.U.

APPLICATION

The PS90 has been intended to produce the triggering edge required for the FF90. The output levels are conforming to '1' and '0' of 60-Series logic.

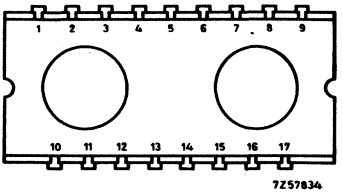
DESCRIPTION

Circuit

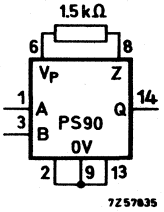


The unit contains a Schmitt trigger circuit followed by an inverting amplifier.

Terminal location



Drawing symbol



1 = A = Input via resistor
2 = 0 V = 0 V common (connect to pins 9 and 13)
3 = B = Input direct to base
4 = Not connected
5 = Not connected
6 = Vp = For positive supply (connect also to pin 8 via 1.5 kΩ resistor*)
7 = Not connected
8 = Z = Zener diode ** internally connected to pin 15 (connect to pin 6 via 1.5 kΩ resistor *)
9 = 0 V = 0 V common, internal connection to pin 17 (connect also to pins 2 and 13)
10 = Not connected
11 = Not connected
12 = Not connected
13 = 0 V = 0 V common (connect also to pins 2 and 9)
14 = Q = Output
15 = Z = Internally connected to pin 8
16 = Not connected
17 = 0 V = Internally connected to pin 9.

* The 1.5 kΩ ± 10% resistor connected between pins 6 and 8 (15) has a dissipation of 0.35 W maximum.

** When the PS90 is mounted on PWB60 or PWB61, pins 7 and 16 are connected to the positive supply Vp. Ensure therefore, that neither pins 7 and 8 nor pins 15 and 16 are interconnected. Otherwise, the Zener diode will be damaged.

ELECTRICAL DATA

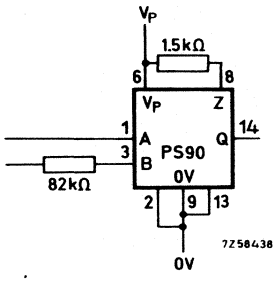
Power supply

Voltage	+24 V ± 25%
Current	< 21 mA

Input Data

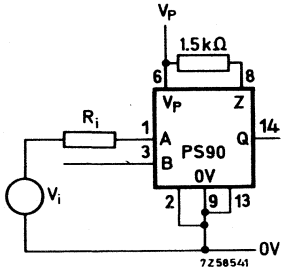
1. Unit driven by circuit block of 60 Series or 90 Series

The input requirement at pin 1 (pin 3 not connected) for '0' output is 1 D.U.
One input may be added, namely an 82 kΩ resistor connected to pin 3 (input requirement is 1 D.U.). The circuit then performs as a 2-input NOR function.
The 82 kΩ resistor should be mounted as close as possible to the unit.



2. Unit driven by any other circuit at pin 1 with pin 3 not connected.

	Operating	Limiting value
Input voltage to give '0' output	min. +6 V	+30 V
Input voltage to give '1' output	max. +1.5 V	−15 V



Hysteresis

ΔV_i min. = 0.55 + 0.003 Ri V (Ri in kΩ)
ΔV_i max. = 1.5 + 0.012 Ri V (Ri in kΩ)

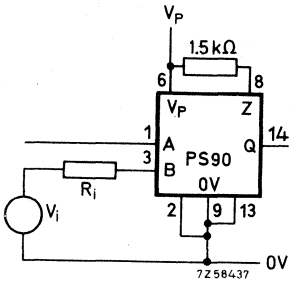
See also "Switching speed".

3. Unit driven by any other circuit at pin 3 with pin 1 not connected

	Operating	Limiting values
Input current to give '0' output	min. 50 μA	5 mA
Input current to give '1' output	max. 15 μA	0 mA

If driven by a voltage source, the source resistance should be minimum 500 Ω.

Max. positive voltage with R_i = 500 Ω +5 V
Max. positive voltage with R_i = 6,8 kΩ +30 V
With pin 2 not connected the max. source resistance is 50 kΩ and the max. negative voltage is 4 V.



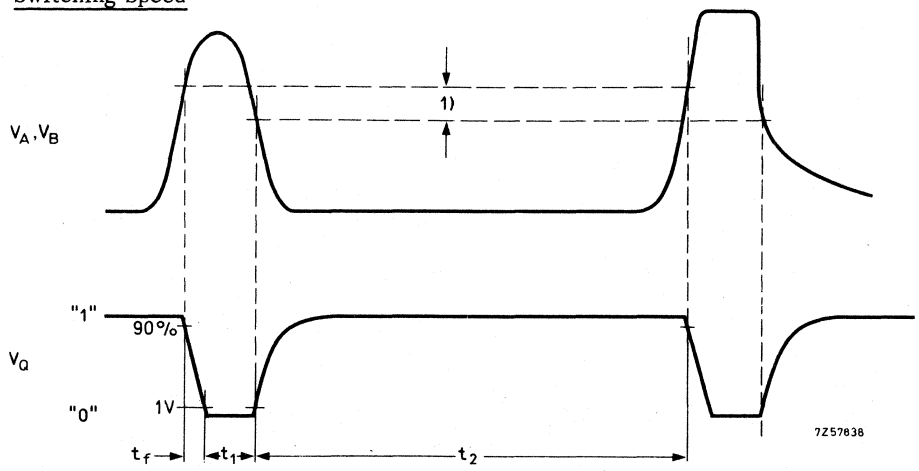
Hysteresis
ΔV_i min. = 0,32 + 0,003 R_i V (R_i in kΩ)
ΔV_i max. = 0,45 + 0,012 R_i V (R_i in kΩ)

See also "Switching speed".

Output Data

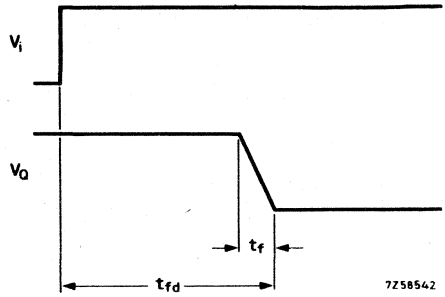
Output capability	6 D.U.
	40 Z.U.
Max. capacitive load	200 pF

Switching Speed



$t_f \leq 3\ \mu s$
t_1 and t_2 depend on input waveforms.
1) Hysteris ΔV_A or ΔV_B

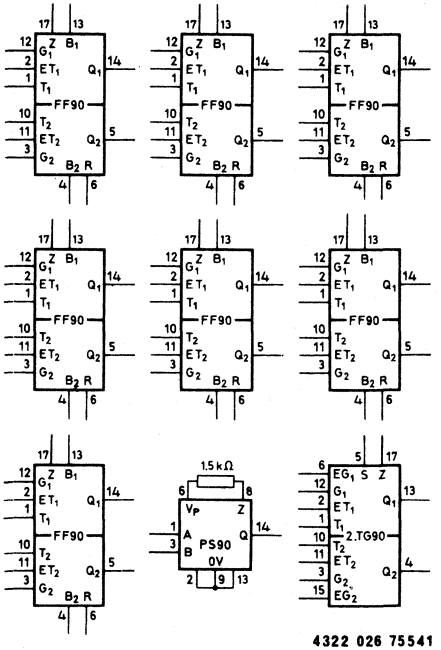
If a step function is applied to the input and the output is loaded with 200 pF the output signal is given by:



Fall time	$t_f < 0.25\ \mu s$
Fall delay time	$t_{fd} < 2.5\ \mu s$

STICKERS FOR THE 90-SERIES CIRCUIT BLOCKS

These are drawing symbols of CIRCUIT BLOCKS printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings.
The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 75541.



Input/output devices

INTRODUCTION

Input devices

Industrial control systems require compatible input devices that are capable of deriving signals representative of controlled or otherwise pertinent conditions. Though the information to be dealt with may take a variety of forms - e.g. presence, position, movement, rotation etc. - many different situations can be covered by a comparitively small selection of input devices.
The requirements of each situation determine the physical principle to be employed in the input device.
For reasons of speed and reliability it is preferable to avoid mechanical contact in deriving the input signal, and often an all-static method of derivation is required.
Experience with input devices has made it clear that skilful use of them can greatly improve machine output and reliability.

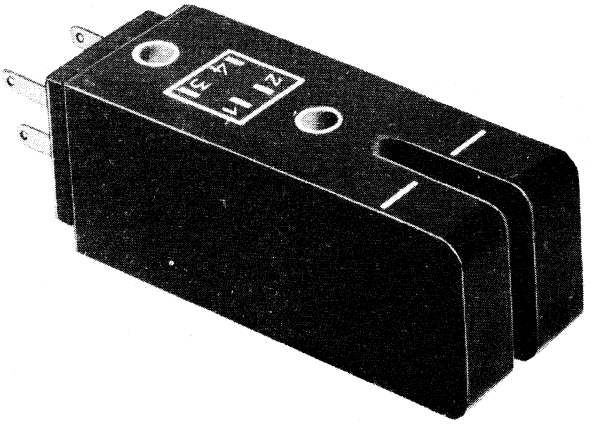
Output devices

Quite often the output of a logic system is required to control the mains power fed to a heavy load (e.g. motor, furnace, etc.). The average power supplied by the power stacks to the load can be controlled by varying the conduction angle of the thyristors.
An interface circuit is required between the logic system and the power stacks. Useful interface curcuits can be made with 61-Series circuit blocks and/or the TT60.

In this series the following units are available:

VANE SWITCHED OSCILLATOR

720809-21-01



Supply voltage	12 V_{dc}
Operating-temperature range	−25 to +85 °C

APPLICATION

The vane switched oscillator can be applied as a static switching device, the switching action being determined by the position of a vane. For the vane any metal can be used.

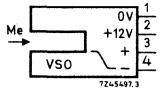
CONSTRUCTION

The vane switched oscillator consists of an oscillator and a diode rectifier. The latter is connected to a separate coupling winding of the oscillator coil, thus providing an isolated d.c. output.
The lay-out of the oscillator is such that upon inserting a suitable piece of metal (vane) in a gap between the oscillator coil windings, the oscillation stops and the d.c. output of the unit will drop to zero.
The complete circuit is encapsulated in epoxy resin.

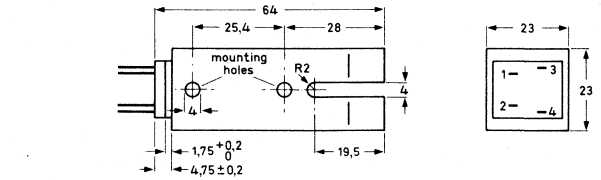
1 = −
2 = + } supply

3 = +
4 = − } output

Terminal location



Drawing symbol



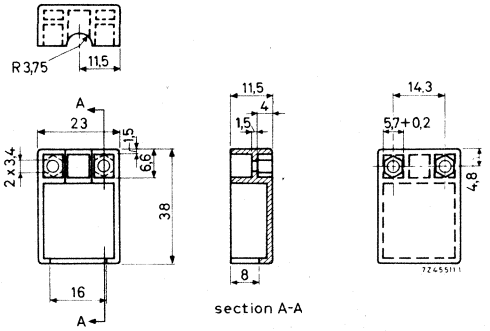
Dimensions (mm)

The weight (without cable anchoring cover) is 42 g.

The unit may be mounted in any position. Two mounting holes allow the use of 4 mm bolts. The bolts should be tightened with a torque of maximum 450 mNm provided that washers are used. Stacking of units is permitted. If two or more units are stacked (gaps in line), they must be placed back to back/front to front.

Connection can be made by 0,110 inch Fastons or by soldering.
A cable anchoring cover, consisting of two equal caps (as shown in the figure below), is supplied with each VSO.

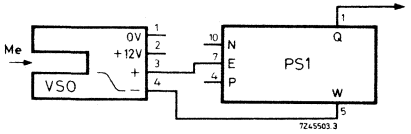
The lines on the arms of the VSO indicate the centre of the oscillator coil windings.

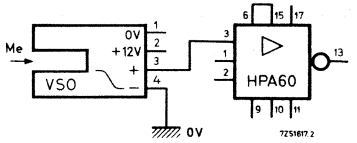


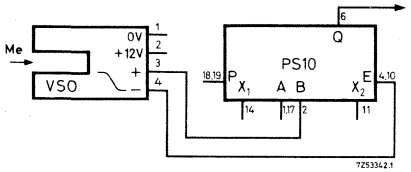
Cable anchoring cover

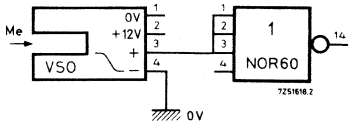
ELECTRICAL DATA

Supply voltage	12 V_{dc} ± 10% or +6 V_{dc} ± 10% and −6 V_{dc} ± 10% (with common 0 V)
Consumed current (in both oscillating and non-oscillating condition)	12 mA ± 10%
Output voltage	5,75 V ± 15% open circuit , isolated from the supply. Maximum permissible voltage between 1-2 and 3-4 is 100 V_p Suited for driving the pulse shaper types PS 1* and PS 10**, and for driving the Norbit HPA60 and 2.NOR60 if three inputs are connected in parallel.









Output impedance (without vane)	4,1 kΩ ± 10%
Maximum detection frequency	1 kHz
Noise (over supply lines)	< 100 mV_{p-p}
Ambient temperature range operating storage	 −25 to +85 °C −40 to +85 °C

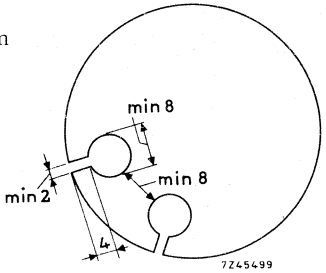
* circuit block 100 kHz series, catalog number 2722 001 11001
** circuit block 10-series , catalog number 2722 004 11001

APPLICATION INFORMATION (typical values)

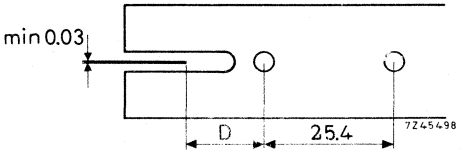
Vane material	any metal
Vane dimensions for aluminium:	
minimum width for a thickness of 2 mm	8 mm
minimum thickness	0,03 mm

As a rule of thumb the thickness of the vane should be about 10 x the electrical resistivity of the material used.

Instead of a vane a disc with holes of indicated dimensions may be used.



The data given below are based on a movement of an aluminium vane 50 x 50 x 2 mm in longitudinal direction.
The operating distance D (see figure below) is the distance at which the output just drops to zero (measured from the centre of the hole nearest to the gap).
Hysteresis is defined as the distance between the vane position at which oscillation ceases and that at which oscillation starts.

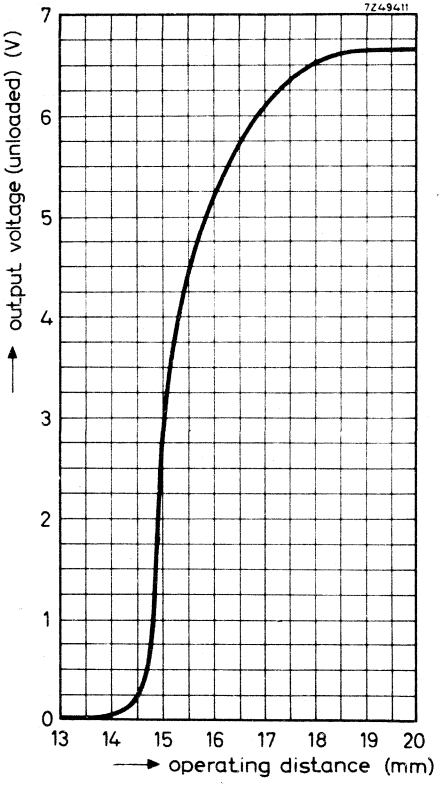


Operating distance D	
open circuit	14,6 ± 1,5 mm
with PS 1 or PS 10 (0 to 1)	15,3 ± 1 mm
Hysteresis	
open circuit	< 1 mm
with PS 1	0,03 mm
with PS 10	0,6 mm

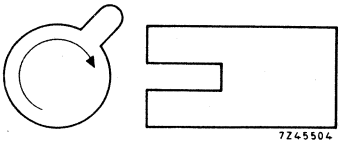
Variation of D with supply voltage

supply voltage	operating distance (mm)
nominal	D
nominal −5%	D +0,06
nominal +5%	D −0,06

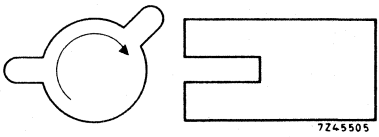
Variation of D with temperature (from −25 to +85 °C)	< 2.7 mm D is maximum at −25 °C
Variation of D with time (at T_{amb} = 25 °C and V_{supply} = 12 V ± 1%, reference point is half the unloaded output voltage of VSO without vane)	< 0.02 mm
Variation of output voltage with D	see typical curve, figure below. From the steep curve it can be seen that a switching point will be kept within very narrow mechanical tolerances.



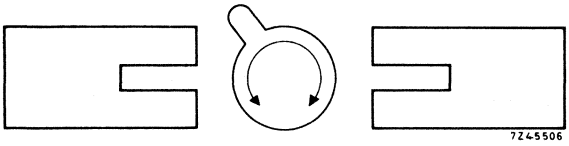
APPLICATION SUGGESTIONS



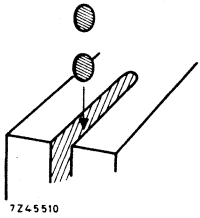
counting of revolutions



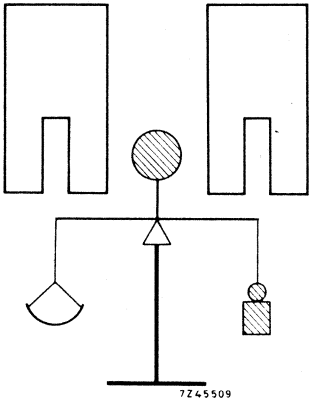
angular position switching (programming)



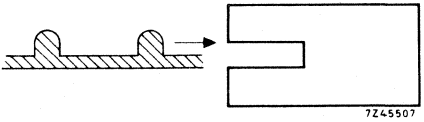
bidirectional counting



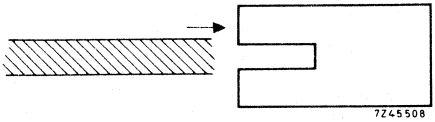
counting of small objects



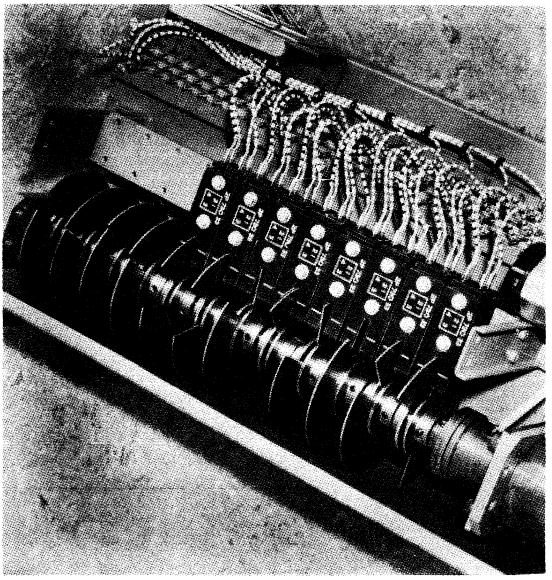
weighing or dosing



linear position switching (programming)

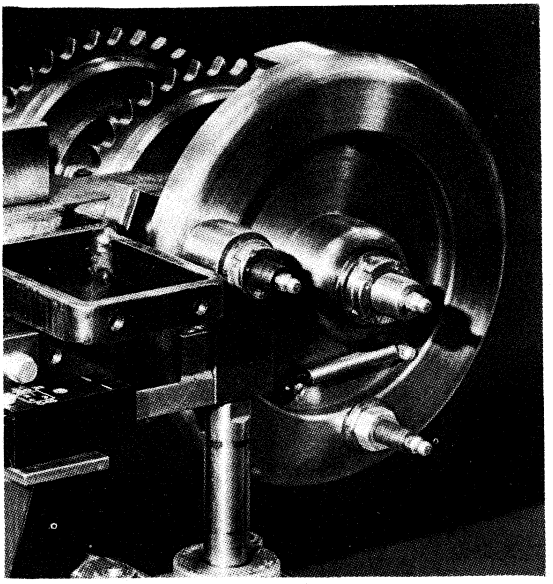


foil continuity check



Eight VSO's used in a disc programmer for control of a metal-working machine.

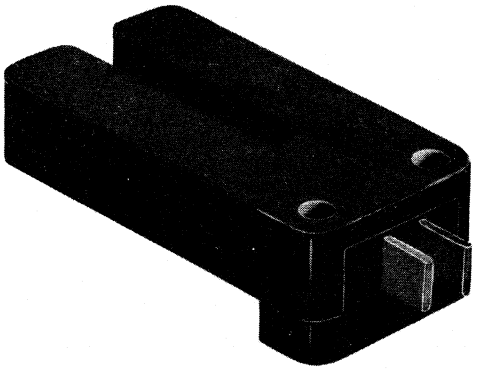
RK 9230-4



VSO control of pneumatic metal-forming machine.

RK 9230-5

IRON VANE SWITCHED REED



RZ21773-3

Maximum switching frequency	100 Hz
Operating-temperature range	−25 to +70 °C

APPLICATION

The iron vane switched reed can be applied as a limit switch, position indicator or as a signal source for low counting speeds.
In conjunction with d.c. amplifiers (UPA61, TT61 or TT60), the IVSR can be used for power switching.
As the IVSR is free from most of the difficulties encountered with mechanical switches, it can succesfully replace micro switches.

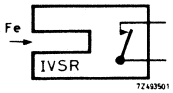
CONSTRUCTION

The IVSR consists of a magnet and a reed switch encapsulated in an U-shaped plastic housing.
When there is no piece of iron (vane) in the gap between the reed switch and the magnet, the reed switch is closed. Inserting a piece of iron of suitable dimensions in the gap reduces the magnetic flux through the reed to such an extent that the reed switch opens.
In this way it is possible to obtain signals that indicate the position of the iron vane.

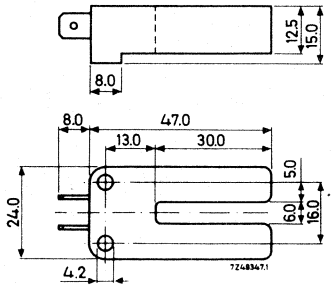
The weight is approximately 20 g.

The IVSR can be mounted in any position. Two mounting holes allow the use of 4 mm bolts. When IVSR's are mounted on a common support, the minimum distance between the housings is 36 mm, to avoid interaction. For mounting IVSR's over each other, this distance is 60 mm.

Connection can be made by means of 0,250" Fastons or by soldering.



Drawing symbol



Dimensions in mm

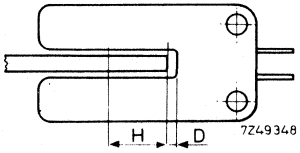
TECHNICAL PERFORMANCE

Load switching capacity (non inductive)	$\leq$ 1.2 VA
Voltage switching capacity	$\leq$ 32 V_{dc}
	$\leq$ 50 V_{ac}
Current switching capacity (non inductive)	$\leq$ 0.1 A_{dc}
Switching frequency	$\leq$ 100 Hz
Contact resistance, measured at 10 mV	
at open circuit	< 150 mΩ
Contact capacitance	$\leq$ 5 pF
Insulation resistance, measured at 250 V_{dc}	
at open circuit	$\geq 10^8$ Ω
Test voltage, measured at open circuit	
for 1 min	500 V_{dc}
Permissible operating-temperature range	−25 to +70 °C
Permissible storage-temperature range	−40 to +85 °C

APPLICATION INFORMATION (typical values)

Vane material	mild steel

The data given are based upon a movement of a mild steel vane 30 x 10 x 4 mm, placed centrally in the gap, in longitudinal direction.



The operating distance (D) is the distance between the front edge of the vane and the rear of the gap at which the reed switch opens.
The hysteresis (H) is defined as the distance between the vane position at which the reed switch opens and that at which the reed switch closes.

Operating distance	4 ± 3 mm
Hysteresis	10 ± 3 mm

APPLICATION SUGGESTIONS

As the reed switch is normally closed, the following two modes of operation can be distinguished:
- output voltage is present when there is no vane in the gap (Fig.a)
- output voltage is present when there is a vane in the gap (Fig.b)

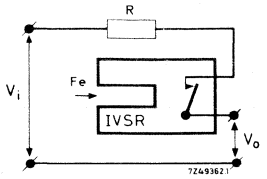


Fig.a

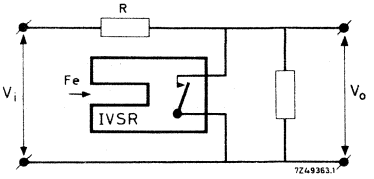


Fig.b

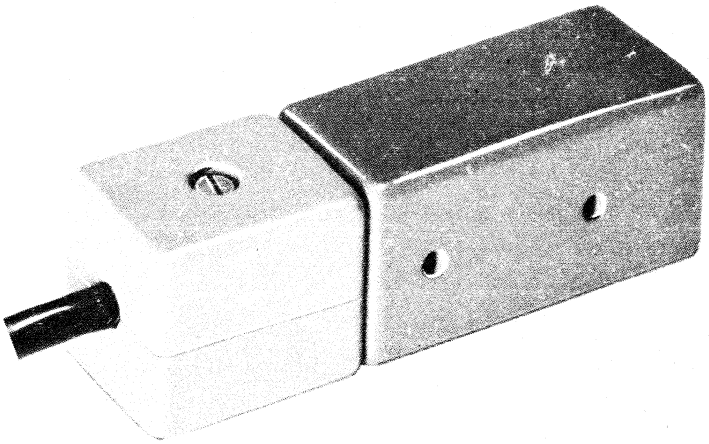
Notes

It is obvious that the IVSR should not be used in environments where iron dust or scraps might impair its operation.

It should be realised that capacitance directly across the switch terminals can be the cause of high currents through the switch at the moment of closing the contacts. This should be avoided by having sufficient resistance in the proper contact circuit.

In case the switch is used with electronic circuitry in which bounce might give rise to malfunctioning of the equipment, appropriate circuitry should be added to get rid of the bounce effect. The safe way out is the use of a one shot multivibrator.
Another solution that sometimes can be used, is applying a low pass RC network between the IVSR and the input of the equipment.

ELECTRONIC PROXIMITY DETECTOR



Supply voltage	12 V_{dc}
Maximum detection frequency	1 kHz
Operating-temperature range	-25 to +85 °C

GENERAL

The electronic proximity detector is a static switching device, the switching action being determined by the presence of a metallic object. The metal can be any electrically conducting material of rather arbitrary shape.
It can be applied as a detector for the presence, passage or position of metal parts and is a versatile tool in various industrial automation set-ups.

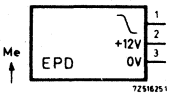
The EPD contains an oscillator which is link coupled to a detector. The detector is followed by an amplifier.
The oscillator coils and the coupling link are placed in a potcore half. In this way a well-defined field is set up in front of the open side of the potcore, located at the front side of the EPD. Bringing a piece of metal in this field the oscillator output and subsequently the output of the amplifier decreases, due to the loading effect of the eddy current losses in the metal.
When no piece of metal is near, the output voltage of the EPD is approximately 12 V. It will decrease in proportion to the reduction of the oscillator output, resulting from a metal object coming nearer.

The complete circuit is epoxy encapsulated in a polycarbonate housing.

The weight is approximately 120 g.

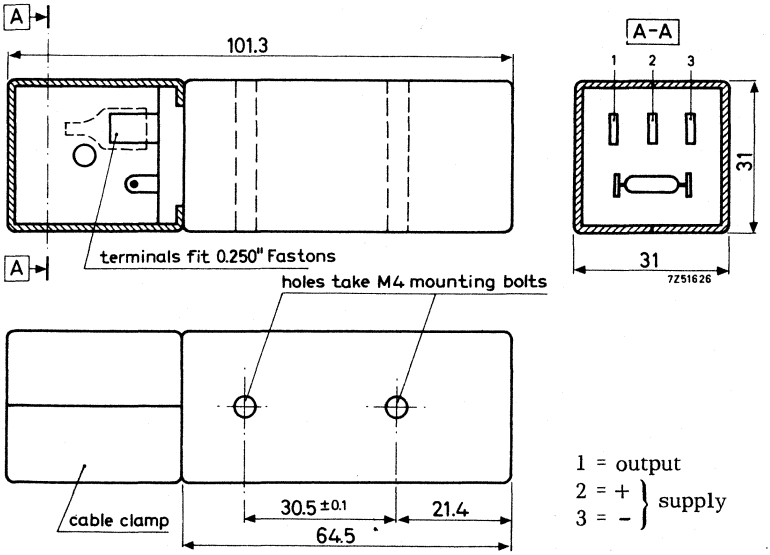
The unit may be mounted in any position. Two mounting holes allow the use of 4 mm bolts.

Connection can be made by 0.250" Fastons or by soldering. A cable clamp consisting of two equal caps is supplied with each EPD. This clamp permits either end or top entrance of a 3-core cable of 7 mm diameter.



Drawing symbol

Dimensions in mm



Note

The resistor between the two 0.110" Fastons is an adjustment resistor for the oscillator loop gain; it should not be changed.

TECHNICAL PERFORMANCE

Supply voltage (V_S)	12 V_{dc} ±5% or +6 V_{dc} ±5% and −6 V_{dc} ±5% (with common 0 V) or 24 V_{dc} via series resistor and 12 V zener diode, giving a stabilised supply voltage of 12 V. (See also APPLICATION SUGGESTIONS.)
limiting value	abs. max. 15 V *) (destructive at $T_{amb} \geq 40$ °C)
Consumed current (nominal value)	16 mA
Output voltage, no object being detected	approximately V_S − 0.5 V
Output resistance no object being detected	680 Ω ±10%
object being detected	3.3 kΩ
Hysteresis for output voltages of 100 mV − 11 V	0 mm
Minimum load	1 kΩ
Maximum detection frequency	1 kHz
Noise (over supply lines)	< 10 mV
Ambient temperature range operating storage	 −25 to +85 °C −40 to +85 °C

APPLICATION INFORMATION (typical values)

Detection graphs

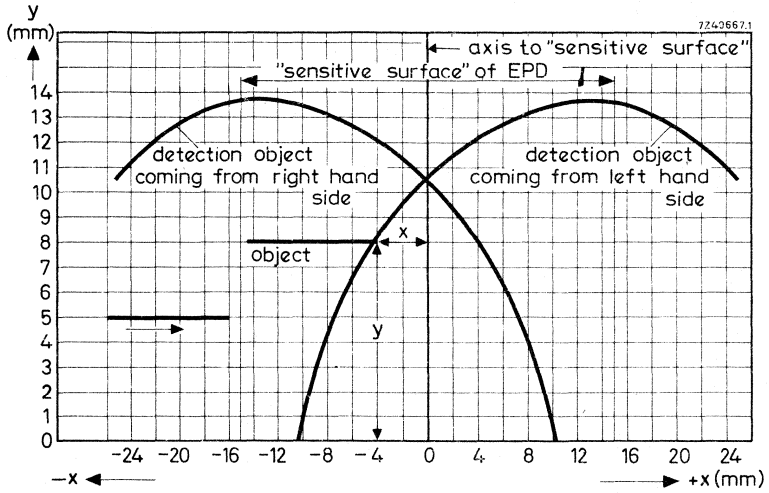
Detection of a rectangular mild steel reference object, 50 x 25 x 1 mm

Sensitive surface	surface of 31 x 31 mm at the opposite end of the EPD to the terminals
Axis	line perpendicular to the centre of the sensitive surface
Operating point	point at which the output voltage of the EPD is reduced to 100 mV (moment of detection)

*) Reversal of supply voltage will damage the detector.

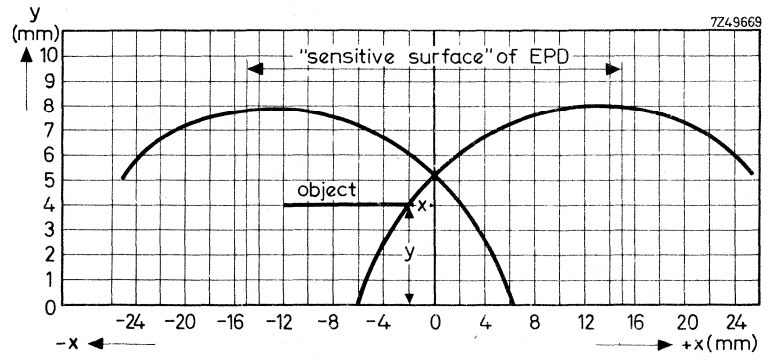
Operating distance — distance of the leading edge of the reference object to the axis at the operating point (x-operating distance)

Detection range — distance of the reference object to the sensitive surface (y-operating distance)



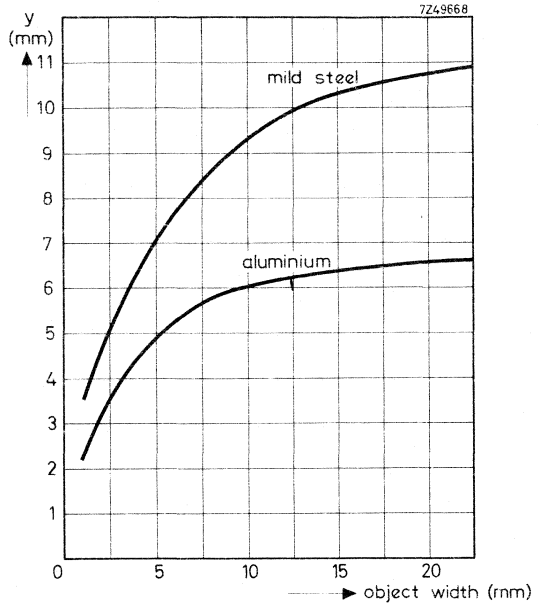
From the graph it can be seen that the object is detected before the axis is reached if it passes at a distance of < 10 mm from the sensitive surface. If it passes at a distance of e.g. 13.5 mm, the object is detected after the axis has been passed.

Detection of a rectangular aluminium reference object, 50 x 25 x 1 mm

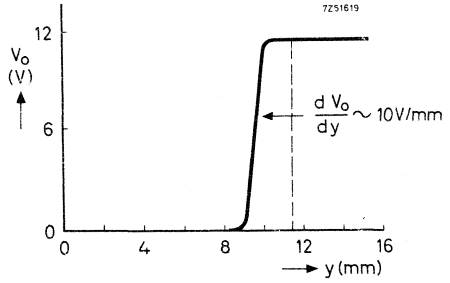


Detection of rectangular mild steel and aluminium reference objects (50 x 1 mm) with different widths

Object approaches the centre of the sensitive surface perpendicularly from in front.



Output voltage as a function of the position of a rectangular mild steel reference object, 50 x 25 x 1 mm



Upon frontal approach of the object to the sensitive surface, the output voltage of the EPD will change from over 11 V to 100 mV within 1 mm from the position in which the output voltage starts to change.
This characteristic is extremely important when the EPD is used as a position detector.

Notes:

The detection graphs may differ slightly from unit to unit.

Quite small objects can be detected when brought close to the sensitive surface. Thickness is relatively unimportant as eddy currents occur in penetration layer only.

Influence of supply voltage variations

A supply voltage variation of ±5% produces a change of ±0.1 mm in y-operating distance, at 10 mm from the sensitive surface.

Influence of temperature

With the reference object at a y-operating distance of 10 mm (at −25 °C) a change in temperature of both EPD and object will cause the y-operating distance to change less than 2 mm over the range from −25° to +85 °C.

Direction of approach

As the exterior field is rotation symmetrical the path along which the detection position is reached is immaterial.

Distance from metallic surroundings

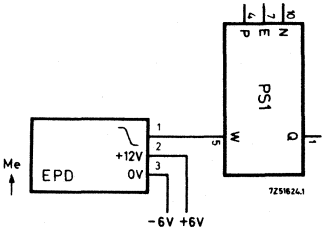
Clearance from metallic surrounding: 30 mm (this applies for sensitive front part of unit).

Spacing required between two detector axes with sensitive surface in the same plane: 60 mm.

Spacing required between two reference objects to give discrete detection: 50 mm. (This property can be put to use in feeder systems, a gap being used to initiate part supply restart.)

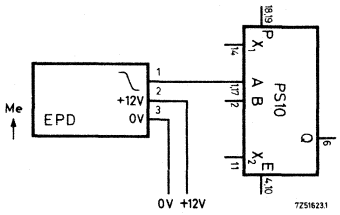
APPLICATION SUGGESTIONS *)

EPD in conjunction with 100 kHz-Series circuit blocks

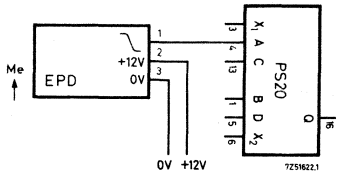


*) With long cables between EPD and subsequent electronics RC decoupling of interference can be employed.

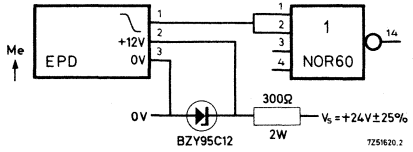
EPD in conjunction with 10-Series circuit blocks

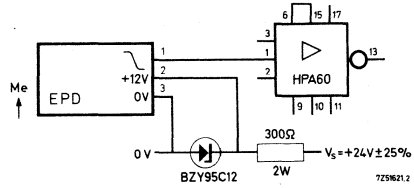


EPD in conjunction with 20-Series circuit blocks



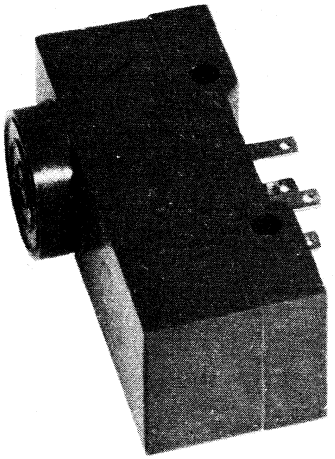
EPD in conjunction with 60-Series Norbits





MINIATURE ELECTRONIC PROXIMITY DETECTOR

QUICK REFERENCE DATA	
Supply voltage	24 V (d.c.) ±25%, or 12 V (d.c.) ± 5%
Maximum detection frequency	1 kHz
Operating temperature range	−25 to + 70 °C
Detection range	3 mm



RZ 28513-2

APPLICATION

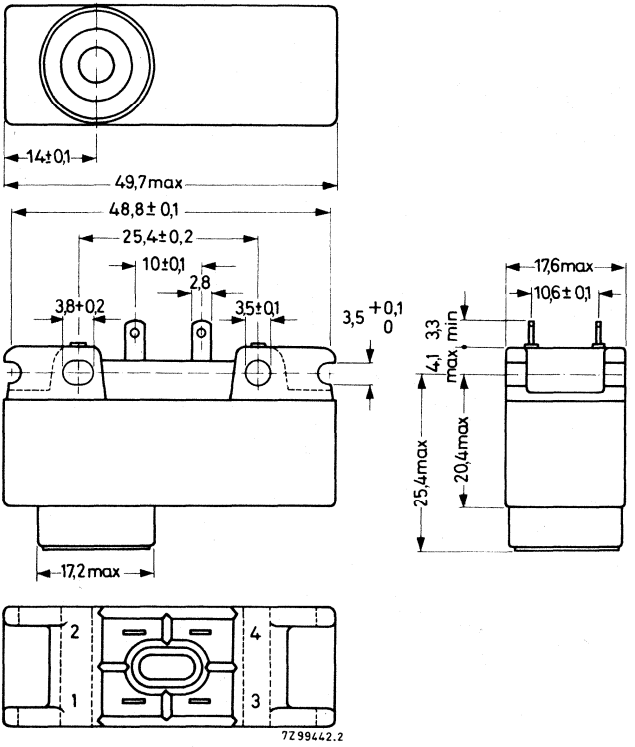
The EPD 60 can be applied as a static switching device, the switching action being determined by the position of a metal object. In this way a static equivalent for the well-known mechanical miniature switch is obtained.

DESCRIPTION

The circuit consists of an oscillator followed by a detector and an amplifier.
The oscillator coil, placed in a potcore half, which is located in the cylindrical part of the housing, sets up a well defined field.
If there is no metal object in the field of the coil the output is low, if a metal object of adequate size is brought far enough into the field, the oscillator will be damped in such a way that the output of the unit goes "high".
The unit is potted in a polydiallylphtalate resin housing, the dimensions of which are compatible with standard mechanical miniature switch housings, see photograph below. Connection to the unit can be made by means of 0.110 inch Fastons or by soldering.

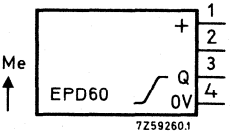
MECHANICAL DATA

Dimensions (mm)



Terminal location

Terminal 1 = +24 V
2 = +12 V (connect 2 and 1)
3 = output (Q)
4 = 0 V common



Drawing symbol

Colour red

Weight 30 g approximately

Mounting

The unit may be mounted in any position. Two mounting holes allow the use of 3 mm bolts. Two grooves in the short sides are provided for bar mounting. Any number of units may be stacked side by side.

ELECTRICAL DATA

Supply voltage (V_S) *)	+24 V ±25%, or +12 V ± 5%
Consumed current (nominal)	15 mA
Limiting value of V_S	
terminal 1	+35 V
terminal 2	+15 V
Ambient temperature range	
operating	−25 to +70 °C
storage	−40 to +70 °C
Maximum detection frequency	1 kHz
Noise on supply lines due to switching	< 5 mV

Output data

			V_S = +24 V		V_S = +12 V	
Output low	at I_Q	=	0	mA	0	mA
	max. V_Q	=	+0.3	V	+0.3	V
Output resistance		=	3	kΩ	3	kΩ
Output high	at − I_Q	=	0.41	mA	0.20	mA
	and at min. V_S	=	18.0	V	11.4	V
	at loading equivalent	=	3 D.U. in 24 V nom. 60-Series operation		2 D.U. in 12 V nom. 60-Series operation	
	V_Q	=	min.+11.4	V	min.+8.3	V
	max. V_Q	=	max.V_S		max.V_S	
Output resistance		=	15	kΩ	15	kΩ

External short-circuit (from Q to V_S and from Q to 0V common) is not destructive.

APPLICATION INFORMATION

The EPD 60 can be switched by moving either a ferrous or a non-ferrous metal object of any size and form in front of the detection head. If the object is ferrous the resulting damping on the oscillator is proportional to the volume of the object; in the case of a non-ferrous object it is governed by the conductivity of the material. Thus, a perfect conductor cannot be detected unless it is sufficiently thin and brought close to the detection head.

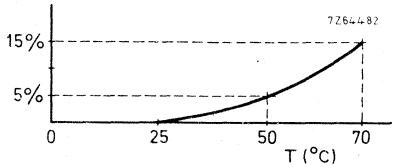
*) Accidental polarity reversal is not destructive.

Operating distance

The operating distance (X) is the distance between the centre of an object and the centre of the detection head at which the output is about to go "high" (measured axially)

For circular steel disc (ϕ15 mm), d = 0, 2 mm in centre of axis, X = 3 mm ± 10%

Influence of temperature in % of X_{nom}



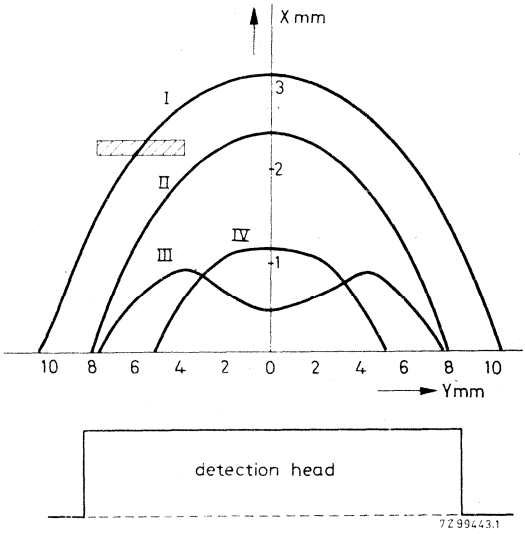
Influence of supply voltage (18 to 30 V) $\Delta X < 20\,\mu m$

Hysteresis $< 50\,\mu m$

For reference purposes four standard objects are used:

Object I : mild steel, circular disc Ø 15 mm, thickness 0.2 mm
Object II : mild steel, circular disc Ø 10 mm, thickness 0.2 mm
Object III : copper, circular disc Ø 15 mm, thickness 0.04 mm
Object IV : copper, circular disc Ø 10 mm, thickness 0.04 mm

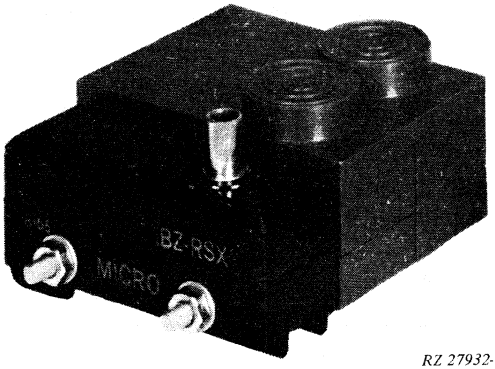
The graph below gives X for each of the four standard objects traversing the sensitive area of the detection head along any straight line parallel to the surface of the head, intersecting the axis of the head.



CLIMATIC TESTS

According to 60-series Norbits

Protection degree according to DIN 40.050 P55 (IP66)

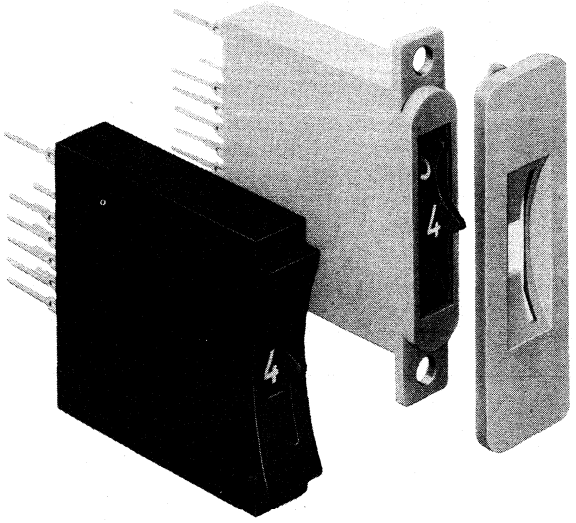


RZ 27932-12

The photograph shows two EPD 60's together with a "Microswitch".

THUMBWHEEL SWITCHES

A 51168



Contact resistance	≤ 50 mΩ
Operating temperature range	−25 to +85 °C.

APPLICATION

These thumbwheel switches have been developed to be used as pre-set devices in digital control systems in which numerical information is handled.

CONSTRUCTION

Housing	shock resistant polycarbonate colour: grey (facade mounting) black (block mounting)
Facades	polycarbonate standard colour: grey *)
Contact springs	heat-treated copper beryllium
Contact surface	721 rolled alloy (70% gold, 20% silver, 10% copper)
Terminals	tinplated brass suited for soldering or wire-wrapping
Thumbwheel	high grade plastic, standard colour black **), provided with white figures or signs

*) Also available in several other colours on request.
**) Also available in red on request.

Thumbwheel detent	copper beryllium spring with low wear molybdenum bisulfide doped snap
Printed wiring boards	glass-epoxy; goldplated tracks
Type identification	catalog number is given on the closing strip at the rear, type abbreviation on housing

Dimensions in mm

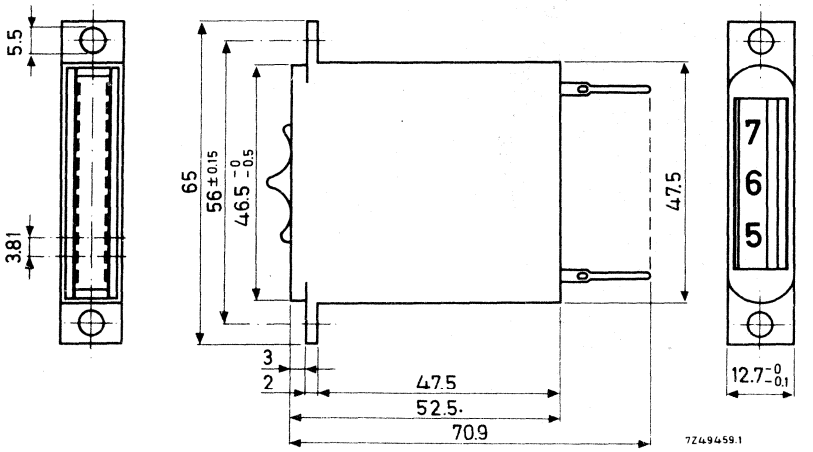


Fig. 1. Switch for facade mounting.

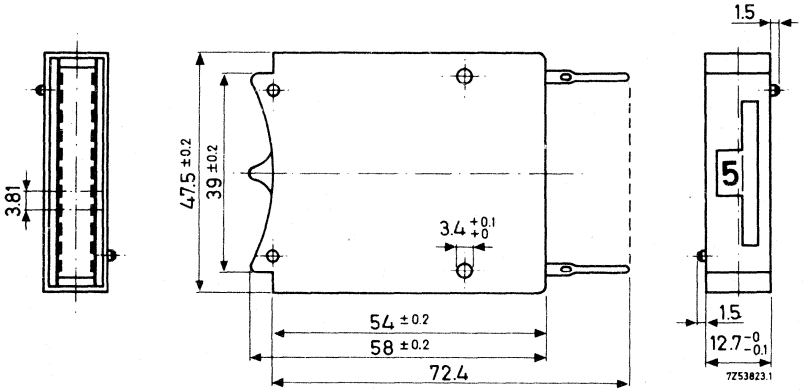


Fig. 2. Switch for block mounting.

TECHNICAL PERFORMANCE

Working voltage	60 V d.c.
Test voltage for 1 min *)	500 V d.c.
Insulation resistance, measured at 100 V d.c. *)	$\geq 10^9\ \Omega$
Power switching capability at resistive load	12 W
Current switching capacity in purely resistive circuits	0,1 A d.c.
Maximum current carrying capacity	0,5 A d.c.
Contact resistance measured at 20 mV, 0,1 A, 1 kHz	$\leq 50\ m\Omega$
Losses (tan δ), measured at 1 MHz between any terminal and all others connected together to earth	$\leq 25.\ 10^{-4}$
Capacitance, measured at 1 MHz between any pair of terminals and between any terminal and all others connected together to earth	≤ 15 pF
Operating temperature range	−25 to +85 °C
Storage temperature range	−40 to +85 °C
Life	in excess of 100 000 complete rotations at a rate of 1 step/s
Operating torque after 20 000 rotations	25 to 75 mNm 15 to 65 mNm
Dimensions of the figures on the thumbwheel	6 x 4 mm, line thickness 0,8 mm
Weight	30 g approximately
Quality control tests, IEC 68-2:	
test Aa, cold	−55 °C
test Ba, dry heat	100 °C
test C, damp heat	56 days
test F, vibration	–
test Na, temperature cycling	−55 to +100 °C
test Ea, shock	–
test T, solderability	0 hours and 56 days

FAÇADE MOUNTING

The switches can be mounted in panels with a thickness up to 4 mm by means of mounting façades and the screws and washers supplied (see Fig. 3). When the panel thickness is less than 4 mm, additional washers must be used between the panel and the switch. The following mounting façades, giving facilities for mounting up to 10 switches, are available (Fig. 4).

*) Between any pair of terminals and between any terminal and all others connected together.

mounting façade	number of switches	catalog number
FMF 1	1	4311 027 80598
FMF 2	2	4311 027 80608
FMF 3	3	4311 027 80618
FMF 4	4	4311 027 80628
FMF 5	5	4311 027 80638
FMF 6	6	4311 027 80648
FMF 7	7	4311 027 81163
FMF 8	8	4311 027 81173
FMF 9	9	4311 027 81183
FMF10	10	4311 027 81193

The facades are normally supplied in grey, but are also available in several other colours on request.

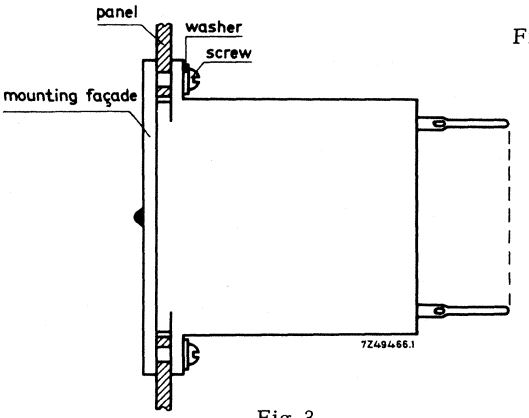
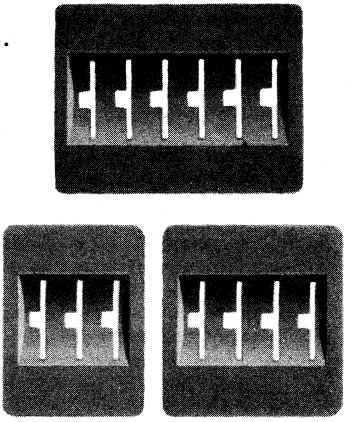


Fig.3.

Fig.4.



The dimensions of the necessary panel holes are indicated in Fig.5; the outline of the mounting façade is indicated by a dash line.

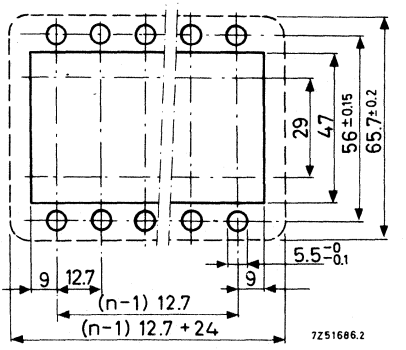


Fig.5.

(n = number of switches)

BLOCK MOUNTING

Type BM switches, which do not require a front facade, can be "block mounted" by means of mounting brackets and 3 mm tie rods, and can be supplied coupled in master-slave arrangements. Maximum allowable couple applied to the nuts to clamp the switches to each other is 750 gcm. Accessories include:

a) BM CLO, catalogue number 4311 027 82141
(a blank housing suitable as distance piece for future extension, for housing slave switches or ancillary circuits, or for engraving)

BM CLD, catalogue number 4311 027 83491
(BM CLO provided with a decimal point)

b) BM SEP, catalogue number 4311 027 82161
(a spacer suitable for left and right hand mounting)

c) BM EXT, catalogue number 4311 027 82151
(end piece suitable for left and right hand mounting)

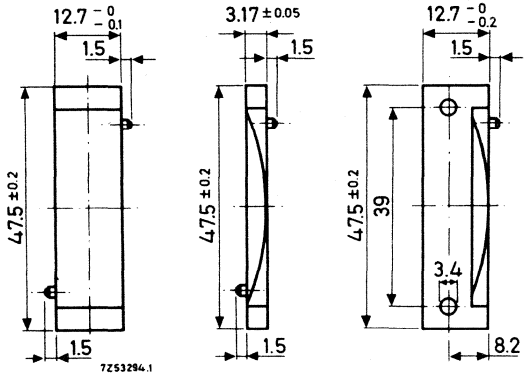
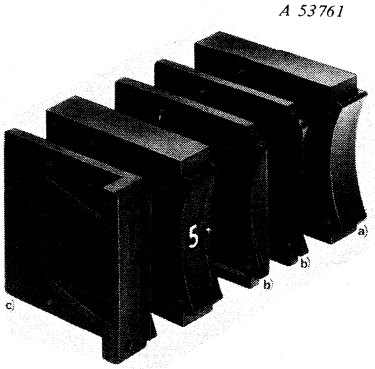


Fig. 6. Spacers and end piece



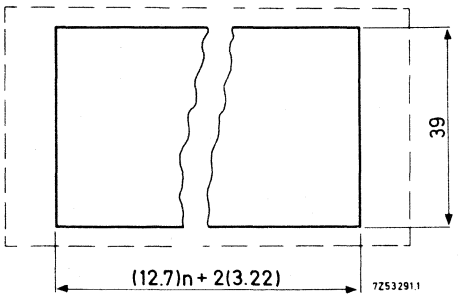


Fig. 7. Panel cut-out
(n = number of switches)

SURVEY OF TYPES

	description	abbreviation	figures or signs *)	catalog no. 4311 027 ..... facade mounting	block mounting
decimal and 2 position switches	10 position 2 pole switch	10P2C	0 - 9	82201	82521
	10 position 1 pole switch	10P1C	0 - 9	82321	82401
	2 position 4 pole sign switch	2P4+ −	+, −	82231	82641
	2 position 2 pole sign switch	2P2+ −	+, −	82341	82601
	2 position 4 pole sign switch	2P4x ÷	x, ÷	82311	82651
	2 position 2 pole sign switch	2P2x ÷	x, ÷	82351	82611
binary decoding switches (including 4 diodes BAX13 and a resistor of 12 kΩ)	decoding switch 1248 negative logic	1248N	0 - 9	82221	82391
	decoding switch 1248 positive logic	1248P	0 - 9	82251	82411
	decoding switch 1242 (jump at 8) negative logic (Berkeley code)	1242N	0 - 9	82211	82711
	decoding switch 1242 (jump at 8) positive logic (Berkeley code)	1242P	0 - 9	82241	82721
	decoding switch 1248 negative logic **)	1248N/C	0 - 9	82451	82541
	decoding switch 1248 positive logic **)	1248P/C	0 - 9	82431	82551
	decoding switch 1242 (jump at 8) negative logic **)	1242N/C	0 - 9	82441	82571
	decoding switch 1242 (jump at 8) positive logic **)	1242P/C	0 - 9	82421	82581
binary coding switches	coding switch 1248	1248C	0 - 9	82271	82531
	coding switch 1242 (jump at 8)	1242C	0 - 9	82261	82701
	coding switch 1248 ***)	1248C/C	0 - 9	82471	82561
	coding switch 1242 (jump at 8)***)	1242C/C	0 - 9	82461	82591
	coding switch 1248	1248S	0 - 9		82511

Note: The contacts of all switches break before make.

*) Other possibilities on request

**) Switch decodes 9-complement of decimal digit on thumbwheel.

***) Switch encodes 9-complement of decimal digit on thumbwheel.

DIAGRAMS AND TERMINAL LOCATION

Rear view obtained when rotating switch round the vertical axis with symbols upright.

10P2C

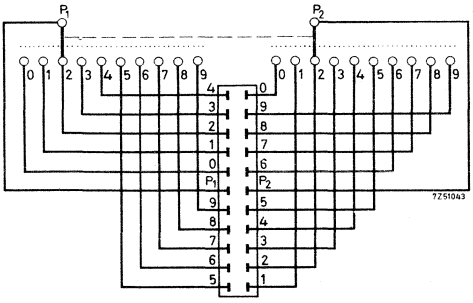


Fig. 9

10P1C

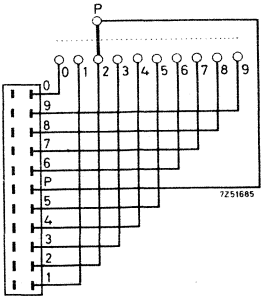


Fig. 10

2P4 + −

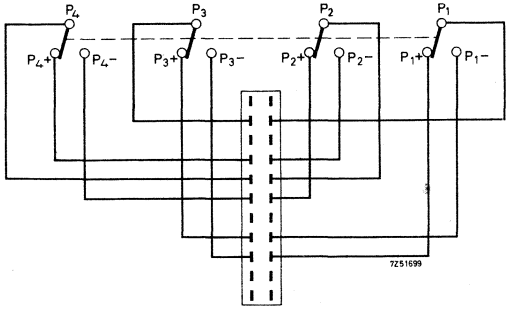


Fig. 11

2P2 + −

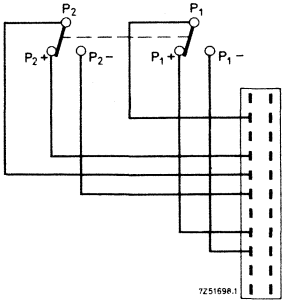


Fig. 12

2P4 x ÷

As diagram of Fig. 11 but with x and ÷ instead of + and − respectively.

2P2 x ÷

As diagram of Fig. 12 but with x and ÷ instead of + and − respectively.

1248N

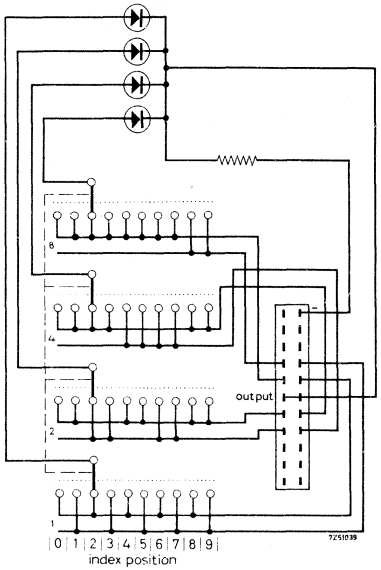


Fig.13

Truth table

Index	1	2	4	8
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

1248P

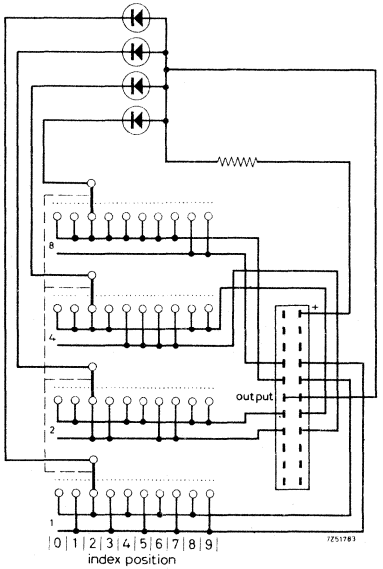


Fig.14

For truth table, see above

1242N

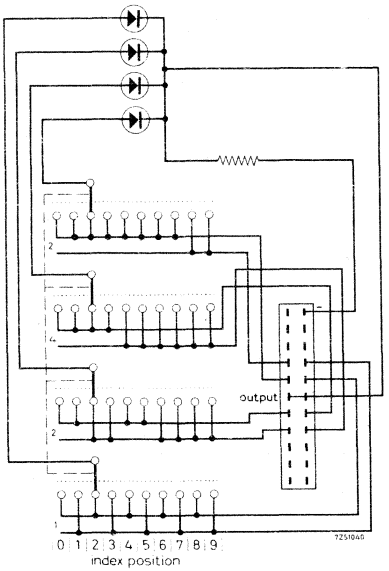


Fig.15

Truth table

Index	1	2	4	2
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	1	1	1
9	1	1	1	1

1242P

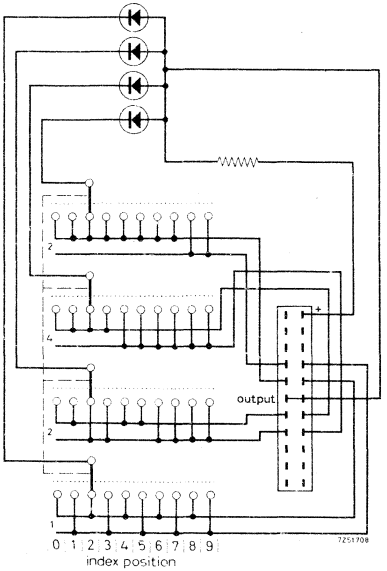


Fig.16

For truth table, see above

1248N/C

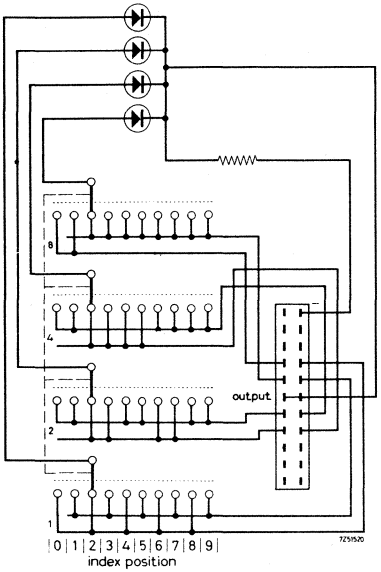


Fig.17

Truth table

Index	1	2	4	8
0	1	0	0	1
1	0	0	0	1
2	1	1	1	0
3	0	1	1	0
4	1	0	1	0
5	0	0	1	0
6	1	1	0	0
7	0	1	0	0
8	1	0	0	0
9	0	0	0	0

1248P/C

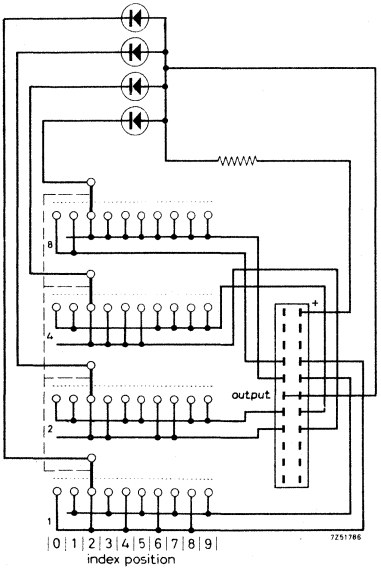


Fig.18

For truth table, see above

1242N/C

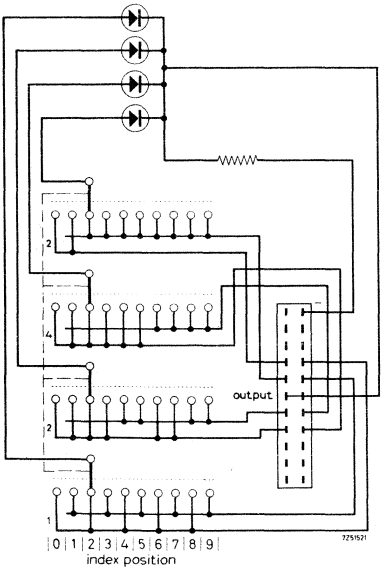


Fig.19

Truth table

Index	1	2	4	2
0	1	1	1	1
1	0	1	1	1
2	1	1	1	0
3	0	1	1	0
4	1	0	1	0
5	0	0	1	0
6	1	1	0	0
7	0	1	0	0
8	1	0	0	0
9	0	0	0	0

1242P/C

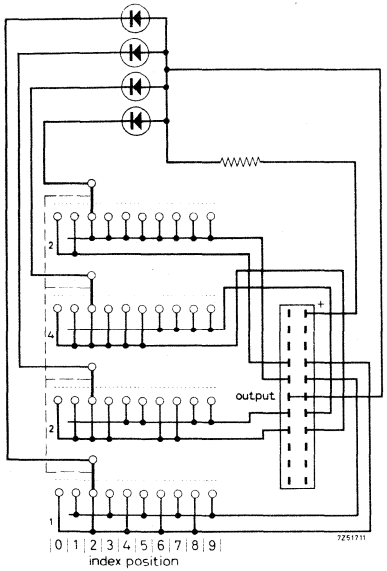


Fig.20

For truth table, see above

1248C

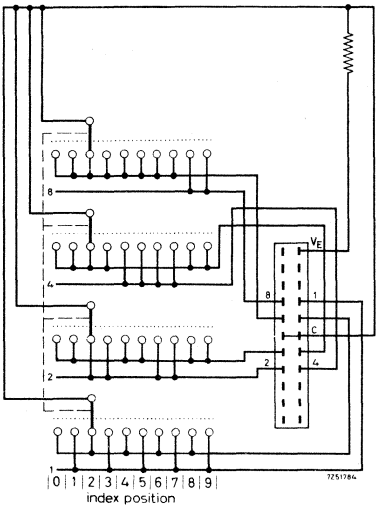


Fig. 21

Truth table

Index	1	2	4	8
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

1242C

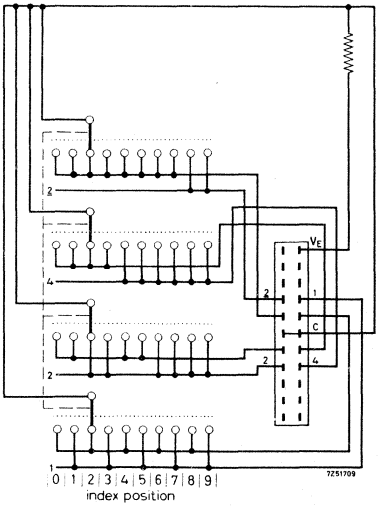


Fig. 22

Truth table

Index	1	2	4	2
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	1	1	1
9	1	1	1	1

1248C/C

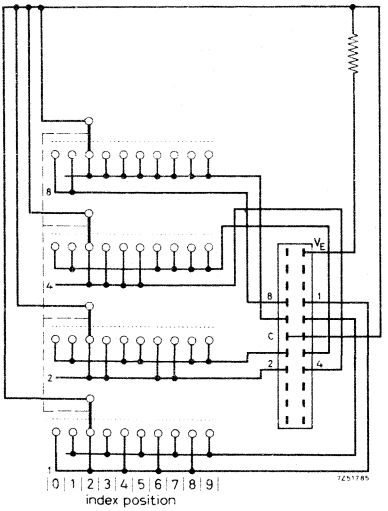


Fig. 23

Truth table

Index	1	2	4	8
0	1	0	0	1
1	0	0	0	1
2	1	1	1	0
3	0	1	1	0
4	1	0	1	0
5	0	0	1	0
6	1	1	0	0
7	0	1	0	0
8	1	0	0	0
9	0	0	0	0

1242C/C

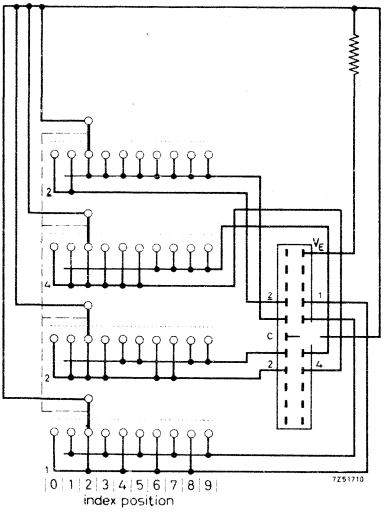


Fig. 24

Truth table

Index	1	2	4	2
0	1	1	1	1
1	0	1	1	1
2	1	1	1	0
3	0	1	1	0
4	1	0	1	0
5	0	0	1	0
6	1	1	0	0
7	0	1	0	0
8	1	0	0	0
9	0	0	0	0

1248S

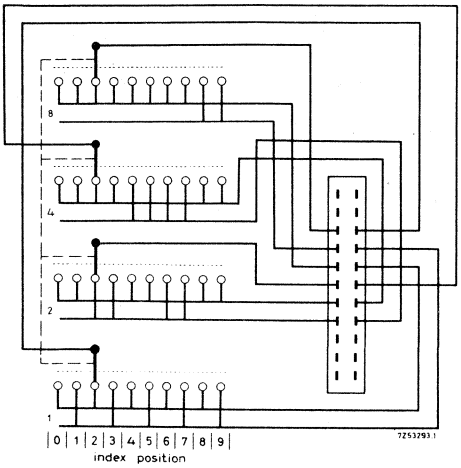


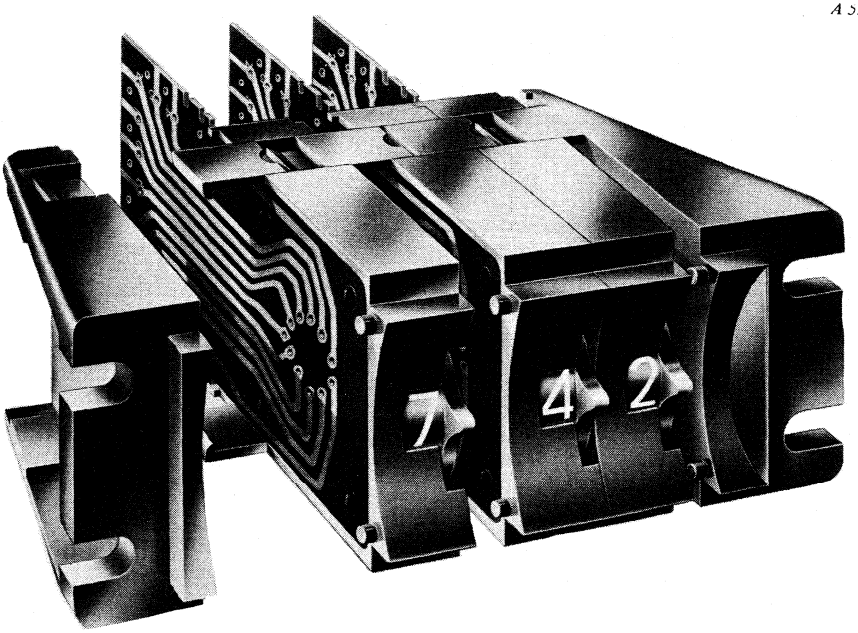
Fig. 25

Truth table

Index	1	2	4	8
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

MINIATURE THUMBWHEEL SWITCHES

A 52941 - 2



Contact resistance	≤ 100 mΩ
Operating temperature range	$-25\ ^{o}C$ to $+70\ ^{o}C$

APPLICATION

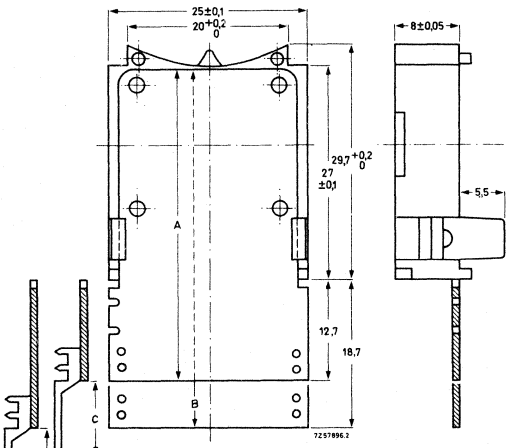
These miniature thumbwheel switches have been developed for use as preset devices in digital systems which have to handle numerical data.

The dimensions are considerably smaller than those of standard switches and allow for easy operation.

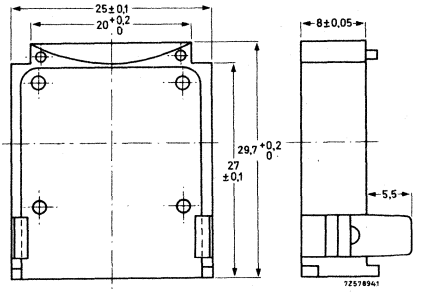
CONSTRUCTION

Housing	black shock-resistant polycarbonate *)
Contact springs	heat-treated copper beryllium
Contact surface	721 alloy balls (70% gold, 20% silver, 10% copper)
Terminals	holes or tin plated pins for wire wrapping
Thumbwheel	black polycarbonate * *) provided with white figures or signs
Thumbwheel detent	steel spring
Printed wiring board	glass epoxy, gold plated tracks on nickel
Stacking	switch housings are provided with "snap in" hooks to eliminate tie bolts
Type identification	catalogue number suffix is given on the rear of the switch, type abbreviation on top of the housing

Dimensions (mm)



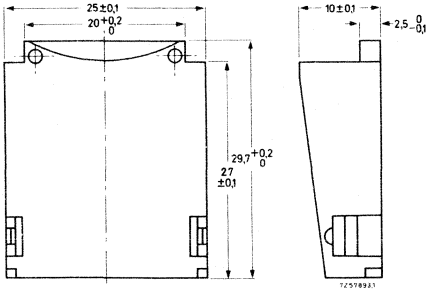
Miniature thumbwheel switch
A: short track plate without diodes
B: long track plate with diodes and for 10P2C
C: 10 mm added to the height for mini-wrap pins



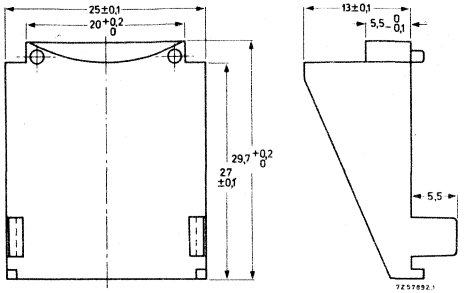
Dimensions in the drawings are in mm

mm	inches	mm	inches
2.5	0.098	18.7	0.736
5.5	0.217	20	0.787
8	0.315	25	0.984
10	0.394	27	1.063
12.7	0.500	29.7	1.169
13	0.512		

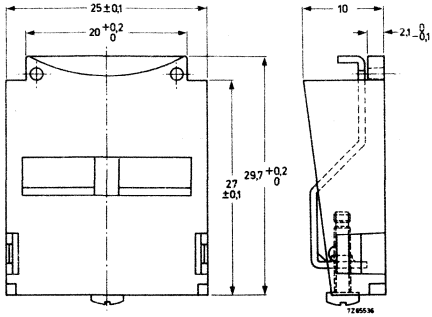
*) in several other colours available on request.
* *) also available in red on request.



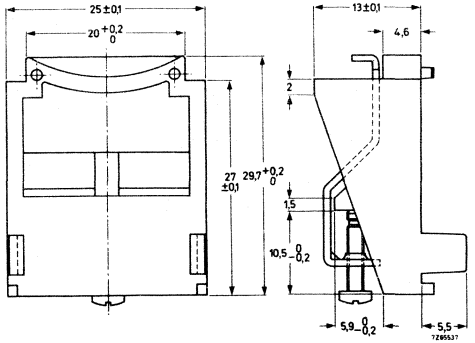
Female end piece (to left of operator) with bolts



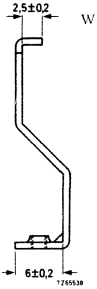
Male end piece (to right of operator) with bolts



Female end piece (to left of operator) with brackets

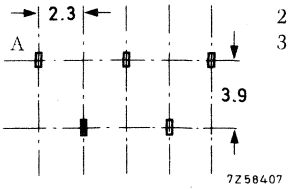


Male end piece (to right of operator) with brackets



Terminal pitch (complementary types)

Terminal A is the most left-hand terminal of the drawings on the pages 55 to 62.

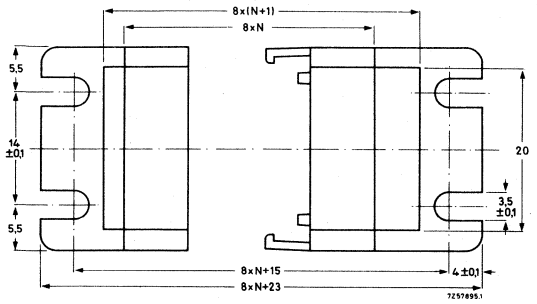


2,3 mm = 0,091 inch
3,9 mm = 0,154 inch

Weight 7 g approx.

Numerals size 5 x 3 mm
line thickness 0,6 mm

Mounting



Dimensions in the drawing are in mm

mm	inches
3.5	0.138
4	0.158
5.5	0.217
8	0.315
14	0.551
15	0.591
20	0.787
23	0.906

TECHNICAL PERFORMANCE

Working voltage	60 V d.c.
Test voltage for 1 min *)	750 V d.c.
Dielectric strength at air pressure of 20 mbar	400 V d.c.
Insulation resistance, measured at 100 V d.c. *)	$> 10^9\ \Omega$
Power switching capability at resistive load	12 W
Current switching capacity in purely resistive circuits	0,1 A d.c.
Maximum current carrying capacity	2 A d.c.
Contact resistance measured at 10 mA	$< 100\ m\Omega$
Capacitance measured at 1 MHz between one terminal and all others connected to earth	< 10 pF
Standard gate resistor	3900 Ω
Operating temperature range	−25 to +85 °C
Storage temperature range	−40 to +85 °C
Life	in excess of 100 000 complete rotations at a rate of 1 step/s
Operating torque	10 to 35 mNm
Dimensions of the figures on the thumbwheel	5 x 3 mm, line thickness 0,6 mm
Weight	10 g approximately
Quality control tests, IEC 68-2:	
test Aa, cold	−55 °C
test Ba, dry heat	100 °C
test C, damp heat	56 days
test F, vibration	–
test Na, temperature cycling	−55 to +100 °C
test Ea, shock	–
test T, solderability	0 hours and 56 days

*) Between any pair of terminals and between any terminal and all others connected together.

SURVEY OF TYPES

Description *)	Type **)	Catalogue number
Decimal switches		
10 position 1 pole switch	M 10P1C	4311 027 84000
	MW 10P1C	84010
10 position 2 pole switch	M 10P2C	84040
+, − switch	M 5x2P1C	84940
	MW 5x2P1C	84950
Double +, − switch	M 5x2P2C	84920
	MW 5x2P2C	84930
Binary switches		
Decoding types:		
decoding switch 1.2.4.8, negative logic, with complement	M 1248/NC	4311 027 84200
	MW 1248/NC	84210
decoding switch 1.2.4.8, positive logic, with complement	M 1248/PC	84240
	MW 1248/PC	84250
Coding types:		
coding switch 1.2.4.8	MW 1248	84170
coding switch 1.2.4.8, with complement	M 1248/C	84160
	MW 1248/C	84290
Encoding types:		
encoding switch 1.2.4.8, with isolating diodes for negative logic	M 1248/N	84080
	MW 1248/N	84090
encoding switch 1.2.4.8, with isolating diodes for positive logic	M 1248/P	84120
	MW 1248/P	84130
Accessories		
Set of two end pieces with bolts		4311 027 84440
Set of two end pieces with brackets		4311 027 88801
Spacer		84590
Spacer with decimal point		84910

Note: The contacts of all switches break before make.

*) Switches can be obtained with figures or signs engraved as ordered by customer.

**) Terminal style: M = without pins (solder direct to track plate)
MW = with pins (for wire wrapping)

SPECIAL VERSIONS

Internally lit switches:

5 V max. Minimum lifetime 50 000 hours (about 6 years). Can also be reduced to 2 V (total darkness). Factory installed.

Limit stop switches:

For prototypes and small series. Catalogue number 4311 027 84411 . Can be installed by customer. For instance switchable to positions 0, 1, 2, and 3 only; stops are provided at positions 9 and 4.

Sealed switches:

Intended for use in hostile environments (dusty or aggressive atmospheres). Contact chamber is sealed by a nylon ring. Available in economy and miniature versions (10P1C). Will be extended to other types. Switches meet dust and sand test acc. to IEC 168-2 and are splash-proof acc. to D.E.F. 13 . Explosion test is in progress.

Colour of housing/rotor and special engraving:

Housing and rotor are normally black (rotor engraved in white). Rotor in red also available. Orders of sufficient quantity can have housing and rotor any colour, and special symbols engraved.

Economy version:

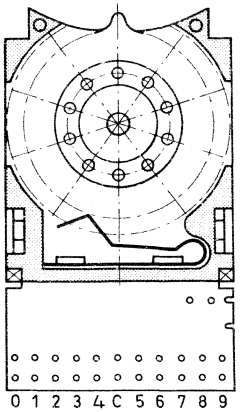
Switches have phenolic resin printed-wiring board instead of glass epoxy. Available as:
- decimal switch PM10P1C (catalogue number 4311 027 89041);
- binary switch PM1248 with true outputs 1, 2, 4, 8 only (catalogue number 4311 027 89001);
- binary switch PM1248C5 with complementary outputs $\overline{1}$, $\overline{2}$, $\overline{4}$, $\overline{8}$, only (catalogue number 4311 027 89031).

Voltage dividers:

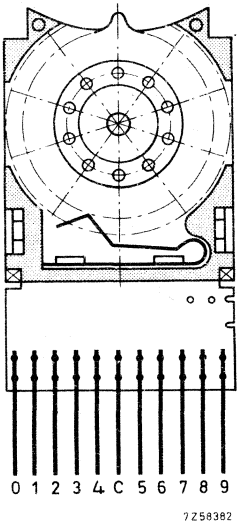
Type M10P1C is also available with printed-wiring boards accommodation for decade resistor network. Switches with resistors mounted can be supplied for larger orders.

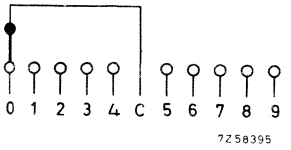
DIAGRAMS AND TERMINAL LOCATION

M10P1C

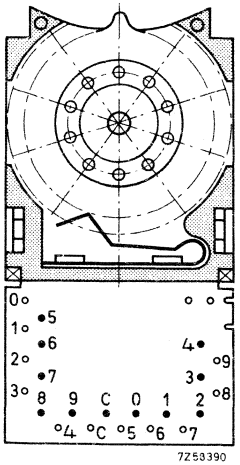


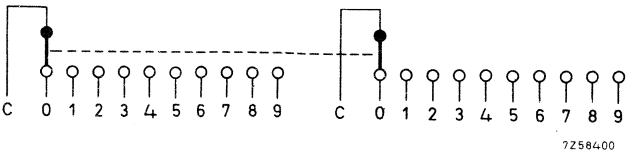
MW10P1C



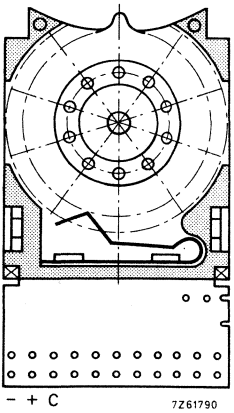


M10P2C

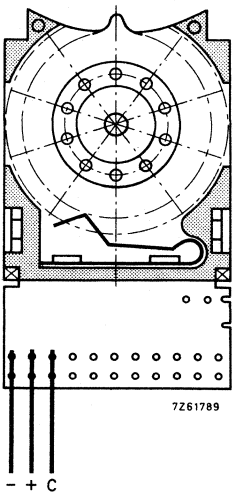


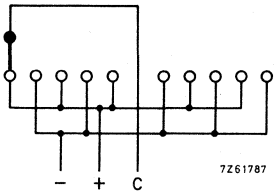


M 5x2 P1C

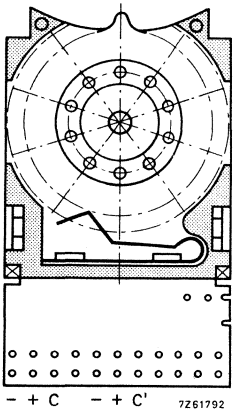


MW 5x2 P1C

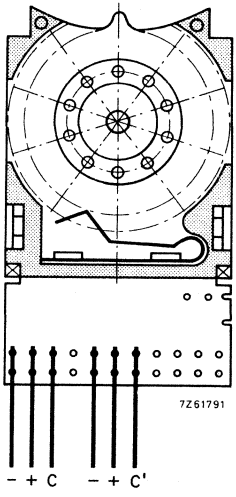


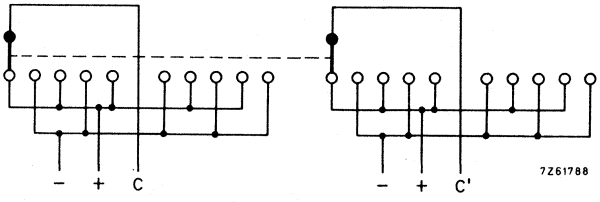


M 5x2 P2C

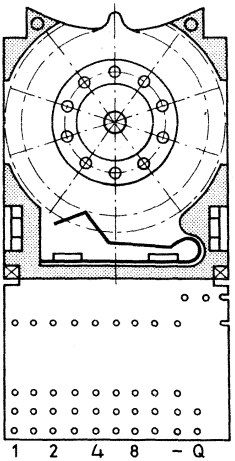


MW 5x2 P2C

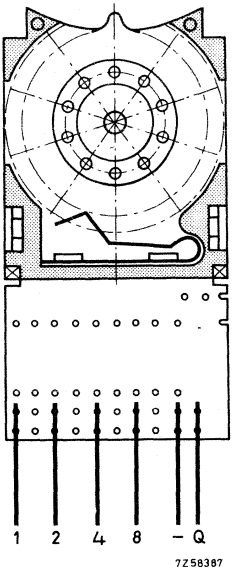




M1248/N



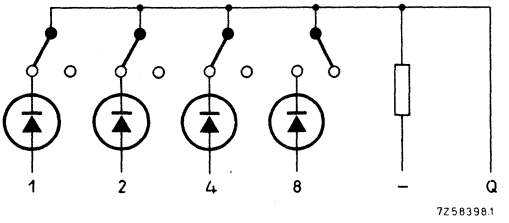
MW1248/N



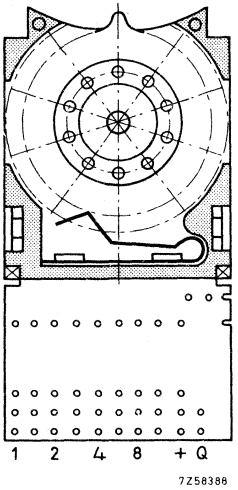
Truth table

Index	1	2	4	8
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

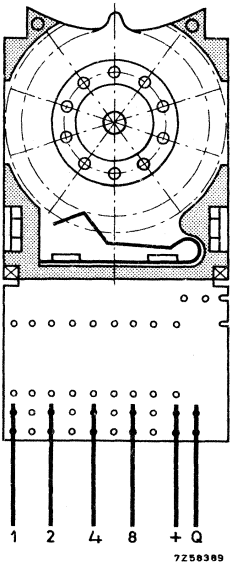
Index 7



M1248/P



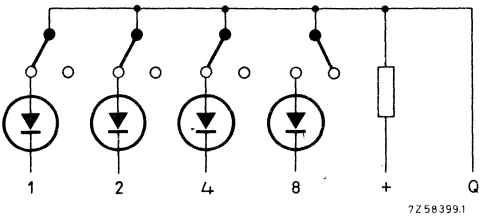
MW1248/P



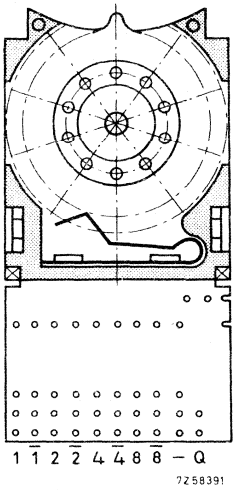
Truth table

Index	1	2	4	8
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

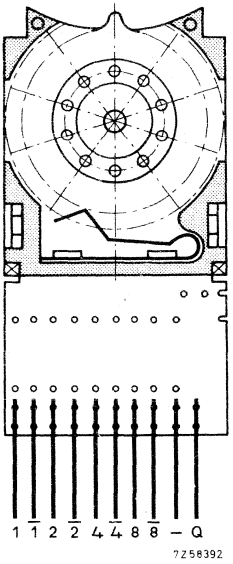
Index 7



M1248/NC



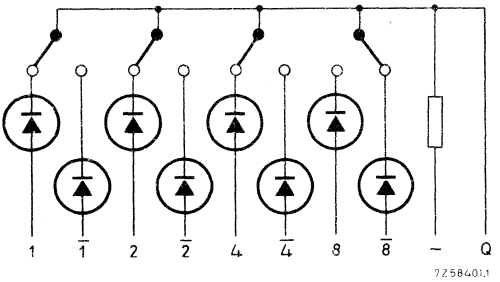
MW1248/NC



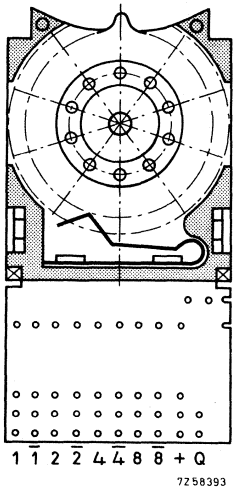
Truth table

Index	1 2 4 8	$\bar{1}$ $\bar{2}$ $\bar{4}$ $\bar{8}$
0	0 0 0 0	1 1 1 1
1	1 0 0 0	0 1 1 1
2	0 1 0 0	1 0 1 1
3	1 1 0 0	0 0 1 1
4	0 0 1 0	1 1 0 1
5	1 0 1 0	0 1 0 1
6	0 1 1 0	1 0 0 1
7	1 1 1 0	0 0 0 1
8	0 0 0 1	1 1 1 0
9	1 0 0 1	0 1 1 0

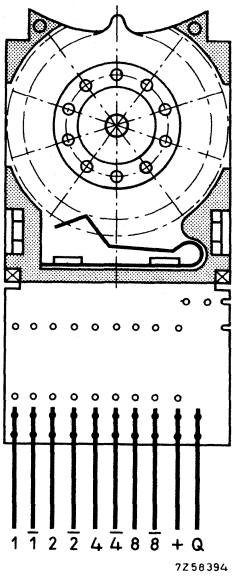
Index 7



M1248/PC



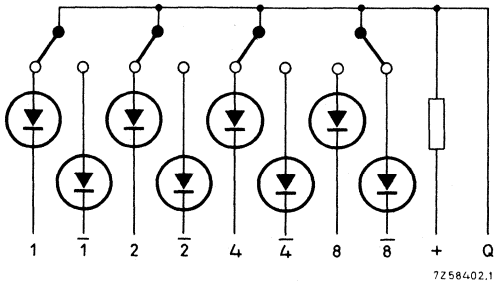
MW1248/PC



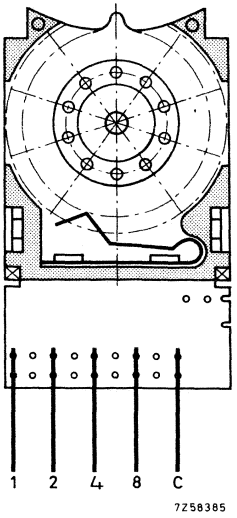
Truth table

Index	1 2 4 8	$\bar{1}$ $\bar{2}$ $\bar{4}$ $\bar{8}$
0	0 0 0 0	1 1 1 1
1	1 0 0 0	0 1 1 1
2	0 1 0 0	1 0 1 1
3	1 1 0 0	0 0 1 1
4	0 0 1 0	1 1 0 1
5	1 0 1 0	0 1 0 1
6	0 1 1 0	1 0 0 1
7	1 1 1 0	0 0 0 1
8	0 0 0 1	1 1 1 0
9	1 0 0 1	0 1 1 0

Index 7



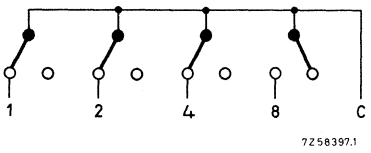
MW1248



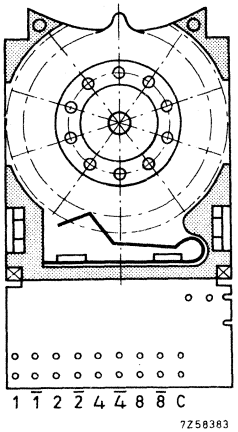
Truth table

Index	1	2	4	8
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

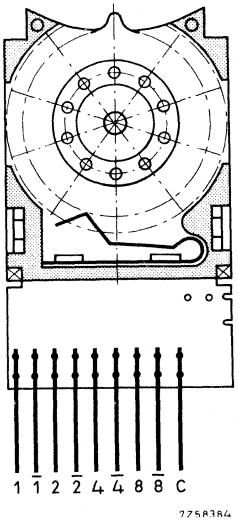
Index 7



M1248/C



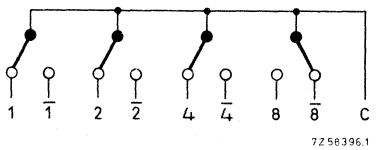
MW1248/C



Truth table

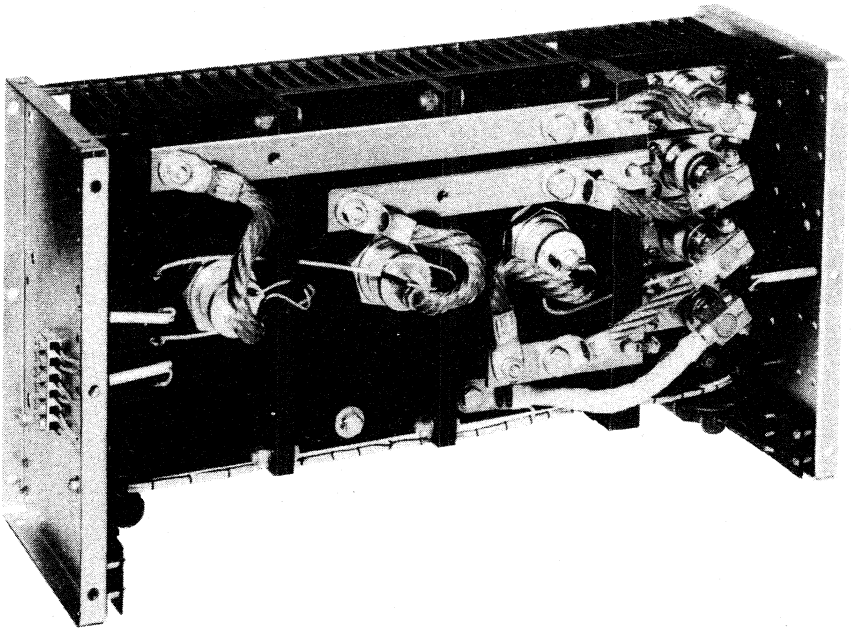
Index	1 2 4 8	$\bar{1}$ $\bar{2}$ $\bar{4}$ $\bar{8}$
0	0 0 0 0	1 1 1 1
1	1 0 0 0	0 1 1 1
2	0 1 0 0	1 0 1 1
3	1 1 0 0	0 0 1 1
4	0 0 1 0	1 1 0 1
5	1 0 1 0	0 1 0 1
6	0 1 1 0	1 0 0 1
7	1 1 1 0	0 0 0 1
8	0 0 0 1	1 1 1 0
9	1 0 0 1	0 1 1 0

Index 7



POWER STACKS WITH DIODES AND/OR THYRISTORS

A 54490 - 3



INTRODUCTION

The "power stacks" are a range of structural units consisting of power semiconductors mounted on their heat-sinks, trigger transformers, RC transient filters, interconnections and terminal blocks. The standard circuit configurations are

diode bridges,
half-control bridges,
full-control bridges and
a.c. controllers

suitable to handle powers ranging from a few kilowatts up to several hundreds of kilowatts.
Single-phase versions are intended for mains voltages up to around 250 V r.m.s., three-phase versions for mains voltages up to 400 V r.m.s.

The data sheets give a number of carefully chosen preferred stacks, suitable for the most common applications. In addition, our Application Laboratories are fully prepared to design a tailor-made stack for applications not covered by the range of preferred stacks.

CONSTRUCTION

Heat-sinks

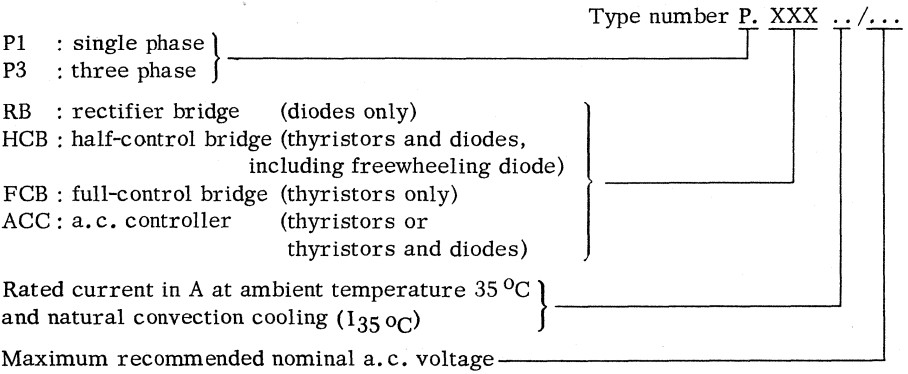
Heavy extruded aluminium heat-sinks are used having a profile suitable for both natural convection cooling and forced air cooling. The design of the power stack system has been based on three different standard lengths, viz. 5, 11 and 23 cm.

End-pieces

The heat-sinks are clamped together between end-pieces, of which there are only two different heights.
The smaller end-piece is for an 11 cm high heat-sink (one heat-sink of 11 cm or two times 5 cm above each other). The longer is for a heat-sink height of 23 cm. When necessary two end-pieces may be mounted on top of each other (mounting holes have been drilled).
End-pieces project roughly 5 cm (2") below the heat-sinks to let the cooling air have access to the power stack when it is mounted on the floor of a cabinet.

TYPE NUMBERING SYSTEM

The stack type number contain information about the basic characteristics of the stacks and are composed as follows:



LIST OF PREFERRED TYPES

P1 RB 20/300	P1 HCB 18/230	P1 FCB 12/230	P1 ACC 14/230
P1 RB 40/270	P1 HCB 37/230	P1 FCB 37/230	P1 ACC 32/230
P1 RB 80/300	P1 HCB 51/230	P1 FCB 51/230	P1 ACC 57/230
P1 RB 185/270	P1 HCB 125/230	P1 FCB 125/230	P1 ACC 138/230
P1 RB 410/270	P1 HCB 238/230	P1 FCB 238/270	P1 ACC 265/270
P3 RB 25/400	P3 HCB 20/400	P3 FCB 15/330	P3 ACC 14/330
P3 RB 46/400	P3 HCB 40/400	P3 FCB 31/400	P3 ACC 35/400
P3 RB 110/400	P3 HCB 100/400	P3 FCB 40/400	P3 ACC 110/400
P3 RB 380/400	P3 HCB 165/400	P3 FCB 81/400	
P3 RB 546/400	P3 HCB 282/400	P3 FCB 165/400	

FREQUENCY

All stacks can be used with mains voltages which have a frequency of 50 Hz or 60 Hz.

CURRENTS

Rated currents

For bridges the rated currents are max. values of the direct current which can be permitted to flow continuously, the conduction angle of the semiconductors being 180^{o} (single phase) or 120^{o} (three phase).
For a.c. controllers the rated currents are maximum r.m.s. values of the line current which can be permitted to flow continuously, the conduction angle of the semiconductors 180^{o}.
The rated current values are based on thermal design consideration, they do not apply to capacitive loads.

Current symbols

$I_{35^{o}C}$: rated current at 35 °C ambient temperature with natural convection cooling
$I_{45^{o}C}$: rated current at 45 °C ambient temperature with natural convection cooling
$I_{5m/s}$: rated current at 35 °C ambient temperature with forced air cooling, air velocity 5 m/s (1000 ft/min).
I_{o} : average output current (for bridges)
I_{L} : r.m.s. value of line current (for a.c. controllers)
I_{SC} : available symmetrical r.m.s. current in one phase under short-circuit conditions

AMBIENT TEMPERATURE

The ambient temperature is defined as the air temperature, measured just below the stack, thermometer shielded from heat radiation.
The air flow through the stack should not be obstructed. Minimum free space above the stack: at least 5 cm when the air can escape to all sides and 8 cm when the air can escape to the front only. See also Cooling Requirements.

TRIGGER INPUT DATA

All power stacks with thyristors have been provided with type TT60 trigger transformers, which are mounted on the stacks.
For reliable triggering of the thyristors it is recommended to drive the trigger transformers by means of the Norbit block UPA61 configurated as free-running oscillator; see data sheets of the TT60 and Application Note 184.

FUSING

To obviate the study of fusing techniques the tables in the data sheets give recommended fuses from two manufacturers, the French firm Ferraz & Cie and the British firm English Electric Ltd. The recommendation of these particular fuses does not disqualify other makes, nor does it mean that fusing is mandatory.
Of the fuse type numbers only that part related to the electrical characteristics is quoted. The full type number also contains mechanical information, and can be obtained from the manufacturer's catalogue.
The recommended fuses are types that protect against short-circuits (i.e. fault currents greater that say 8 times nominal current of the fuse) but not against overload situations (currents between 1 and 8 times nominal current). Protection against overloading may require an overload switch with electro-magnetic and/or thermal cut-out.

The a.c. voltages considered when arriving at these fuse recommendations were the maximum nominal. With considerably lower voltages device protection is more easily obtained. Limitation of I_{SC} then becomes less stringent and in some cases device protection might be obtained from a fuse listed for rated current.
Note that fuses should be ordered directly from the manufacturer's sales organisation.

Fuses for device protection (and installation protection at rated or derated current)

The fuses in the columns "device protection" satisfy the I^2t-ratings of the stack's semiconductors and, in the ideal cases are still large enough to pass the rated current. For some fuses the current I_O or I_L should be limited to an indicated value, which lies below that of the thermally rated current of the stack. For device protection it may also be required that the available short-circuit current I_{SC} should not exceed a stated value.
Users who wish to neglect these limitations can choose the fuse given in the column "rated current".

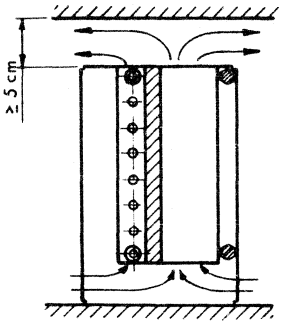
Fuses for installation protection only at rated current

The fuses listed in the columns "rated current" are suited to pass the rated current and protect the installation (stack and load) against short-circuits as described before. However, survival of the semiconductors cannot be guaranteed.
Where no fuse is specified, the fuse quoted in the "device protection" column permits rated current with device protection.

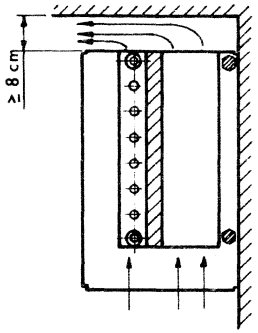
TRANSIENT SUPPRESSION

Refer to Application Information 445 "Transient Suppression Networks for Transformerless Controlled Rectifier Systems".

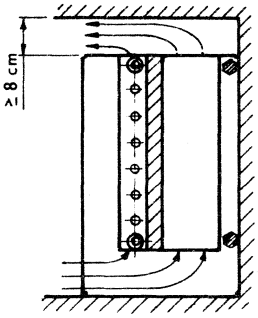
COOLING REQUIREMENTS



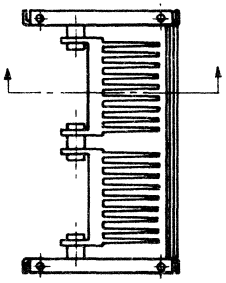
(a) Stack on a horizontal (unperforated) base. Cooling air has access from front and back. Cooling air can flow away to front and back: 5 cm minimum clearance above stack.



Stack with back to vertical wall. Cooling air has access from below. Air cannot escape to the rear:
8 cm minimum clearance above stack.



Stack on horizontal base, back against vertical wall.
Space between end-pieces, where they project below the heat-sinks, provides sufficient access for the air. As in case (b) a clearance of at least 8 cm is required above the stack because the air cannot escape to the rear.



Note
The air velocity of 5 m/s is defined as the average air velocity assuming the stack to be placed in an air channel whose cross-section is large compared with that of the stack.

SINGLE PHASE DIODE BRIDGES

type number	Fig.	$I_{5m/s}$ (A)	$I_{35\,^{o}C}$ (A)	$I_{45\,^{o}C}$ (A)	cat. No.
P1 RB20/300	1	–	20	20	9331 435 30112
P1 RB40/270	2	–	40	40	9331 435 40112
P1 RB80/300	2	–	80	74	9331 435 50112
P1 RB185/270	3		185	175	9331 435 60112
P1 RB410/270 [1]	4	640	410	380	9331 435 70112

Two diodes normal polarity and two diodes reverse polarity. Rated currents are quoted in terms of continuous output currents (average value) at a conduction angle of 180° into a resistive or inductive load.
[1]) Diodes mounted with heat-sink compound (Dow Corning 340).

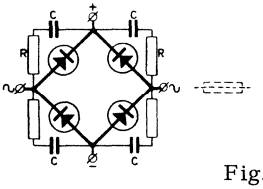
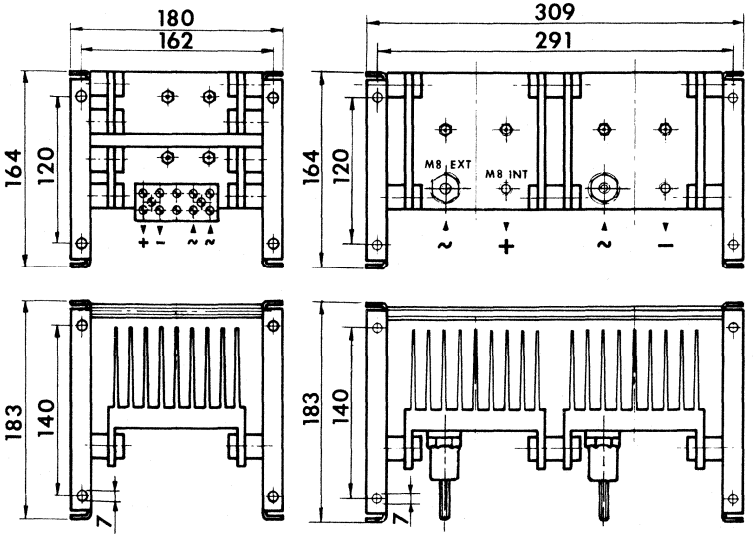


Fig. 1

Fig. 2



recommended line fuse			
Ferraz		English Electric	
device protection	rated current	device protection	rated current
UREcaps Δ 500-16 ($I_o \leq 14.5A$)	UREcaps 500-25	GSG1000-16 ($I_o \leq 14.5A$)	GSG1000-25
UREcaps 500-50	⟵	GSG1000-45	⟵
UREcaps 500-63 ($I_o \leq 57A$)	SRB500-100	GSG1000-110 GSG1000-85	⟵
SRB500-160 ($I_o \leq 144A$)	SRB500-200	GSG1000-200	⟵
SRB500-400 ($I_o \leq 360A$)	URC300-800 URD500-500 SRB500-450	GSG1000-350 ($I_o \leq 315A$)	2xGS1000-400 ▲ GS1000-500

▲) in parallel
Δ) without signalization

Fig. 3

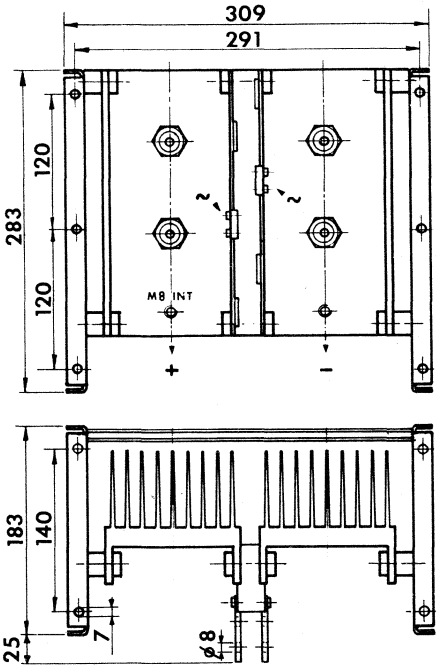
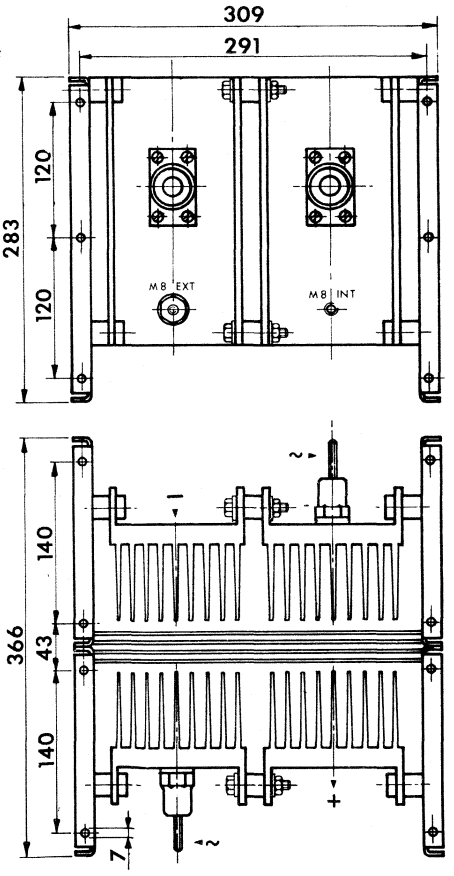


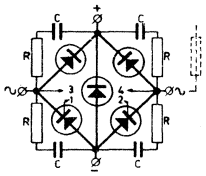
Fig. 4



SINGLE PHASE HALF-CONTROL BRIDGES

type number	Fig.	$I_{5m/s}$ (A)	$I_{35\,^{o}C}$ (A)	$I_{45\,^{o}C}$ (A)	cat. No.
P1 HCB18/230	1	-	18.2	16.4	9331 435 80112
P1 HCB37/230	2	-	37.5	34	9331 435 90112
P1 HCB51/230	3	-	51	50	9331 436 00112
P1 HCB125/230	4	-	125	114	9331 436 10112
P1 HCB238/270 1)	4	400	238	206	9331 436 20112

All diodes normal polarity. Rated currents are quoted in terms of continuous output currents (average value) at a conduction angle of 180° into a resistive or inductive load.
1) Diodes and thyristors mounted with heat-sink compound (Dow Corning 340)



TT60

Fig. 1

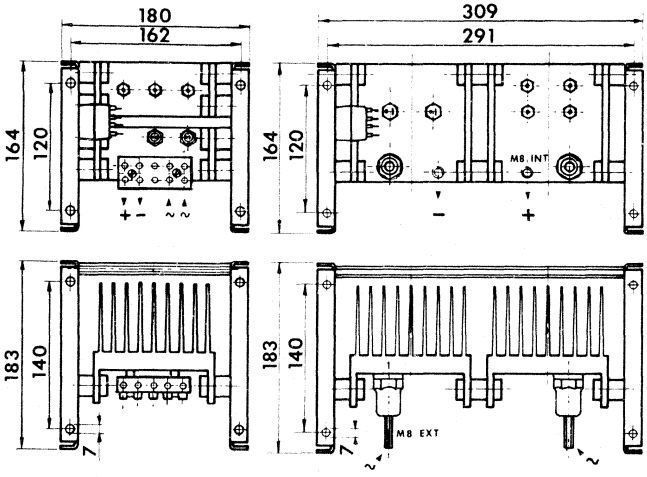


Fig. 2

recommended line fuse			
Ferraz		English Electric	
device protection	rated current	device protection	rated current
UREcaps 500-16 ($I_O \leq 14.5A$)	UREcaps 500-20	GSG1000-16 ($I_O \leq 14.5A$)	GSG1000-25
UREcaps 500-50	←	GSG1000-45	←
UREcaps 500-40		GSG1000-40	
UREcaps 500-63	←	GSG1000-55	←
SRB500-160	←	GSG1000-150	←
URE500-125			
SRB500-400 ($I_O \leq 360$ A)	SRB500-450	2xGSG1000-235▲	
SRB500-315	←	GSG1000-300	←
SRB500-250		GSG1000-235	

▲) in parallel

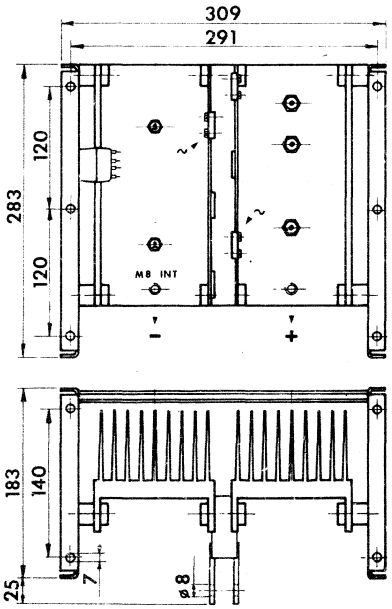


Fig. 3

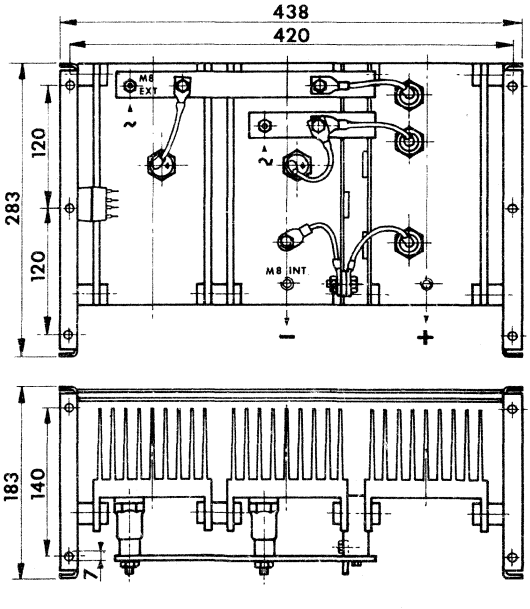


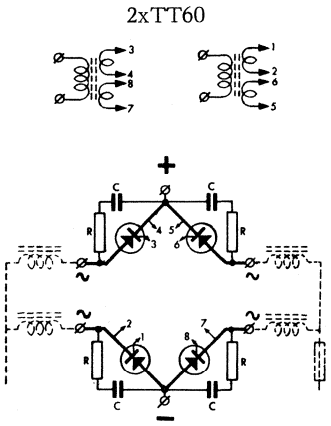
Fig. 4

SINGLE PHASE FULL-CONTROL BRIDGES

type number	Fig.	$I_{5m/s}$ (A)	$I_{35\,^{\circ}C}$ (A)	$I_{45\,^{\circ}C}$ (A)	cat. No.
P1 FCB12/230	1	-	12.8	12.8	9331 436 30112
P1 FCB37/230	1	-	37.5	34	9331 436 40112
P1 FCB51/230	2	-	51	50	9331 436 50112
P1 FCB125/230	3	-	125	114	9331 436 60112
P1 FCB238/270 [1]	3	400	238	206	9331 436 70112

Rated currents are quoted in terms of continuous output currents (average value) at a conduction angle of 180° into a resistive or inductive load.

[1]) Thyristors mounted with heat-sink compound (Dow Corning 340).



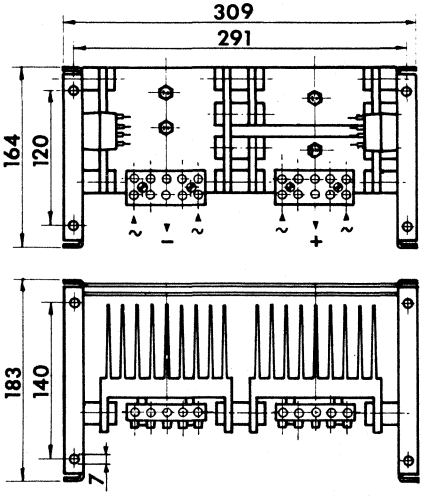


Fig. 1

recommended line fuse			
Ferraz		English Electric	
device protection	rated current	device protection	rated current
UREcaps△500-12 ($I_o \leq 10.5A$)	UREcaps 500-16	GSG1000-16	⟵
UREcaps 500-50	⟵	GSG1000-45	⟵
UREcaps 500-40		GSG1000-40	
UREcaps 500-63	⟵	GSG1000-55	⟵
SRB500-160		GSG1000-150	
SRB500-125			
SRB500-450	⟵	2xGSG1000-235▲	⟵
SRB500-315		GSG1000-300	
SRB500250		GSG1000-235	

△) without signalization
▲) in parallel.

Fig. 2

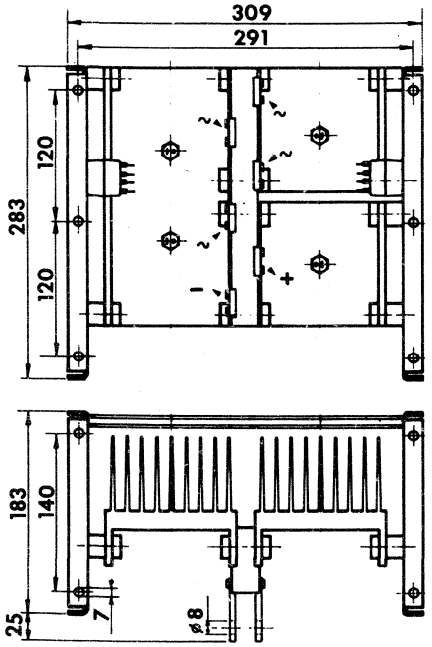
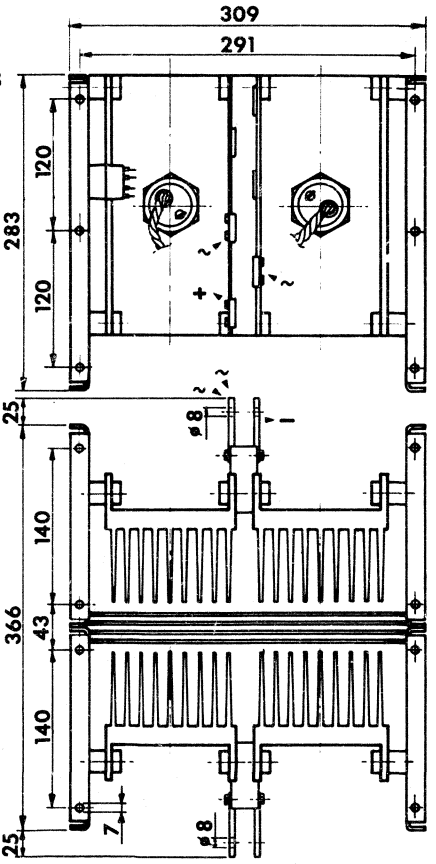


Fig. 3

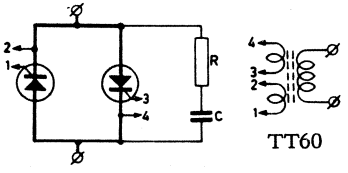


SINGLE PHASE A.C. CONTROLLERS

type number	Fig.	$I_{5m/s}$ (A)	$I_{35\,^oC}$ (A)	$I_{45\,^oC}$ (A)	cat. No.
P1 ACC14/230	1	-	14	14	9331 436 80112
P1 ACC32/230	1	-	32	29	9331 436 90112
P1 ACC57/230	2	-	57	57	9331 437 00112
P1 ACC138/230	3	160	138	127	9331 437 10112
P1 ACC265/270 1)	3	444	265	229	9331 437 20112

Rated currents are quoted in terms of continuous a.c. (r.m.s. value) at a conduction angle of 180° into a resistive or inductive load.

1).Thyristors mounted with heat-sink compound (Dow Corning 340)



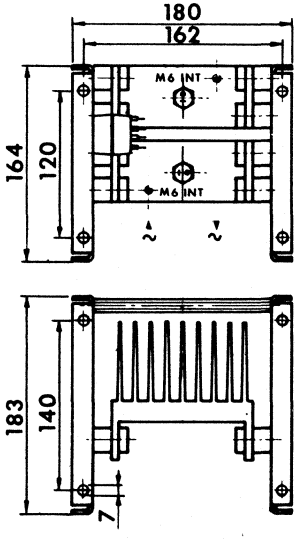


Fig. 1

recommended line fuse			
Ferraz		English Electric	
device protection 2)	rated current	device protection 2)	rated current
URECaps 500-10 or URECaps Δ 500-12	URECaps 500-16	GSG1000-16	<——
URECaps 500-25	URECaps 500-32	GSG1000-30	GSG1000-35 <——
URECaps 500-63	<——	GSG1000-55 or GSG1000-75	<——
SRB500-160	<——	GSG1000-175	<——
SRB500-125		GSG1000-150	
SRB500-450	<——	2xGSG1000-235▲	<——
SRB500-315		GSG1000-300	
SRB500-250		GSG1000-235	

2) Line current $I_L \leq$ fuse rating
Δ) without signalization
▲) in parallel.

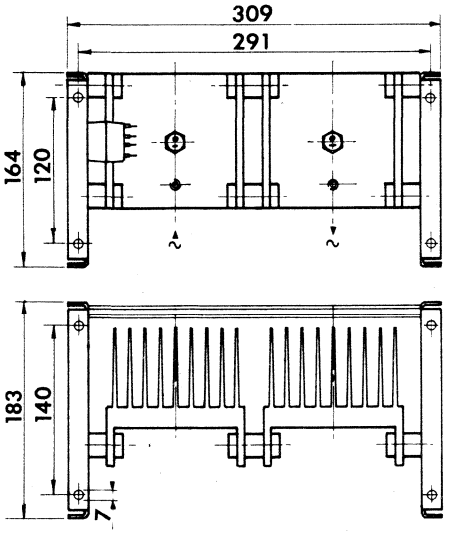


Fig. 2

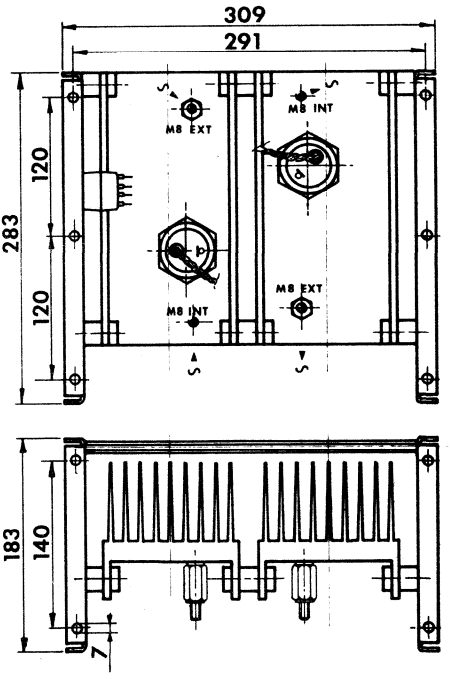
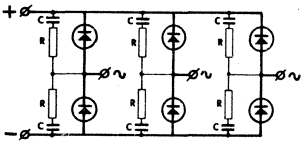


Fig. 3

THREE PHASE DIODE BRIDGES

type number	Fig.	$I_{5m/s}$ (A)	$I_{35\,^{o}C}$ (A)	$I_{45\,^{o}C}$ (A)	cat. No.
P3 RB25/400	1	–	25.5	25.5	9331 437 30112
P3 RB46/400	2	–	46	46	9331 437 40112
P3 RB110/400	3	–	110	105	9331 437 50112
P3 RB210/400	3	300	210	198	9331 437 60112
P3 RB380/400 1)	4	720	380	350	9331 437 70112
P3 RB546/400 1)	5	870	546	510	9331 437 80112

Three diodes normal polarity and three reverse polarity. Rated currents are quoted in terms of continuous output currents (average value) at a conduction angle of 120° into a resistive or inductive load.
1) Diodes mounted with heat-sink compound (Dow Corning 340).



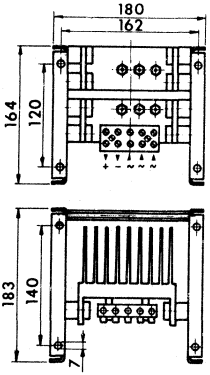


Fig. 1

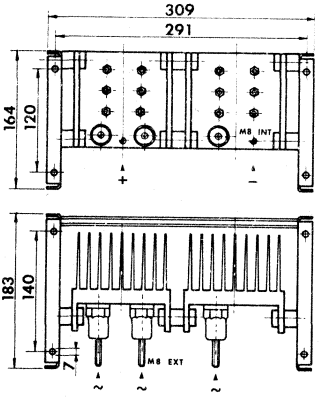


Fig. 2

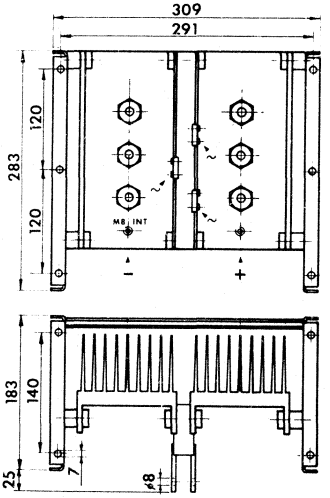


Fig. 3

recommended line fuse			
Ferraz		English Electric	
device protection	rated current	device protection	rated current
URECaps 500-12 ($I_O \leq 14.5A$)	URECaps 500-25	GSG1000-16 ($I_O \leq 19A$)	GSG1000-25
URECaps 500-20 ($I_O \leq 24.5A$)	URECaps 500-40	GSG1000-25 ($I_O \leq 30.5A$) or GSG1000-30 ($I_O \leq 37A$) [2]	GSG1000-40
URECaps 500-63 ($I_O \leq 77A$)	URECaps 500-100	GSG1000-75 ($I_O \leq 92A$)	GSG1000-110
		or GSG1000-85 ($I_O \leq 105A$) [3]	GSG1000-85
URE500-125 ($I_O \leq 153A$)	SRB500-250	GSG1000-110 ($I_O \leq 135A$)	GSG1000-300
	SRB500-200	or GSG1000-150 ($I_O \leq 184A$) [4]	GSG1000-175
	SRB500-160	or GSG1000-175 ($I_O \leq 214A$) [5]	
SRB500-250 ($I_O \leq 306A$) or SRB500-315 ($I_O \leq 386A$) [6]	URC500-630 URC500-315	GSG1000-300 ($I_O \leq 368A$)	2x GS1000-300▲
		or GSG1000-325 ($I_O \leq 398A$) [6]	GSG1000-325
		GSG1000-300	<——
no recommendation	2xURC500-400 [7]	no recommendation	2xGS1000-400▲
	SRB500-450		GS1000-500

Device protection if [2] $I_{SC} \leq 8$ kA, [3] $I_{SC} \leq 20$ kA, [4] $I_{SC} \leq 10$ kA, [5] $I_{SC} \leq 2$ kA, [6] $I_{SC} \leq 9$ kA, [7] $I_{SC} \leq 10$ kA.

▲) in parallel.

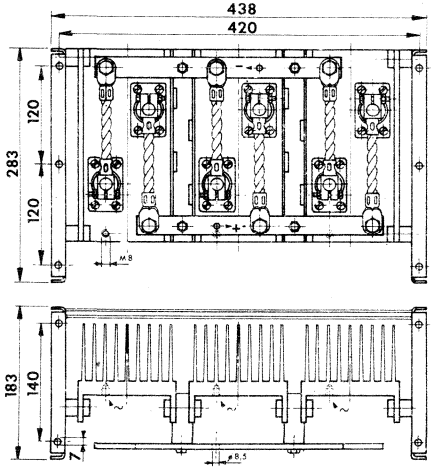


Fig. 4

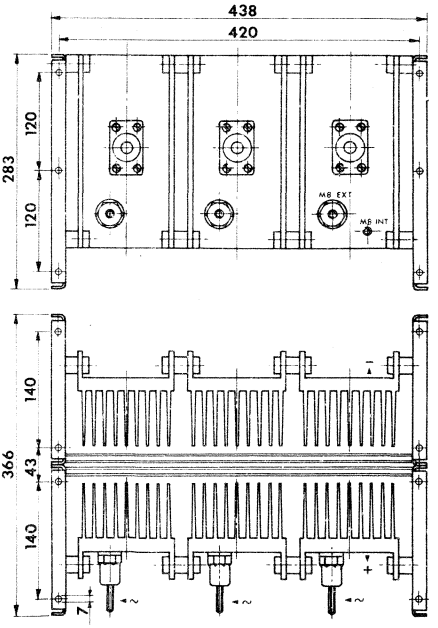
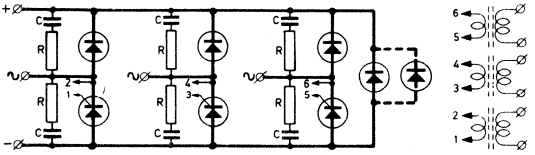


Fig. 5

THREE PHASE HALF-CONTROL BRIDGES

type number	Fig.	$I_{5m/s}$ (A)	$I_{35\,^oC}$ (A)	$I_{45\,^oC}$ (A)	cat. No.
P3 HCB20/400	1	–	20	17.4	9331 437 90112
P3 HCB40/400	2	–	40	37.5	9331 438 00112
P3 HCB100/400	2	–	100	90	9331 438 10112
P3 HCB165/400	3	–	165	150	9331 438 20112
P3 HCB282/400 1)	3	550	282	260	9331 438 30112

All diodes normal polarity. Current ratings are quoted in terms of continuous output currents (average value) at a conduction angle of 120^o into an inductive or resistive load.
1) Semiconductors mounted with heat-sink compound (Dow Corning 340)



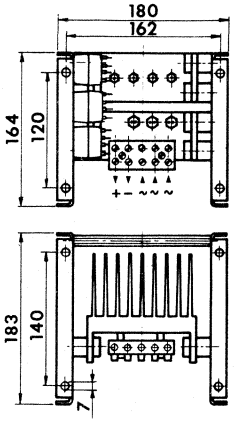


Fig. 1

recommended line fuse			
Ferraz		English Electric	
device protection	rated current	device protection	rated current
URE caps 500-12 ($I_O \leq 14.7A$)	URE caps 500-20	GSG1000-16 ($I_O \leq 19.5A$)	GSG1000-25
	URE caps 500-16	GSG1000-16	<——
URE caps 500-20 ($I_O \leq 24.5A$)	URE caps 500-40 URE caps 500-32	GSG1000-30 [2] ($I_O \leq 37A$) or GSG1000-25 ($I_O \leq 30.5A$)	GSG1000-35
URE caps 500-63 ($I_O \leq 77A$)	URE caps 500-100	GSG1000-85 [4] or GSG1000-75 ($I_O \leq 92A$)	GSG1000-85
	URE caps 500-80	GSG1000-75	<——
SRB500-125 ($I_O \leq 153A$)	SRB500-160	GSG1000-150 [3] or GSG1000-110 ($I_O \leq 135A$)	GSG1000-150
SRB500-125	<——		
SRB500-315 ($I_O \leq 386A$)	SRB500-450	GSG1000-300 ($I_O \leq 367A$) or GSG1000-325 [4] ($I_O \leq 398A$)	GSG1000-500
SRB500-250	<——	GSG1000-235	<——

Device protection if [2] $I_{SC} \leq 4$ kA, [3] $I_{SC} \leq 10$ kA, [4] $I_{SC} \leq 14$ kA.

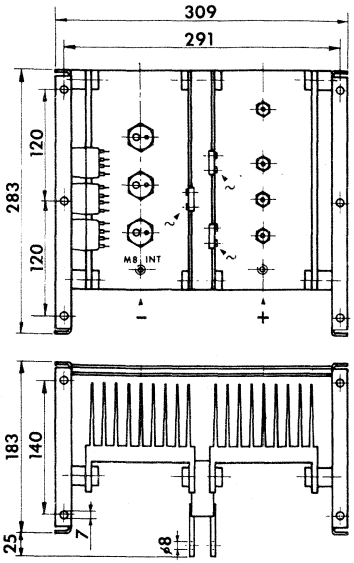


Fig. 2

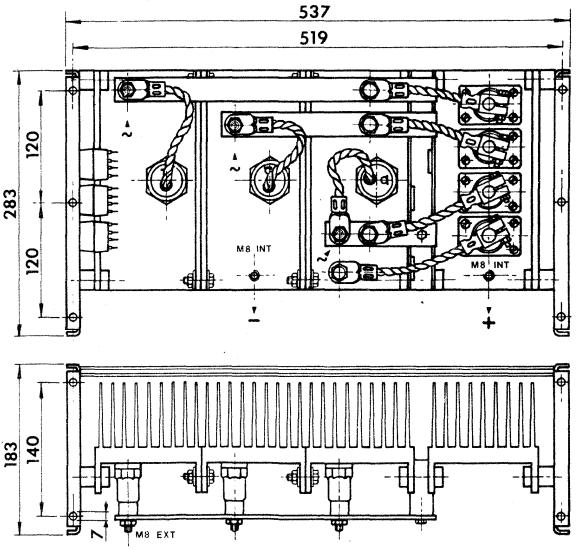


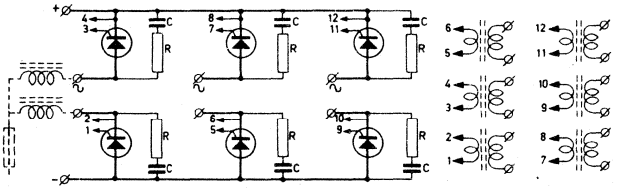
Fig. 3

THREE PHASE FULL-CONTROL BRIDGES

type number	Fig.	$I_{5m/s}$ (A)	$I_{35\,^{o}C}$ (A)	$I_{45\,^{o}C}$ (A)	cat. No.
P3 FCB15/330	1	–	15	15	9331 438 40112
P3 FCB31/400	2	–	31	28	9331 438 50112
P3 FCB40/400	2	–	40	37	9331 438 60112
P3 FCB81/400	2	–	81	72	9331 438 70112
P3 FCB165/400	3	–	165	150	9331 438 80112
P3 FCB327/400 [1]	3	550	327	288	9331 438 90112

Rated currents are quoted in terms of continuous output current (average value) at a conduction angle of 120° into resistive or inductive load.

1) Thyristors mounted with heat-sink compound (Dow Corning 340).



6xTT60

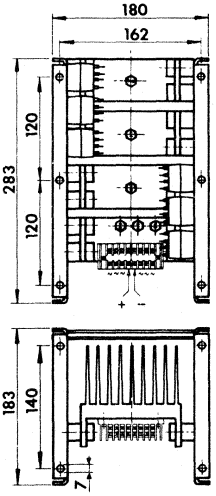


Fig.1

recommended line fuse			
Ferraz		English Electric	
device protection	rated current	device protection	rated current
URE caps 500-8 ($I_O \leq 10A$) or URE caps 500-10 ($I_O \leq 12A$)	URE caps 500-16	GS1000-10 ($I_O \leq 12A$) or GS1000-15 [2]	GSG1000-16
URE caps 500-16 ($I_O \leq 20A$) or URE caps Δ 500-20 ($I_O \leq 24.5A$)	URE caps 500-25	GSG1000-16 ($I_O \leq 20A$) or GSG1000-25 [3]	GSG1000-25
URE caps 500-20 ($I_O \leq 24.5A$)	URE caps 500-40	GSG1000-25 ($I_O \leq 30A$) or GSG1000-30 [4] ($I_O \leq 37A$)	GSG1000-35
	URE caps 500-32		GSG1000-30
URE caps 500-80	<——	GSG1000-75	<——
URE caps 500-63			
SRB500-125 ($I_O \leq 153A$)	SRB500-160	GSG1000-110 ($I_O \leq 135A$) or GSG1000-150 [5]	GSG1000-150
SRB500-450	<——	2xGSG1000-235▲	<——
SRB500-315		GSG1000-300	
SRB500-250		GSG1000-235	

Device protection if [2] $I_{SC} \leq 1$ kA, [3] $I_{SC} \leq 450$ A, [4] $I_{SC} \leq 4.5$ kA, [5] $I_{SC} \leq 6.5$ kA,
Δ) without signalization
▲) in parallel.

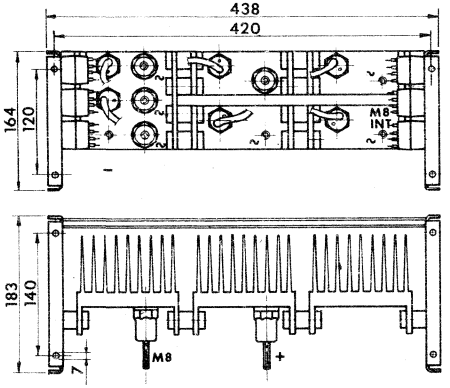


Fig.2

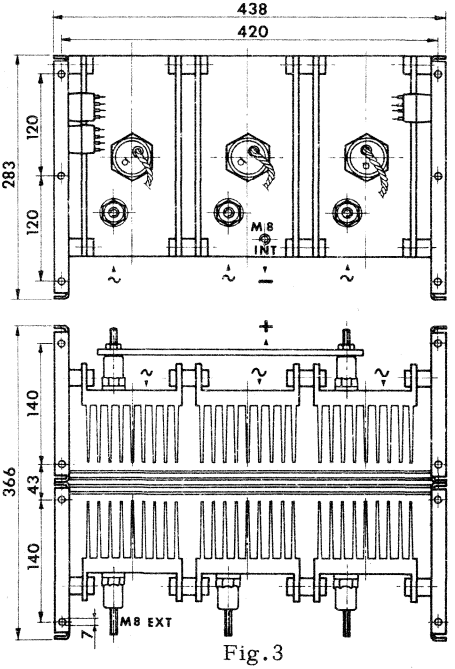


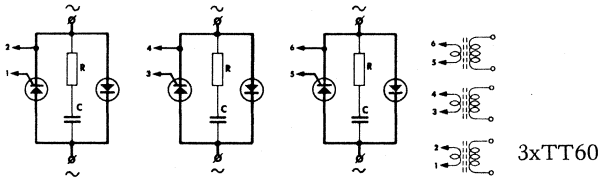
Fig.3

THREE PHASE A.C. CONTROLLERS

type number	Fig.	$I_{5m/s}$ (A)	$I_{35\,^{o}C}$ (A)	$I_{45\,^{o}C}$ (A)	cat. No.
P3 ACC14/330	1	–	14	13	9331 439 00112
P3 ACC35/400	2	–	35	32	9331 439 10112
P3 ACC110/400	3	160	110	100	9331 439 20112
P3 ACC265/400 [1])	4	400	265	230	9331 439 30112

All diodes are of normal polarity. Rated currents are quoted in terms of continuous a.c. (r.m.s. value) at a conduction angle of 180° into a resistive or inductive load.

[1]) Semiconductors mounted with heat-sink compound (Dow Corning 340).



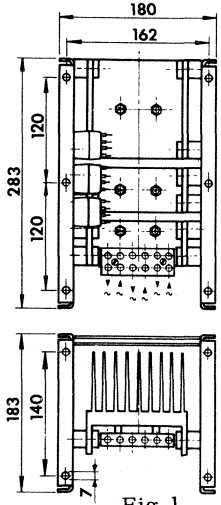


Fig.1

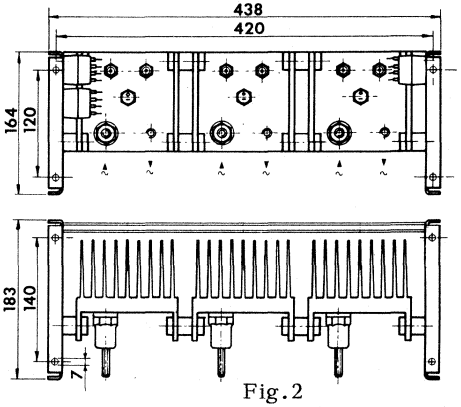


Fig.2

recommended line fuse			
Ferraz		English Electric	
device protection [2]	rated current	device protection [2]	rated current
UREcaps 500-10	UREcaps 500-16	GS1000-10 or GS1000-15 ($I_{SC} \leq 1$ kA)	GSG1000-16
UREcaps 500-20	UREcaps 500-40	GSG1000-30 ($I_{SC} \leq 4.5$ kA) or GSG1000-25	GSG1000-35
	UREcaps 500-32		
SRB500-125	SRB500-160	GSG1000-150 ($I_{SC} \leq 6.5$ kA) or GSG1000-110	GSG1000-175
SRB500-125	⟵	GSG1000-110	⟵
SRB500-100			
SRB500-315	SRB500-450	2xGSG1000-175▲ or GSG1000-325 ($I_{SC} \leq 10$ kA) or GSG1000-300	GS1000-500
SRB500-315	⟵	GSG1000-300	⟵
SRB500-250		GSG1000-235	

[2]) Line current ≤ fuse rating.
▲) in parallel.

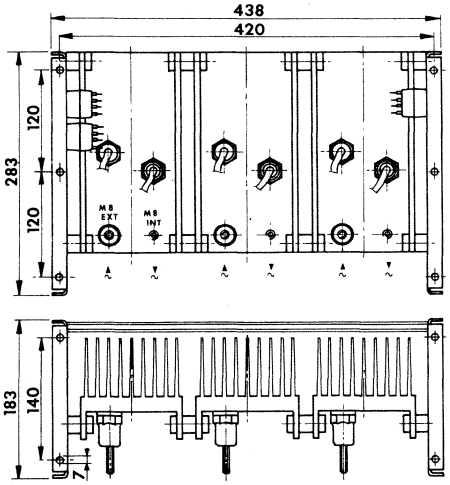


Fig.3

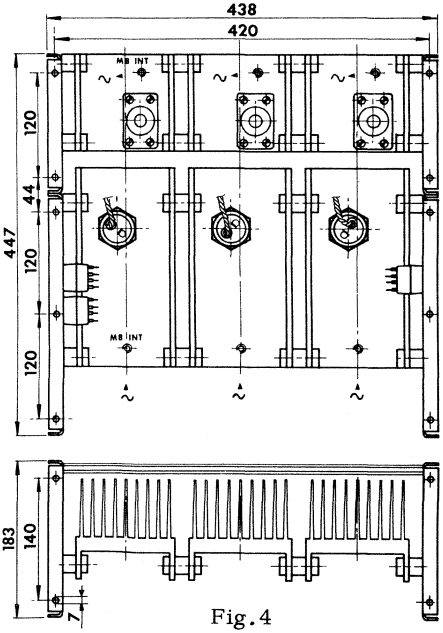
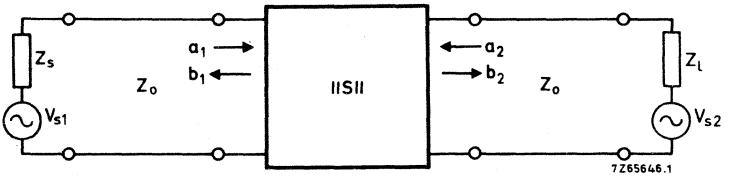


Fig.4

Hybrid integrated circuits

SCATTERING PARAMETERS

In distinction to the conventional h, y and z-parameters, s-parameters relate to travelling wave conditions. The figure below shows a two-port network with the incident and reflected waves a_1, b_1, a_2 and b_2.



$$a_1 = \frac{V_{i1}}{\sqrt{Z_o}} \qquad a_2 = \frac{V_{i2}}{\sqrt{Z_o}} \qquad 1)$$

$$b_1 = \frac{V_{r1}}{\sqrt{Z_o}} \qquad b_2 = \frac{V_{r2}}{\sqrt{Z_o}}$$

Z_o = characteristic impedance of the transmission line in which the two-port is connected.

V_i = incident voltage

V_r = reflected (generated) voltage

The four-pole equations for s-parameters are:

$$b_1 = s_{11}a_1 + s_{12}a_2$$
$$b_2 = s_{21}a_1 + s_{22}a_2$$

Using the subscripts i for 11, r for 12, f for 21 and o for 22, it follows that:

$$s_i = s_{11} = \left.\frac{b_1}{a_1}\right|_{a_2 = 0}$$
$$s_r = s_{12} = \left.\frac{b_1}{a_2}\right|_{a_1 = 0}$$
$$s_f = s_{21} = \left.\frac{b_2}{a_1}\right|_{a_2 = 0}$$
$$s_o = s_{22} = \left.\frac{b_2}{a_2}\right|_{a_1 = 0}$$

1) The squares of these quantities have the dimension of power.

The s-parameters can be named and expressed as follows:

$s_i = s_{11}$ = Input reflection coefficient.
The complex ratio of the reflected wave and the incident wave at the input, under the conditions $Z_l = Z_o$ and $V_{s2} = 0$.

$s_r = s_{12}$ = Reverse transmission coefficient.
The complex ratio of the generated wave at the input and the incident wave at the output, under the conditions $Z_s = Z_o$ and $V_{s1} = 0$.

$s_f = s_{21}$ = Forward transmission coefficient.
The complex ratio of the generated wave at the output and the incident wave at the input, under the conditions $Z_l = Z_o$ and $V_{s2} = 0$

$s_o = s_{22}$ = Output reflection coefficient.
The complex ratio of the reflected wave and the incident wave at the output, under the conditions $Z_s = Z_o$ and $V_{s1} = 0$.

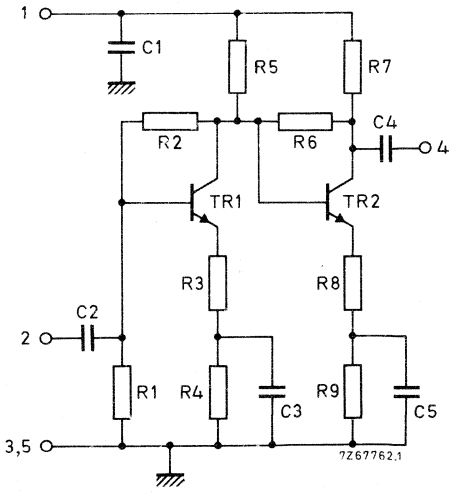
HYBRID VHF/UHF WIDE-BAND AMPLIFIER

Two-stage wide-band amplifier in the hybrid technique, designed for use as distribution amplifier in MATV and CATV systems and as general-purpose amplifier for v.h.f. and u.h.f. applications.

QUICK REFERENCE DATA				
Frequency range	f		40 to 860	MHz
Source and load (characteristic) impedance	$R_S = R_\ell = Z_O$		75	Ω
Transducer gain	$G_{tr} = \lvert s_f \rvert^2$	typ.	15	dB
Flatness of frequency response	$\pm\Delta \lvert s_f \rvert^2$	typ.	0,3	dB
Output voltage at −60 dB intermodulation distortion (DIN45004, 3-tone)	$V_{o(rms)}$	>	103	dBμV
Noise figure	F	typ.	7	dB
D.C. supply voltage	V_B	=	24	V ±10%
Operating ambient temperature	T_{amb}		−20 to +70	°C

ENCAPSULATION 5-lead, plastic case on metal base, see MECHANICAL DATA

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Operating ambient temperature	T_{amb}		−20 to +70	°C
Operating mounting-base temperature	T_{mb}	max.	100	°C
Storage temperature	T_{stg}		−40 to +125	°C
D.C. supply voltage	V_B	max.	28	V
Peak voltages on pins 2 and 4	V_{2M}, V_{4M}	max.	28	V
	$-V_{2M}$, $-V_{4M}$	max.	10	V
Peak incident powers on pins 2 and 4	P_{I2M}, P_{I4M}	max.	100	mW

CHARACTERISTICS

Measuring conditions

Ambient temperature	T_{amb}	=	25	°C
D.C. supply voltage	V_B	=	24	V
Source impedance and load impedance	R_s, R_ℓ	=	75	Ω
Characteristic impedance of h.f. connections	Z_o	=	75	Ω
Frequency range	f	=	40 to 860	MHz

Performance

Supply current	I_B	typ.	60	mA
Transducer gain	$G_{tr} = \lvert s_f \rvert^2$		14 to 16	dB
		typ.	15	dB
Flatness of frequency response	$\pm\Delta \lvert s_f \rvert^2$	typ.	0,3	dB
		<	0,5	dB
Individual maximum v.s.w.r.				
input	$VSWR_{(i)}$	typ.	1,7	[1]
output	$VSWR_{(o)}$	typ.	1,7	[1]
Back attenuation				
f = 100 MHz	$\lvert s_r \rvert^2$	typ.	31	dB
f = 860 MHz	$\lvert s_r \rvert^2$	typ.	25	dB
Output voltage at −60 dB intermodulation distortion (DIN45004, par. 6.3: 3-tone)	$V_{o(rms)}$	>	103	dBμV
		typ.	105	dBμV
Noise figure	F	typ.	7	dB

s-parameters:		
	$s_f = s_{21}$	$s_i = s_{11}$
	$s_r = s_{12}$	$s_o = s_{22}$

[1]) Highest value, for a sample, occurring in the frequency range.

OPERATING CONDITIONS

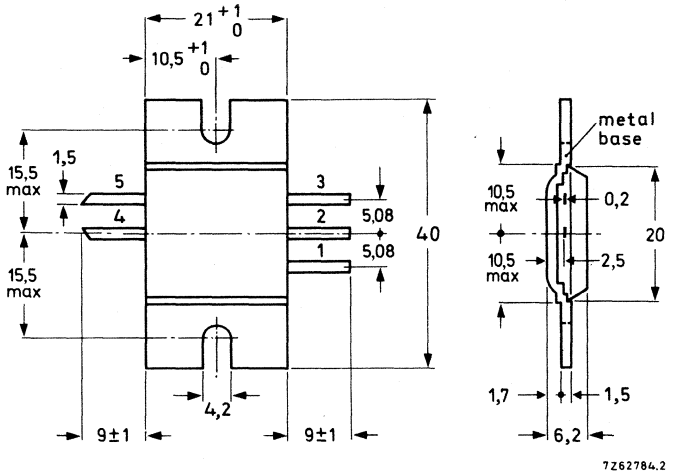
Ambient temperature range	T_{amb}		−20 to +70	°C
D.C. supply voltage	V_B	=	24	V ±10%
Frequency range	f		40 to 860	MHz
Source impedance and load impedance	R_S, R_ℓ	=	75	Ω

MECHANICAL DATA

Dimensions in mm

Encapsulation

The device is mounted on a metal mounting base and sealed in plastic.



Terminal connections

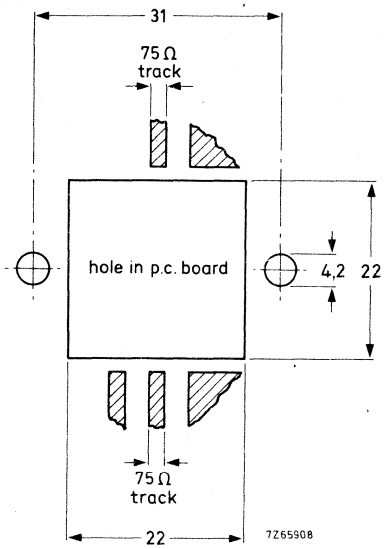
1	= Supply (+)
2	= Input
3 and 5	= Common (internally connected to metal base)
4	= Output

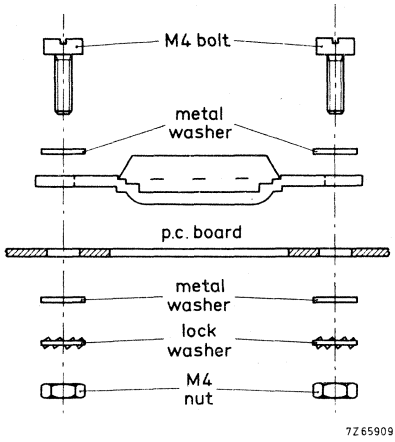
Soldering recommendations

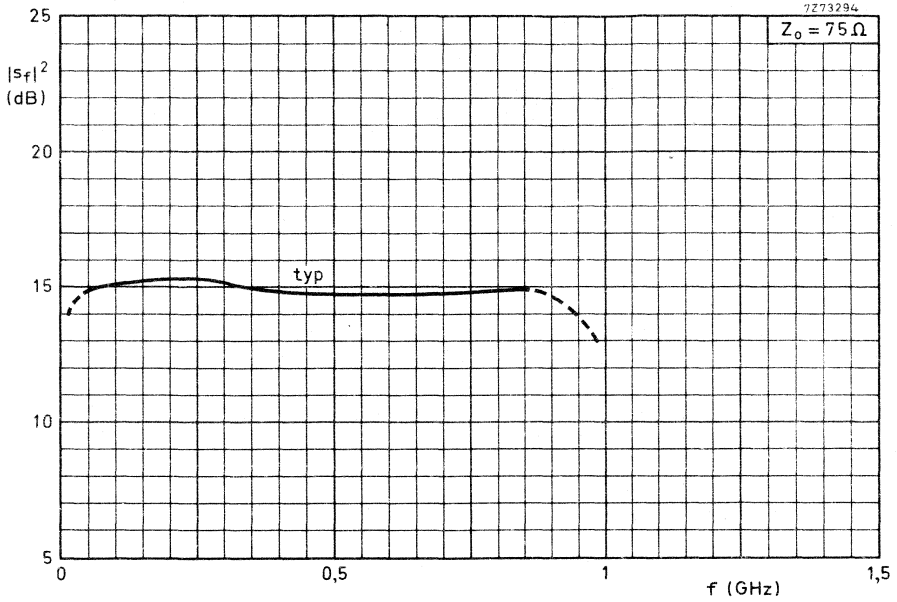
Maximum contact time for a soldering-iron temperature of 260 °C 5 s

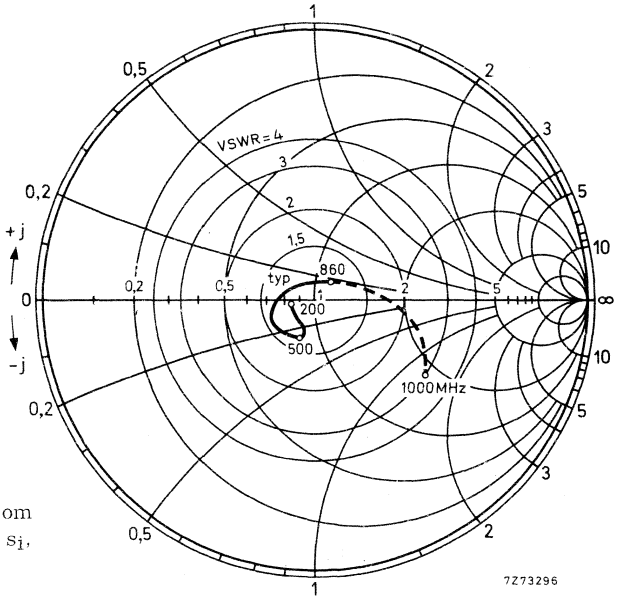
Mounting recommendations

The module should preferably be mounted on a double-sided printed-circuit board, see the examples shown below. Input and output should be connected to 75 Ω tracks.

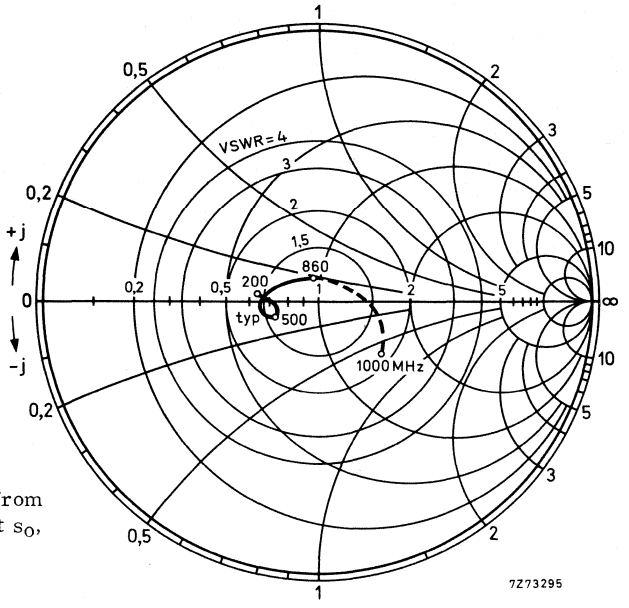








Input impedance derived from input reflection coefficient s_i, co-ordinates in ohm x 75



Output impedance derived from output reflection coefficient s_o, co-ordinates in ohm x 75

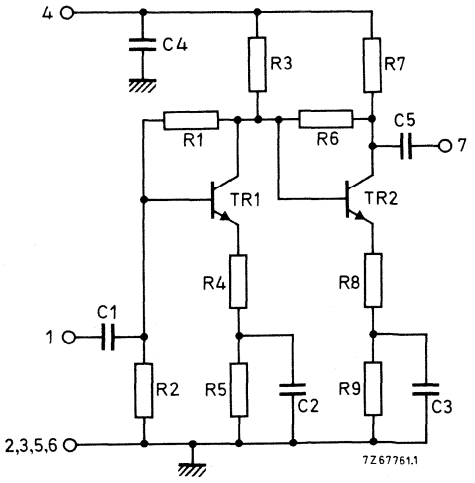
HYBRID VHF/UHF WIDE-BAND AMPLIFIER

Two-stage wide-band amplifier in the hybrid technique, designed for use in mast-head booster amplifiers, as pre-amplifier in MATV systems, and as general-purpose amplifier for v.h.f. and u.h.f. applications

QUICK REFERENCE DATA				
Frequency range	f		40 to 860	MHz
Source and load (characteristic) impedance	$R_S = R_\ell = Z_o$	=	75	Ω
Transducer gain	$G_{tr} = \|s_f\|^2$	typ.	15,5	dB
Flatness of frequency response	$\pm\Delta\|s_f\|^2$	typ.	1	dB
Output voltage at −60 dB intermodulation distortion (DIN45004, 3-tone)	$V_{o(rms)}$	>	92	dBμV
Noise figure	F	typ.	5,5	dB
D.C. supply voltage	V_B	=	24	V ± 10%
Operating ambient temperature	T_{amb}	−20 to +70		°C

ENCAPSULATION 7-pin, in-line, resin-coated body, see MECHANICAL DATA

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Operating ambient temperature	T_{amb}		−20 to +70	°C
Storage temperature	T_{stg}		−40 to +125	°C
D.C. supply voltage	V_B	max.	28	V
Peak voltages on pins 1 and 7	V_{1M}, V_{7M}	max.	28	V
	$-V_{1M}$, $-V_{7M}$	max.	10	V
Peak incident powers on pins 1 and 7	P_{I1M}, P_{I7M}	max.	100	mW

CHARACTERISTICS

Measuring conditions

Ambient temperature	T_{amb}	=	25	°C
D.C. supply voltage	V_B	=	24	V
Source impedance and load impedance	R_S, R_ℓ	=	75	Ω
Characteristic impedance of h.f. connections	Z_o	=	75	Ω
Frequency range	f		40 to 860	MHz

Performance

Supply current	I_B	typ.	23	mA
Transducer gain	$G_{tr} = \lvert s_f \rvert^2$		13 to 18	dB
		typ.	15,5	dB
Flatness of frequency response	$\pm\Delta \lvert s_f \rvert^2$	typ.	1	dB
Individual maximum v.s.w.r.				
input	$VSWR_{(i)}$	typ.	2,2	[1]
output	$VSWR_{(o)}$	typ.	2,5	[1]
Back attenuation				
f = 100 MHz	$\lvert s_r \rvert^2$	typ.	30	dB
f = 860 MHz	$\lvert s_r \rvert^2$	typ.	24	dB
Output voltage at −60 dB intermodulation distortion (DIN45004, par. 6.3: 3-tone)	$V_{o(rms)}$	>	92	dBμV
		typ.	94	dBμV
Noise figure	F	typ.	5,5	dB

s-parameters:	$s_f = s_{21}$	$s_i = s_{11}$
	$s_r = s_{12}$	$s_o = s_{22}$

[1]) Highest value, for a sample, occurring in the frequency range.

OPERATING CONDITIONS

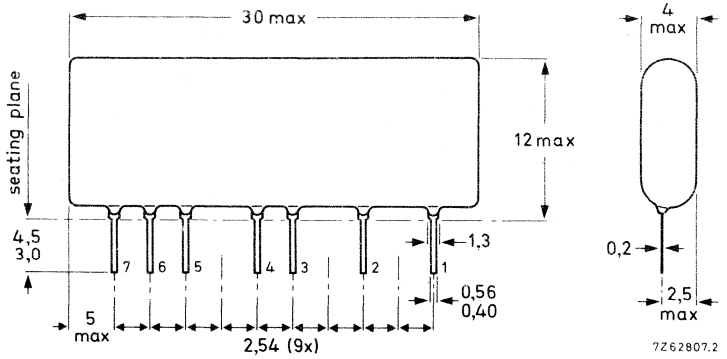
Ambient temperature range	T_{amb}		−20 to +70	°C
D.C. supply voltage	V_B	=	24	V ±10%
Frequency range	f		40 to 860	MHz
Source impedance and load impedance	R_S, R_ℓ	=	75	Ω

MECHANICAL DATA

Dimensions in mm

Encapsulation

The device is resin coated.



Terminal connections

1	= Input
2, 3, 5, 6	= Common
4	= Supply (+)
7	= Output

Soldering recommendations

Hand soldering

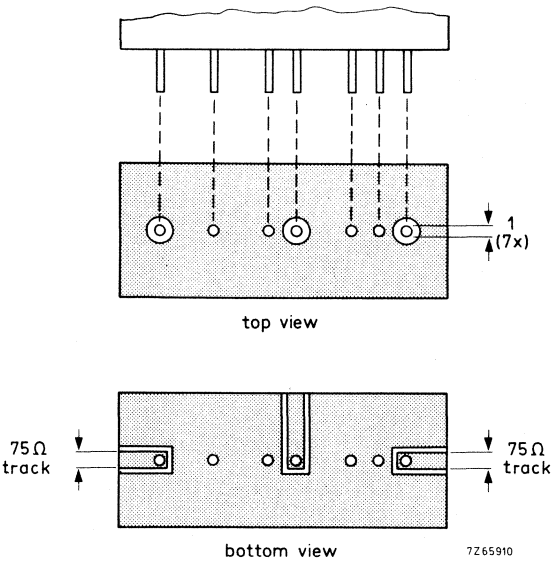
Maximum contact time for a soldering-iron temperature of 260 °C; up to seating plane: 5 s

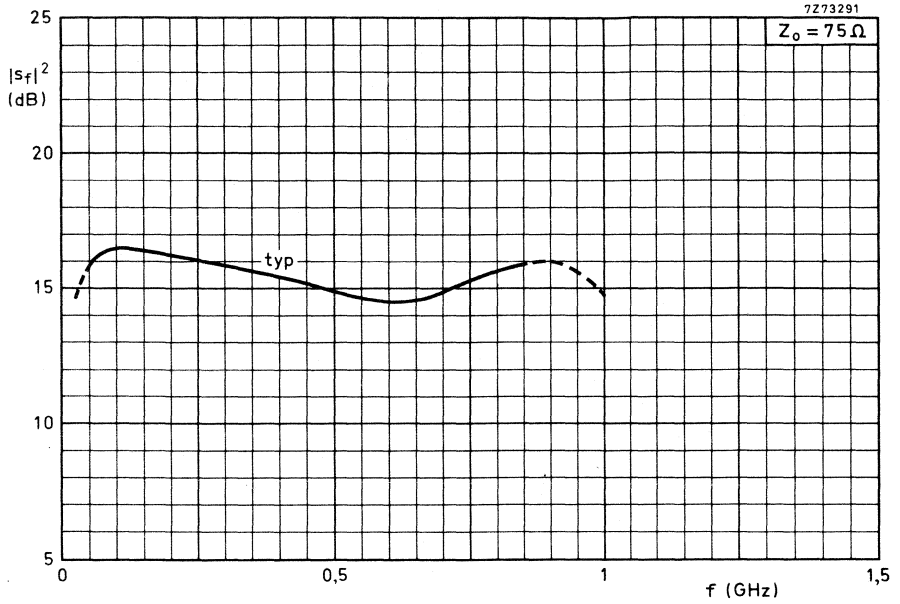
Dip or wave soldering

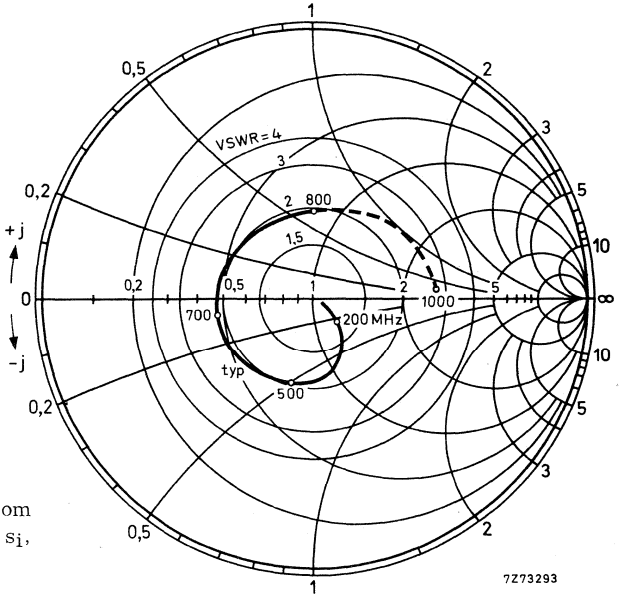
260 °C is the maximum permissible temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted against the printed-circuit board, but the temperature of the device must not exceed 125 °C. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature below the allowable limit.

Mounting recommendations

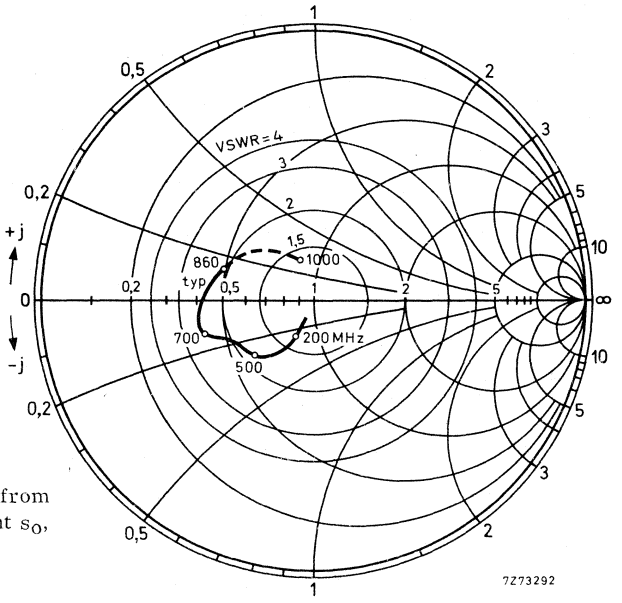
The module should preferably be mounted on double-sided printed-circuit board, see the example shown below.
Input and output should be connected to 75 Ω tracks.
The connections to the "common" pins should be as close to the seating plane as possible.







Input impedance derived from input reflection coefficient s_i, co-ordinates in ohm x 75.



Output impedance derived from output reflection coefficient s_o, co-ordinates in ohm x 75.

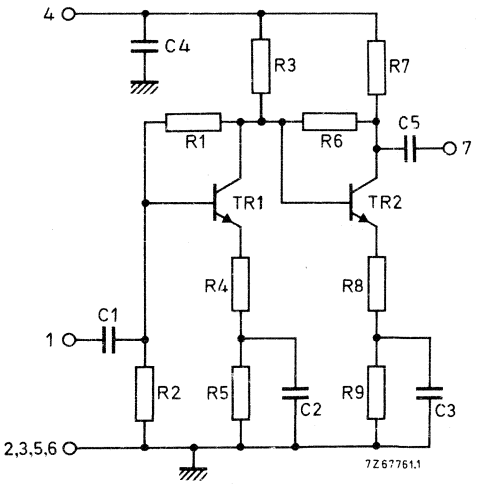
HYBRID VHF/UHF WIDE BAND AMPLIFIER

Two-stage wide-band amplifier in the hybrid technique, designed for use in mast-head booster-amplifiers, as pre-amplifier in MATV systems, and as general-purpose amplifier for v.h.f. and u.h.f. applications.

QUICK REFERENCE DATA				
Frequency range	f		40 to 860	MHz
Source and load (characteristic) impedance	$R_S = R_\ell = Z_0$	=	75	Ω
Transducer gain	$G_{tr} = \lvert s_f \rvert^2$	typ.	15,5	dB
Flatness of frequency response	$\pm\Delta \lvert s_f \rvert^2$	typ.	1	dB
Output voltage at −60 dB intermodulation distortion (DIN45004, 3-tone)	$V_{o(rms)}$	>	98	dBμV
Noise figure	F	typ.	6	dB
D.C. supply voltage	V_B	=	24	V ±10%
Operating ambient temperature	T_{amb}		−20 to +70	°C

ENCAPSULATION 7-pin, in-line, resin-coated body, see MECHANICAL DATA

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Operating ambient temperature	T_{amb}		−20 to +70	°C
Storage temperature	T_{stg}		−40 to + 125	°C
D.C. supply voltage	V_B	max.	28	V
Peak voltages on pins 1 and 7	V_{1M}, V_{7M}	max.	28	V
	$-V_{1M}$, $-V_{7M}$	max.	10	V
Peak incident powers on pins 1 and 7	P_{I1M}, P_{I7M}	max.	100	mW

CHARACTERISTICS

Measuring conditions

Ambient temperature	T_{amb}	=	25	°C
D.C. supply voltage	V_B	=	24	V
Source impedance and load impedance	R_s, R_ℓ	=	75	Ω
Characteristic impedance of h.f. connections	Z_o	=	75	Ω
Frequency range	f	=	40 to 860	MHz

Performance

Supply current	I_B	typ.	33	mA
Transducer gain	$G_{tr} = \lvert s_f \rvert^2$		13 to 18	dB
		typ.	15,5	dB
Flatness of frequency response	$\pm\Delta \lvert s_f \rvert^2$	typ.	1	dB
Individual maximum v.s.w.r.				
input	$VSWR_{(i)}$	typ.	2,5	[1]
output	$VSWR_{(o)}$	typ.	2,0	[1]
Back attenuation				
f = 100 MHz	$\lvert s_r \rvert^2$	typ.	30	dB
f = 860 MHz	$\lvert s_r \rvert^2$	typ.	26	dB
Output voltage at −60 dB intermodulation distortion (DIN45004, par. 6.3: 3-tone)	$V_{o(rms)}$	>	98	dBμV
		typ.	100	dBμV
Noise figure	F	typ.	6	dB

s-parameters:	$s_f = s_{21}$	$s_i = s_{11}$
	$s_r = s_{12}$	$s_o = s_{22}$

[1]) Highest value, for a sample, occuring in the frequency range.

OPERATING CONDITIONS

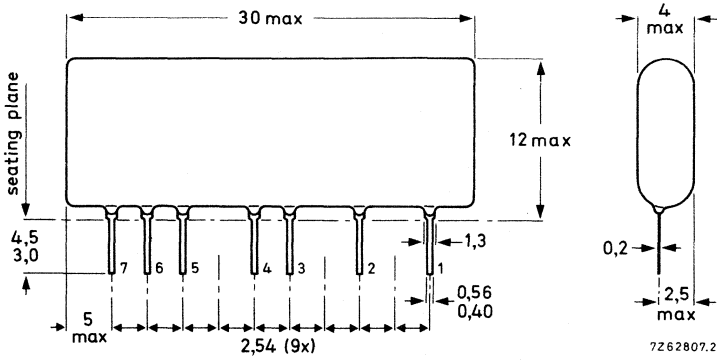
Ambient temperature range	T_{amb}		−20 to + 70	°C
D.C. supply voltage	V_B	=	24	V ±10%
Frequency range	f		40 to 860	MHz
Source impedance and load impedance	R_S, R_ℓ	=	75	Ω

MECHANICAL DATA

Dimensions in mm

Encapsulation

The device is resin coated.



Terminal connections

1	= Input
2, 3, 5, 6	= Common
4	= Supply (+)
7	= Output

Soldering recommendations

Hand soldering

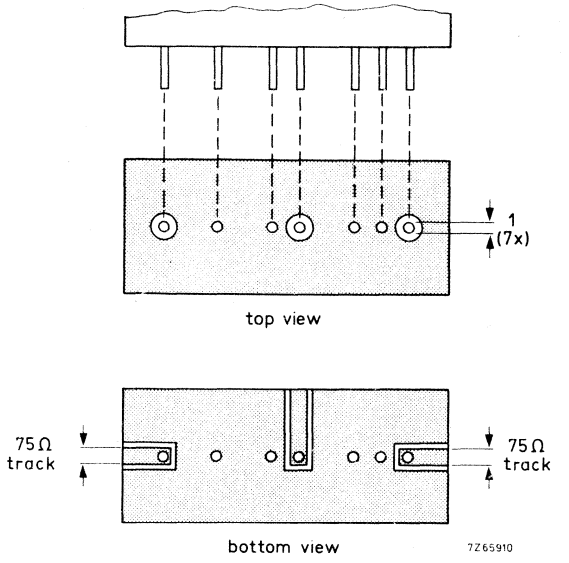
Maximum contact time for a soldering-iron temperature of 260 °C; up to seating plane: 5 s

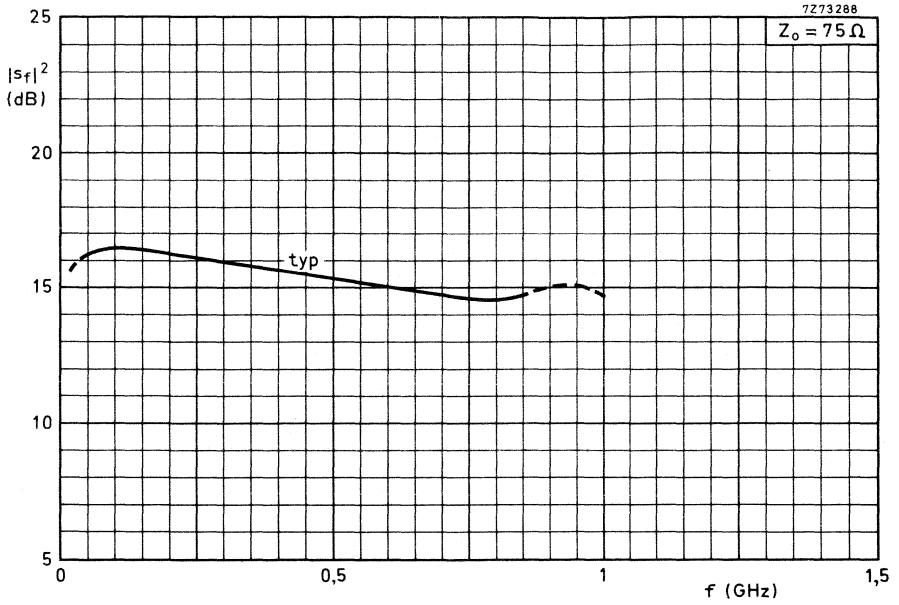
Dip or wave soldering

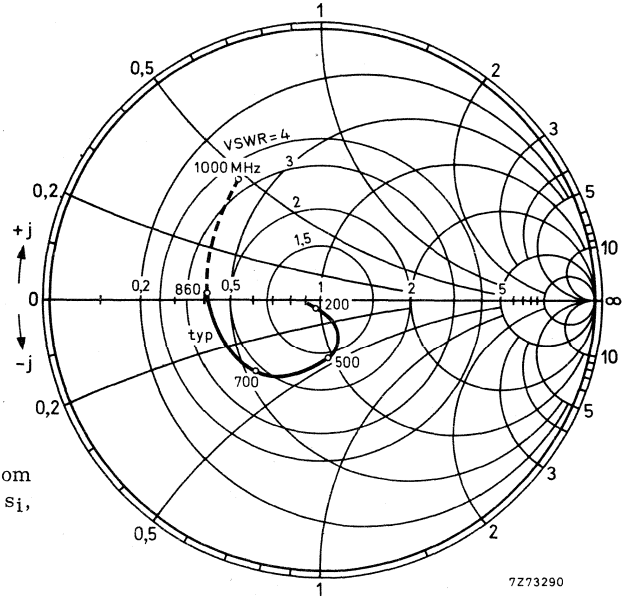
260 °C is the maximum permissible temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted against the printed-circuit board, but the temperature of the device must not exceed 125 °C. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature below the allowable limit.

Mounting recommendations

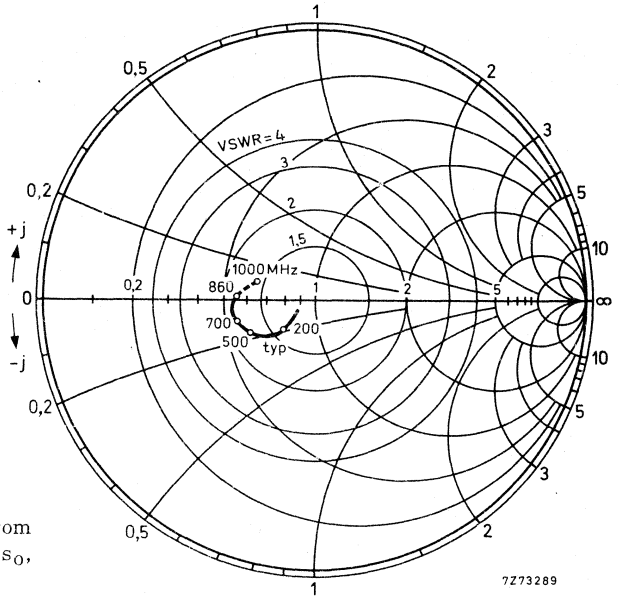
The module should preferably be mounted on double-sided printed-circuit board, see the example shown below.
Input and output should be connected to 75 Ω tracks.
The connections to the "common" pins should be as close to the seating plane as possible.







Input impedance derived from input reflection coefficient s_i, co-ordinates in ohm x 75.



Output impedance derived from output reflection coefficient s_o, co-ordinates in ohm x 75.

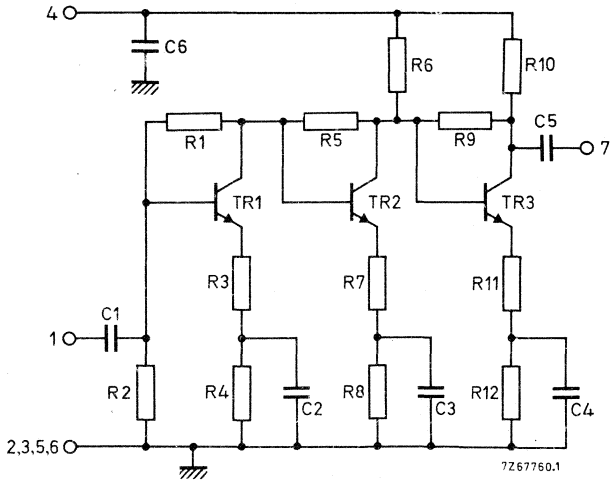
HYBRID VHF/UHF WIDE-BAND AMPLIFIER

Three-stage wide-band amplifier in the hybrid technique, designed for use in mast-head booster-amplifiers, as pre-amplifier in MATV systems, and as general-purpose amplifier for v.h.f. and u.h.f. applications.

QUICK REFERENCE DATA				
Frequency range	f		40 to 860	MHz
Source and load (characteristic) impedance	$R_S = R_\ell = Z_o$	=	75	Ω
Transducer gain	$G_{tr} = \|s_f\|^2$	typ.	27	dB
Flatness of frequency response	$\pm\Delta \|s_f\|^2$	typ.	1,6	dB
Output voltage at −60 dB intermodulation distortion (DIN45004, 3-tone)	$V_{o(rms)}$	>	98	dBμV
Noise figure	F	typ.	5,5	dB
D.C. supply voltage	V_B	=	24	V ±10%
Operating ambient temperature	T_{amb}		−20 to + 70	°C

ENCAPSULATION 7-pin, in-line, resin-coated body, see MECHANICAL DATA

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Operating ambient temperature	T_{amb}		−20 to +70	°C
Storage temperature	T_{stg}		−40 to + 125	°C
D.C. supply voltage	V_B	max.	28	V
Peak voltages on pins 1 and 7	V_{1M}, V_{7M}	max.	28	V
	$-V_{1M}$, $-V_{7M}$	max.	10	V
Peak incident powers on pins 1 and 7	P_{I1M}, P_{I7M}	max.	100	mW

CHARACTERISTICS

Measuring conditions

Ambient temperature	T_{amb}	=	25	°C
D.C. supply voltage	V_B	=	24	V
Source impedance and load impedance	R_s, R_ℓ	=	75	Ω
Characteristic impedance of h.f. connections	Z_o	=	75	Ω
Frequency range	f	=	40 to 860	MHz

Performance

Supply current	I_B	typ.	35	mA
Transducer gain	$G_{tr} = \lvert s_f \rvert^2$		23 to 31	dB
		typ.	27	dB
Flatness of frequency response	$\pm\Delta \lvert s_f \rvert^2$	typ.	1,6	dB
Individual maximum v.s.w.r.				
input	$VSWR_{(i)}$	typ.	1,9	1)
output	$VSWR_{(o)}$	typ.	3,2	1)
Back attenuation				
f = 100 MHz	$\lvert s_r \rvert^2$	typ.	46	dB
f = 860 MHz	$\lvert s_r \rvert^2$	typ.	40	dB
Output voltage at −60 dB intermodulation distortion (DIN45004, par. 6.3: 3-tone)	$V_{o(rms)}$	>	98	dBμV
		typ.	101	dBμV
Noise figure	F	typ.	5,5	dB

s-parameters:	$s_f = s_{21}$	$s_i = s_{11}$
	$s_r = s_{12}$	$s_o = s_{22}$

1) Highest value, for a sample, occuring in the frequency range.

OPERATING CONDITIONS

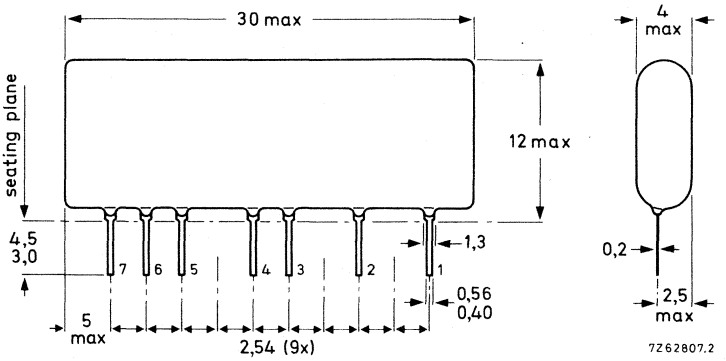
Ambient temperature range	T_{amb}		−20 to +70	°C
D.C. supply voltage	V_B	=	24	V ±10%
Frequency range	f		40 to 860	MHz
Source impedance and load impedance	R_S, R_ℓ	=	75	Ω

MECHANICAL DATA

Dimensions in mm

Encapsulation

The device is resin coated.



Terminal connections

1	= Input
2, 3, 5, 6	= Common
4	= Supply (+)
7	= Output

Soldering recommendations

Hand soldering

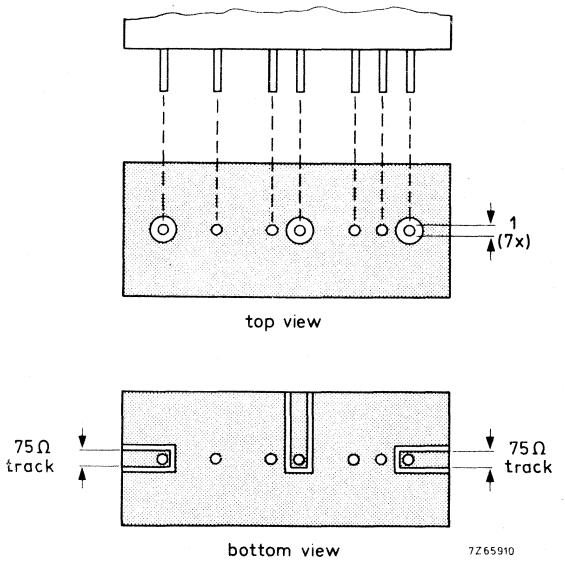
Maximum contact time for a soldering-iron temperature of 260 °C; up to seating plane: 5 s

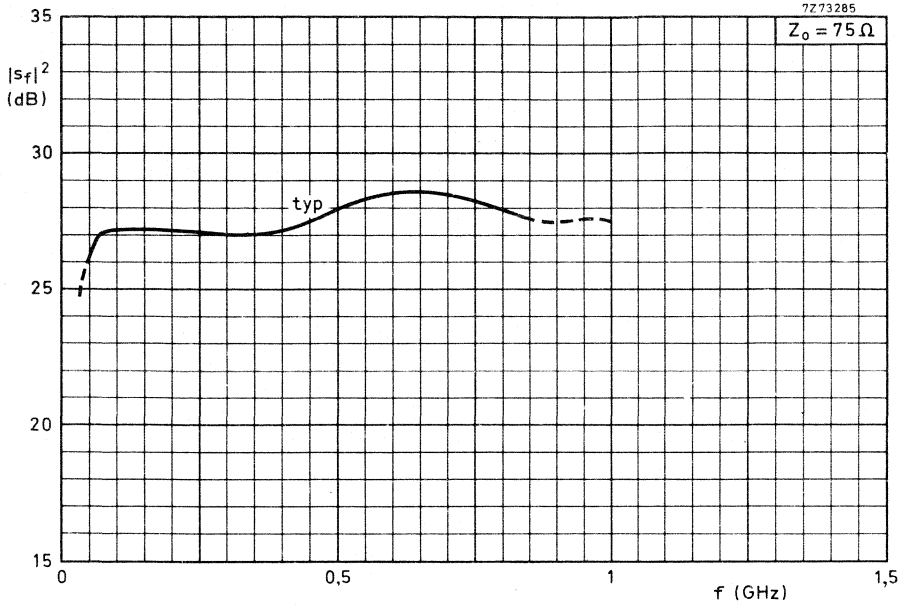
Dip or wave soldering

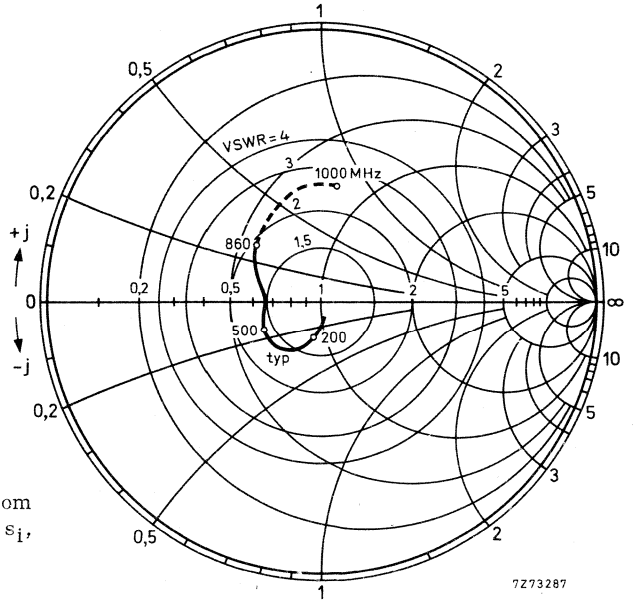
260 °C is the maximum permissible temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted against the printed-circuit board, but the temperature of the device must not exceed 125 °C. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature below the allowable limit.

Mounting recommendations

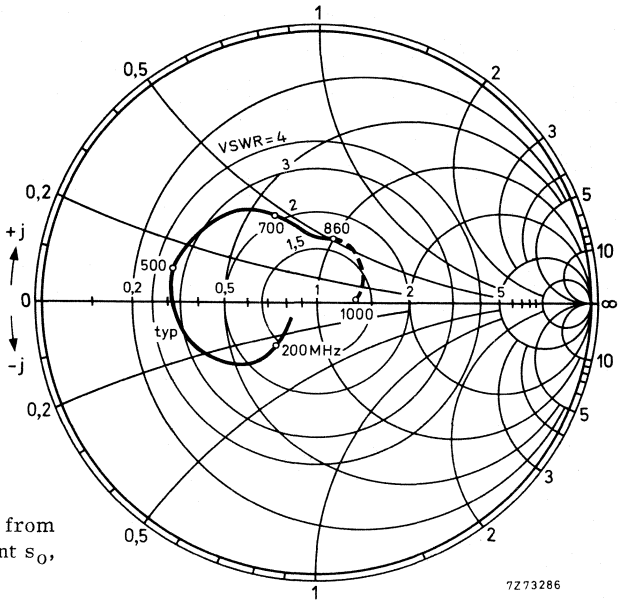
The module should preferably be mounted on double-sided printed-circuit board, see the example shown below.
Input and output should be connected to 75 Ω tracks.
The connections to the "common" pins should be as close to the seating plane as possible.







Input impedance derived from input reflection coefficient s_i, co-ordinates in ohm x 75.



Output impedance derived from output reflection coefficient s_o, co-ordinates in ohm x 75.

Peripheral devices

MOSAIC PRINTERS

INTRODUCTION

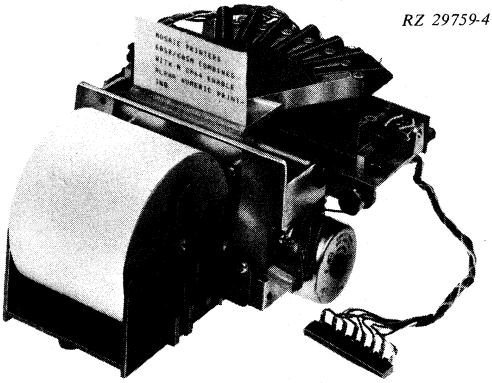
The Mosaic Printers, types 60SR and 60SA, can print all characters that can be formed within a 5x7 dot matrix. The printing speed is 50 characters per second. One line of maximum 20 characters is printed in one second. Both types print on a standard paper roll of 60 mm width.
The 60SR, equipped with an inked-ribbon system, prints on ordinary paper, the 60SA is designed for printing on 3M's self-action paper.
The printers are controlled by a module, containing the circuits for character generation and printer head drive.
The character modules available are:

CM20 for printing the numerals 0 to 9, and 10 symbols (see relevant data sheet)
CM64 for complete alpha-numeric printing with a total capacity of 64 different characters

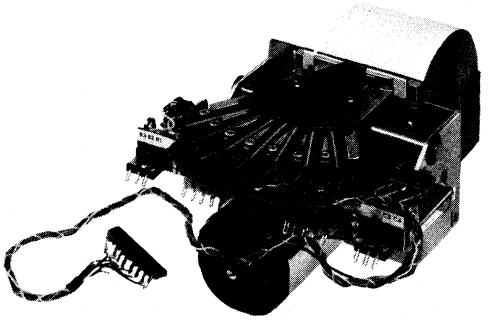
Each character is basically formed within a 5x7 dot matrix, with 5 columns of 7 dots each. The dots are printed by means of 7 needles, with blunt tips, one above the other. The needles are controlled by 7 solenoids and the 7 combinations needle--solenoid are mounted on a printer head. The needles strike the paper from the rear, the characters being read from the front.
The printer head moves from left to right during the printing operation in the normal reading sense. During the return of the printer head the paper is automatically transported upwards.

The Character Module selects and drives the relevant solenoids required to print the character selected at the address inputs. Address input selection and character printing is performed serially, the character being printed immediately after input selection is completed. The logic voltage levels for all input and output terminals are adapted to the commonly used DTL and TTL integrated circuit ranges.

RZ 29759-4

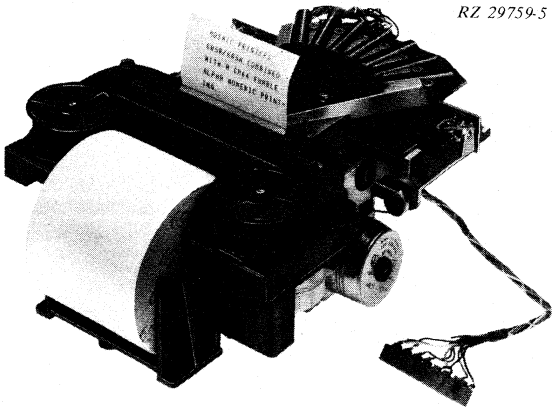


RZ 29759-2

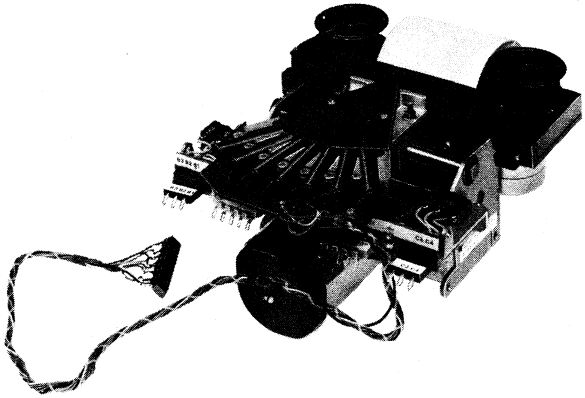


Mosaic printer, type 60SA (cat.no 4311 111 03370).

RZ 29759-5



RZ 29759-3



Mosaic printer, type 60SR (cat.no 4311 111 03380), equipped with inked-ribbon system.

DESCRIPTION OF THE MOSAIC PRINTERS

Main parts (see Fig. 1).

The printer consists of a metal frame which supports the following elements:

1. The cross-slide that carries the printer head on which the 7 solenoids and corresponding needles are mounted in a horizontal plane. When energized the solenoids drive the needles in the direction of the paper roll against the pressure of a spring.
   Although the solenoids are positioned in a horizontal plane, the needles are so guided that their tips are vertically positioned at the printing end.
   For easy replacement the printer head is fixed to the cross-slide by two screws.

2. The anvil on which the needles strike.
   With printer type 60SA, the paper is positioned between needles and anvil.
   With printer type 60SR, one finds the needles, next the paper, then the ribbon and finally the anvil. So, by pushing the paper against the ribbon, each needle tip causes a black dot appear on the paper.

3. Two motors in the case of printer type 60SA.
   Four motors in the case of printer type 60SR.

   The synchronous motors and their drive mechanisms have the following functions:
   - driving the cross-slide, one motor
   - driving the paper roll, one motor
   - driving the inked-ribbon, two motors (for 60SR only)

4. Six micro-switches and one memory bar (see Fig. 2) for the following functions:

   - Switch A : For stopping the paper-drive motor. It is connected in series with switch E and operated at the end of the line by the memory bar (MB1)

   - Switch B : Free. It may be used for indication purposes or for switching off the start signal for the Character Module at the end of the line.

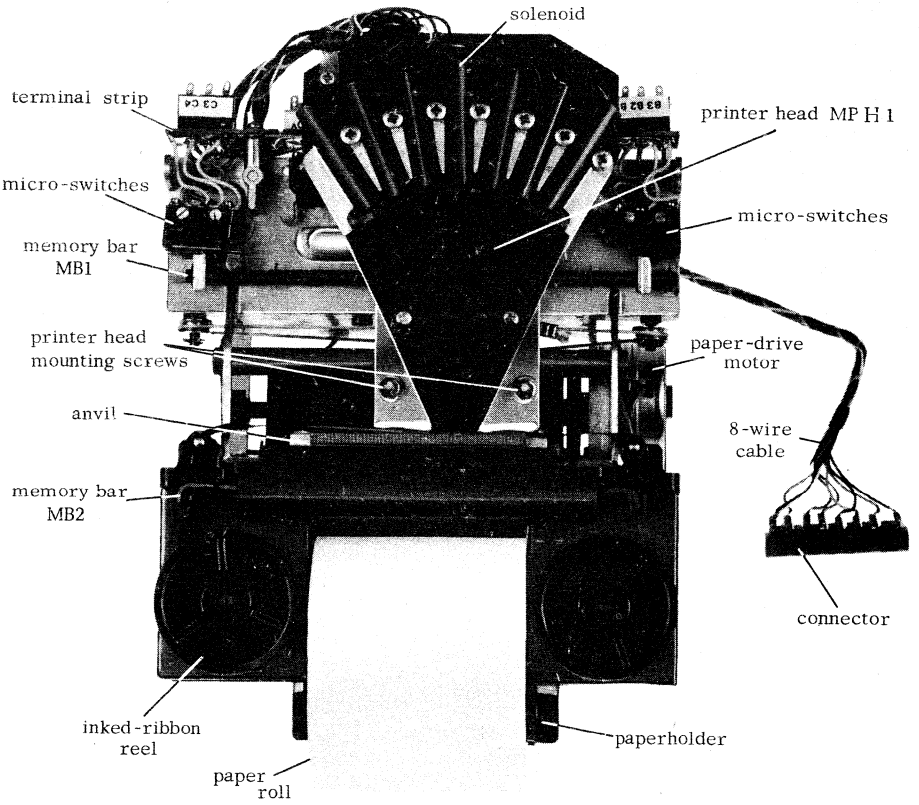
   - Switch C : Commutates the direction of rotation of the printer-head motor; is operated by the memory bar.

   - Switch D : Takes over function of external pushbutton "Start printer". Operates as soon as printer head leaves its rest (extreme left) position.

   - Switch E : Starts the paper-drive motor.
     Connected in series with switch A.

   - Switch F : Supplies signal "start printing" when the printer head motor attains its constant speed.

RZ 29759-6R


solenoid
terminal strip
printer head MP H 1
micro-switches
micro-switches
memory bar MB1
printer head mounting screws
paper-drive motor
anvil
8-wire cable
memory bar MB2
connector
inked-ribbon reel
paperholder
paper roll

5. For type 60SR only:
   Inked-ribbon transport mechanism.
   By means of screws this mechanism is connected at the front to the metal frame. It carries microswitch G and memory bar MB2 controlling the direction of rotation of the two inked-ribbon drive motors RM.

Operation (see Figs 2 and 3)

The printer head is assumed to be in the rest position (extreme left). When the terminals C_3 and C_4 are interconnected (in Fig. 6 "Start printer"), the printer-head motor HM is energized via switch C3-1 and starts moving from left to right (print direction). As soon as it leaves the rest position, switch D takes over the function of the external push-button. After 80 to 100 ms the motor HM attains its constant speed; switch F is then released and gives the signal "Start printing" to the electronic control circuitry. The printing operation can now start. During the movement of the printer head the switch E is operated. The contact E1-3 is opened, to prevent the paper-drive motor from starting as soon as switch A2-3 is closed (at the end of the line). At the end of the line the memory bar actuates commutating switch A so that contacts A1-3 are closed. At the same time switch C is operated and via its contacts C3-2 the motor HM is reversely energized. The printer head is then returned to its rest position. During this return movement switch E is released and via contacts E1-3 and A1-3 the paper-drive motor PM is started. After some time switch F will be operated similarly, interrupting the signal "Start printing".
When the printing head has reached its rest position (extreme left), first switch D is operated, causing the motor HM to stop. Also, memory bar MB1 is operated, commutating the switches A, B and C. Because switch A is switched over to contacts A2-3 the paper-drive motor stops. This ends the operation cycle.

In the 60SR, the ink ribbon is driven by motors RM. When the ribbon spool is empty, the memory bar MB2 is shifted as a result of the tension of the ink ribbon. This operates switch G so reversing the rotation of motors RM and the ink ribbon is then re-wound on the empty spool.

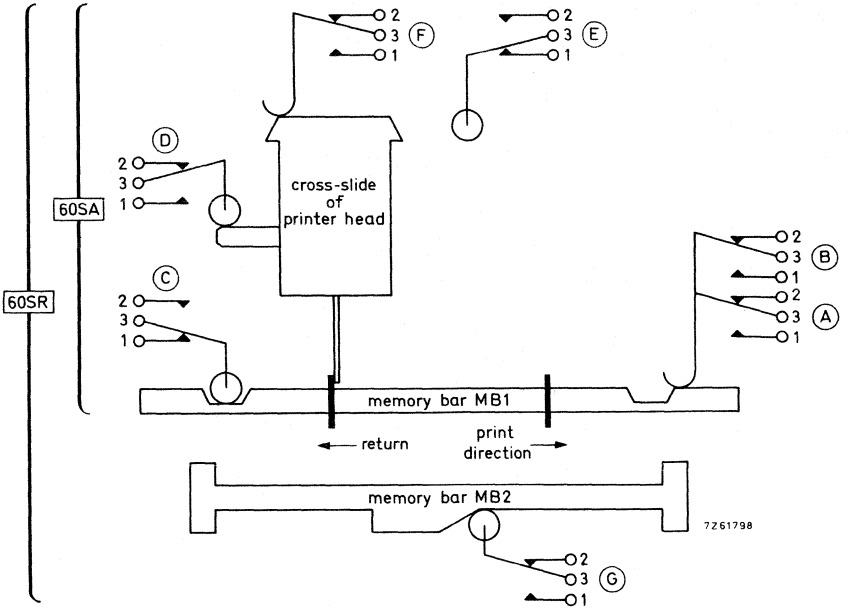


Fig. 2. Operation diagram

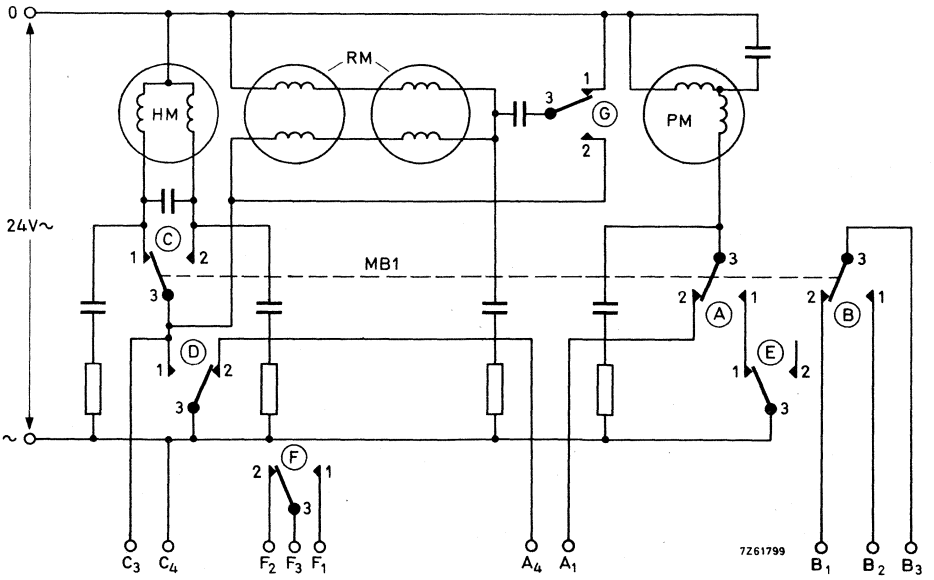
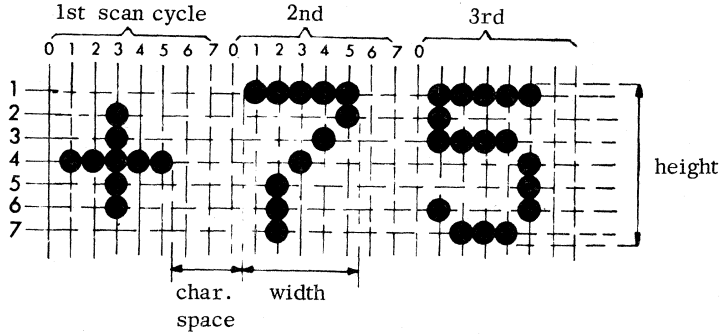


Fig. 3. Circuit diagram

TECHNICAL DATA

Character width	max.	1,5 mm
height		$2.5\ ^{+0.15}_{-0.05}$ mm
Needle diameter		0,35 mm
Character spacing	min. 3 columns,	min. 0,7 mm



Printing speed	50 characters per second
Column capacity	adjustable between approx 18 and 20
Line spacing	approx. 5 mm
Line speed	60 lines of max. 20 characters per min.
Paper transport speed	25 mm/s
Data entry	serial entry
Interconnection time C_3-C_4	
to start printer	min. 30 ms
Temperature range	
operating	0 to +55 °C
storage	−25 to +55 °C
Power supply	
- Printer head,	
voltage }	see Data sheets of
current }	Character Modules
- Motors,	
voltage	24 V ± 10%, 50 Hz
current of	
printer head motor	200 mA
paper transport motor	60 mA
inked-ribbon transport motors (type 60SR only)	90 mA per motor
Overall dimensions,	
width	148 mm (5.83 in)
depth	210 mm (8.26 in)
height	76 mm (2.99 in)
Weight, type 60SR	2 kg approximately
type 60SA	1.5 kg approximately

Mounting

Both printers are provided with 7 mounting holes, positioned as shown in Fig. 5.

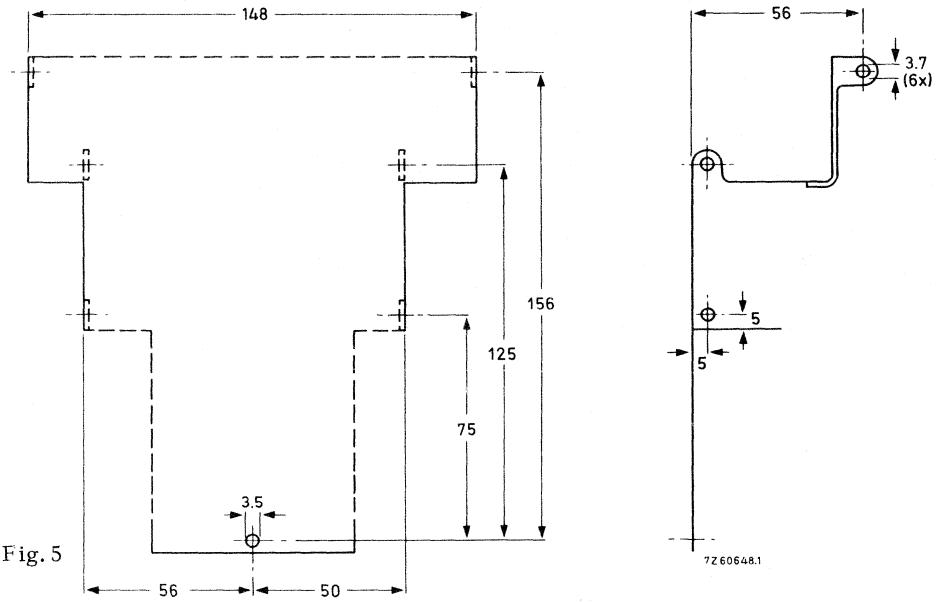


Fig. 5

The 6 holes of 3.7 mm should be used for fixation with self-tapping screws of 4 mm

Electrical connections

The printer head is equipped with a 9-wires flexible cable of which 8-wires are to be connected to the character module and 1 wire to the earth point on the rear panel of the printer. The 8-wire connection is pluggable at the character module.
To the rear of the frame-work a small p.w. board is mounted. The pluggable connections are shown below (see also Fig. 3).

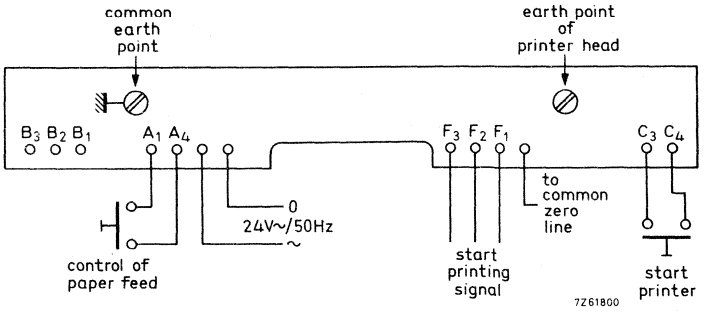


Fig. 6

ACCESSORIES

Printpapers

Normal paper (catalogue number 2811 063 10001)

-length	36 m approximately
-width	59 ± 1 mm
-external diameter	max. 73 mm
-internal diameter	max. 12 mm
-force factor	64 g/m^2
	e.g. Velin AFNOR VII-1 type
-thickness	approx. 0.1 mm

Selfprinting paper (catalogue number 2811 063 10051)

-length	36 m approximately
-width	59 ± 1 mm
-external diameter	73 mm max.
-internal diameter	12 mm
-force factor	45 g/m^2
-colour	white
	green-yellow
-name	3M's action paper

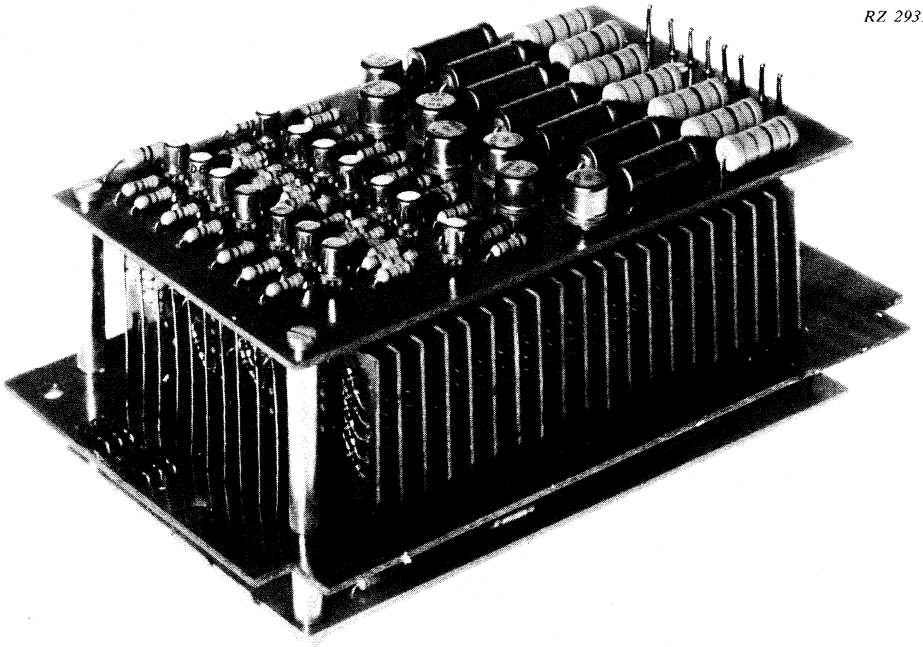
Inked-ribbon (catalogue number 2811 062 06001)

-reel	DIN 2103
-external diameter	40 mm
-axe diameter	11 mm
-length of the ribbon	min. 8, max. 10 m
-width of the ribbon	13 mm
-ribbon quality	silk, monocolour (black)

Character modules

-CM20, 20-character module, see relevant Data sheet
-CM64, 64-character module

20-CHARACTER MODULE



RZ 293103

INTRODUCTION

The 20-character module has been designed to control a mosaic printer type 60SA or 60SR. It selects and drives the various solenoids of the printer head in order to print the character selected at the character inputs.
Character input selection and character printing is performed serially. The logic voltage levels for all input and output terminals are adapted to the commonly used DTL and TTL integrated circuits.

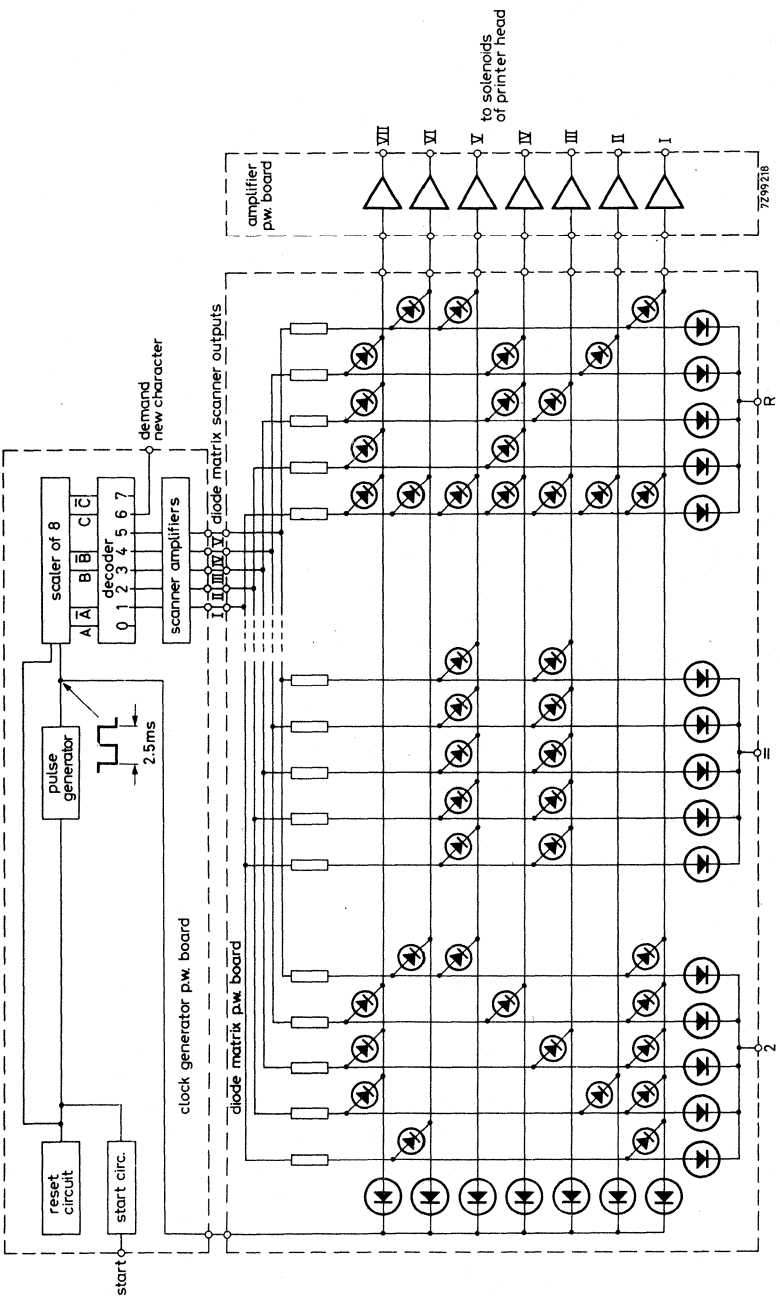


Fig. 1. Circuit diagram of CM20

DESCRIPTION

Basic parts

The module consists of three major parts (horizontal printed-wiring boards in the photograph on the front page) namely from bottom to top:

- the clock generator, decoding circuits for the scanning operation and start circuit.
- the character diode matrices.
  Each character has its own diode configuration mounted on a small vertical printed-wiring board. All boards are basically identical in design.
- the solenoid amplifying circuits (separately available as AC20, catalogue number 4311 111 03330).

Operation

In the circuit diagram (Fig. 1) the three main electronic circuits are clearly indicated. For the explanation of the system function the characters 2, = and R are chosen arbitrarily. Suppose the pulse generator is started. It triggers the scaler of 8 and after 8 trigger pulses the scaler has completed one cycle and regains its zero position. Out of the 8 scaler states, 6 sequential ones are used after decoding and amplifying, namely:

- 5 for scanning the diode matrices
- 1 for demanding a new character as soon as the diode scanning operation is completed.

The scanner outputs I to V are applied to the corresponding inputs of the diode matrices. If a character input is at a high level, the printer solenoids will be energized during the scanning operation depending on the diode configuration. This can be explained as follows:
The five scanning lines control the printing of the dots in the corresponding 5 columns of which each character is constructed. The number of dots per column is controlled by the diode matrix configuration. Suppose the figure 2 is to be printed, then the corresponding input is at high level. As soon as the pulse generator is started, the scaler changes state and, after decoding, the scanning line I will be high. It can be seen that in the first column the solenoids 2 and 7 will be energized and the corresponding dots are printed. At the next trigger pulse the scanning line II will be high and now the solenoids 1, 6 and 7 are energized. Consequently the corresponding dots will be printed in the 2nd column.
At the following 3 trigger pulses the scanning lines III, IV and V select the solenoids depending on the diode configuration and the dots will be printed accordingly. Now the printing cycle of the character is completed.
State 6 of the scaler is, after decoding, used to ask for a new character. States 7 and 0 have no specific function but are used together with state 6 for spacing purposes between two succeeding characters.

Furthermore the output of the pulse generator is fed direct to the diode matrices. It serves three purposes:

- To allow the solenoids to be de-energized and ready for the next scanning pulse.
- To prevent the system from being triggered by interfering pulses.
- To limit the dissipation in the power amplifiers because the operation time is only 1.2 ms.

The seven power stages, mounted on one printed-wiring board are straightforward circuits that supply the required energy for the solenoids driving the needles.

TECHNICAL DATA

Characters available	numerals 0 to 9 symbols - . + x ÷ * ◊ R M
Power supply	
solenoids, voltage	21.6 to 26.4 V, max. 28 V *)
current	max. 6 A (0.85 A per solenoid) for approx. 1.25 ms, with a period time of 2.5 ms **)
module, voltage	4.75 to 5.25 V, max. 7.0 V *)
current	200 mA
Power consumption	21 W
Ambient temperature range	
operating	0 to 55 °C
storage	-40 to +70 °C

Logic levels

Character inputs

Input conditions: A character is selected when its input is at high level; all other inputs must be at low level.

Input HIGH	V	min. 2.4 V
	I	max. 65 µA at V = 2.4 V ***)
Input LOW	V	max. 0.8 V
	-I	max. 1.5 mA at V = 0.8 V

Start input

Input conditions: The electronic module is started when the start signal is at low level.

Input HIGH	V	min. 2 V
	I	max. 290 µA at V = 2.4 V (V_{supply} = 5.25 V)
Input LOW	V	max. 0.6 V
	-I	max. 1.6 mA at V = 0.4 V (V_{supply} = 5.25 V)

It is allowed to drive the start circuit by integrated circuits of the FC-family provided units are used with a built-in collector resistance.

*) Limiting values in accordance with the Absolute Maximum Rating System of IEC134.

**) In practice the current has an average value of 1.7 A because on an average only 2 solenoids are energized simultaneously.

***) Minimum duration can be found in Fig. 2 ($V_{char\ 1}$ and $V_{char\ 2}$).

Demand New Character output

When the signal "demand new character" is present this output is at low level.

Output HIGH	V	min. 2.4	V	at V_{supply} = 4.75 V
	-I	max. 0.4	mA	
Output LOW	V	max. 0.4	V	at V_{supply} = 4.75 V
	I	max. 16	mA	
Fan-out	10 TTL gate loads			

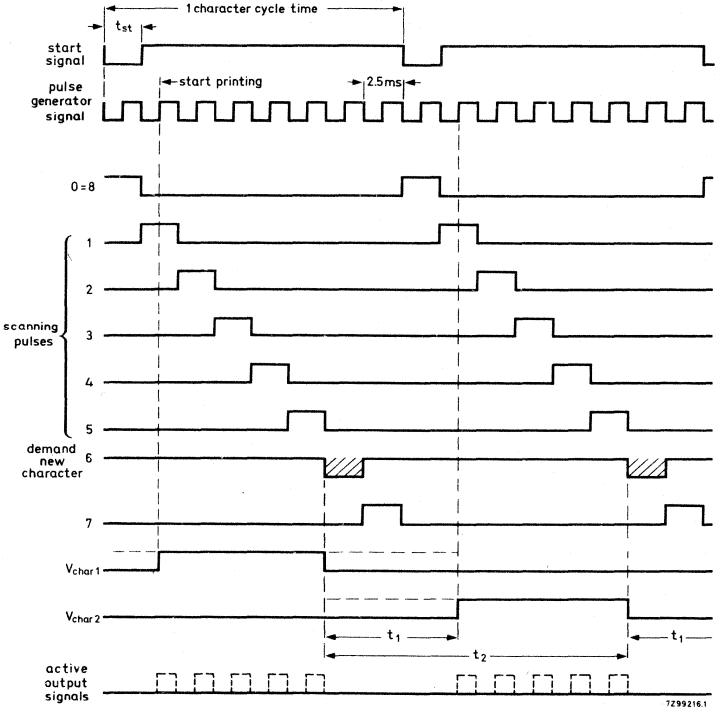


Fig. 2. Time sequence diagram of the printing operation.

t_{st} = min. 2.5 ms

t_1 = min. 0 ms

max. (3 x 2.5 + 1.5) ms = max. 9 ms

t_2 = min. 20 ms

max. 29 ms

Terminal location

The module is provided with 26 contacts on the diode matrices printed-wiring board adapted to a single sided printed-wiring connector type FO45.
The amplifier printed-wiring board has 8 terminals, of which 7 are to be connected to the 7 solenoids on the printer head and one supplies the common 24 V.
Both types of Mosaic Printer are supplied with an 8-pole plug for the purpose.

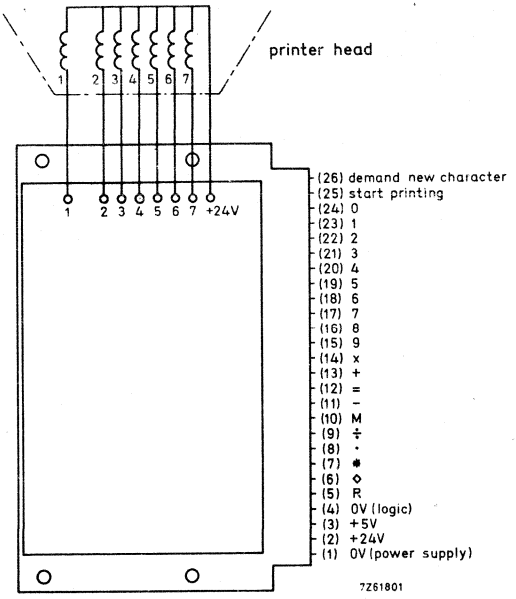


Fig. 3

Dimensions of the module in mm

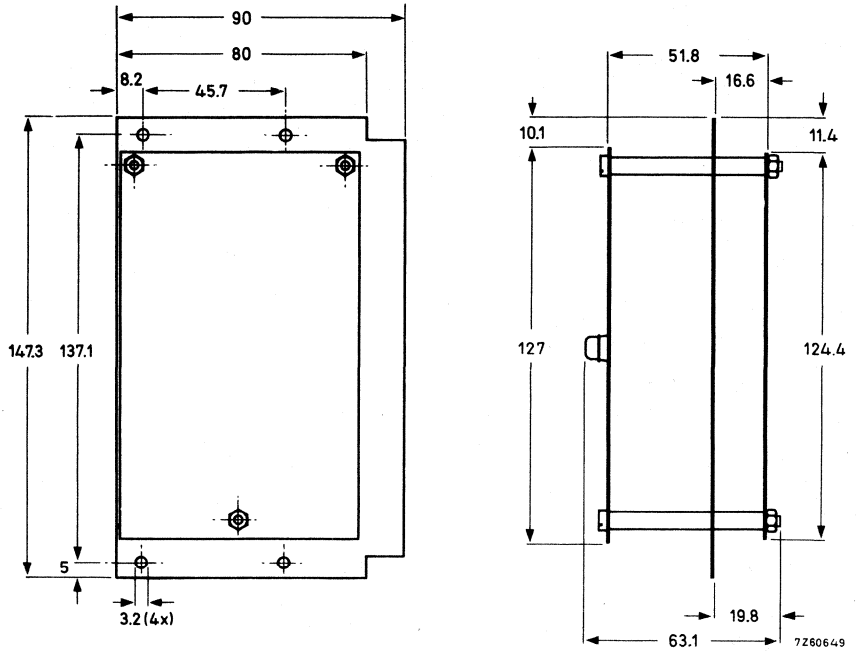


Fig. 4

Overall dimensions,	width	148 mm (5.83 in)
	depth	90 mm (3.54 in)
	height	64 mm (2.52 in)
Weight		250 g approximately

Mounting

The printed-wiring board carrying the character diode matrices is provided with 4 mounting holes.

CONNECTIONS BETWEEN PRINTER, CHARACTER MODULE AND PERIPHERAL WORLD

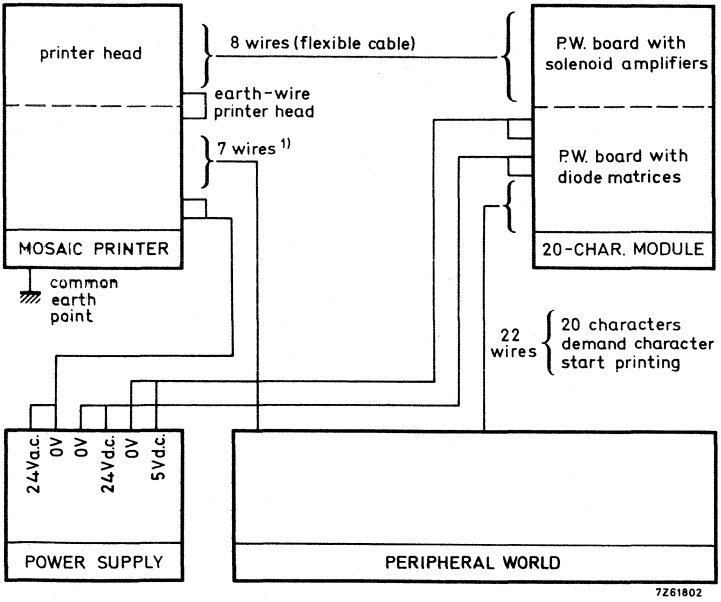


Fig. 5

1) manual control of paper drive motor 2 wires
start of head motor 2 wires
switch "start printing" 3 wires

64-CHARACTER MODULE FOR MOSAIC PRINTERS

QUICK REFERENCE DATA	
The CM64 consists of a CC64, 64-character circuit a AC64, amplifier circuit	
Characters *)	@ABCDEFGHIJKLMNOPQ RSTUVWXYZ[\]^_ !"£ $%&'()*+,-./012345 6789:;<=>?
Address input	6 bits

*) Also obtainable with other characters on request

APPLICATION

The CM64 is intended to operate in conjunction with the mosaic printers 60SR and 60SA.

DESCRIPTION

The module comprises the electronic circuitry for alpha-numeric selection and supplies the driving power for character printing.
The 64 characters, stored in a Read Only Memory (MOS-ROM) formed within a 5 x 7 dot matrix (5 vertical columns of 7 dots per column), are selected by means of a 6-bit address signal (in accordance with the USASCII-code, but the character ≠ has been replaced by £).
With 7 needles placed in a vertical row the characters are printed by driving the appropriate needles of the 7- needle vertical colomn in the 5 colomn positions of the printer head. Spacing between two adjacent characters is equal to 3 column positions.
The CM64 consists of 2 glass-epoxy printed-wiring boards which fit into our miniature mounting chassis. One printed-wiring board, the 64 Character Circuit (CC64) comprises the start circuit, oscillator, column counter, input and output gates, and the 64 Character MOS-ROM of 2240 bits. On the other printed-wiring board, the Amplifier Circuit (AC64), are 7 amplifier circuits for driving the 7 needle solenoids of the printer head.
The character is printed immediately after the input selection is done and the start signal is given. Address input selection and character printing are performed serially. The logic voltage levels for all input and output terminals are adapted to commonly used 5-volt logic integrated circuit ranges (e.g. DTL and TTL).

DIMENSIONS (mm) AND TERMINAL LOCATION

Character circuit CC64 , see Fig. 1.

Terminals on printed-wiring connector

1 = Q_{osc} , oscillator output
3 = I_{st} , start input
7 = V_{P1} , +5 V supply
8 = V_{P1} , +5 V supply
10 = Q_D , 4th output column counter
11 = Q_C , 3rd output column counter
12 = Q_B , 2nd output column counter
13 = Q_A , 1st output column counter
15 = 0 V , common 0-line
16 = 0 V , common 0-line
17 = I_7 , inhibit input
18 = I_1 , address input
19 = I_2 , address input
20 = I_3 , address input
21 = I_4 , address input
22 = I_5 , address input
23 = I_6 , address input
24 = Q_{DN} , "demand new character" output
25 = V_{P2} , +14 V supply
26 = V_N , −14 V supply
29 = O_1 , character output
30 = O_2 , character output
31 = O_3 , character output
32 = O_4 , character output
33 = O_5 , character output
34 = O_6 , character output
35 = O_7 , character output

Requirements for electrical connection

Terminals 7 and 8 of the printed-wiring connector must be interconnected.

Terminals 15 and 16 of the printed-wiring connector must be interconnected.

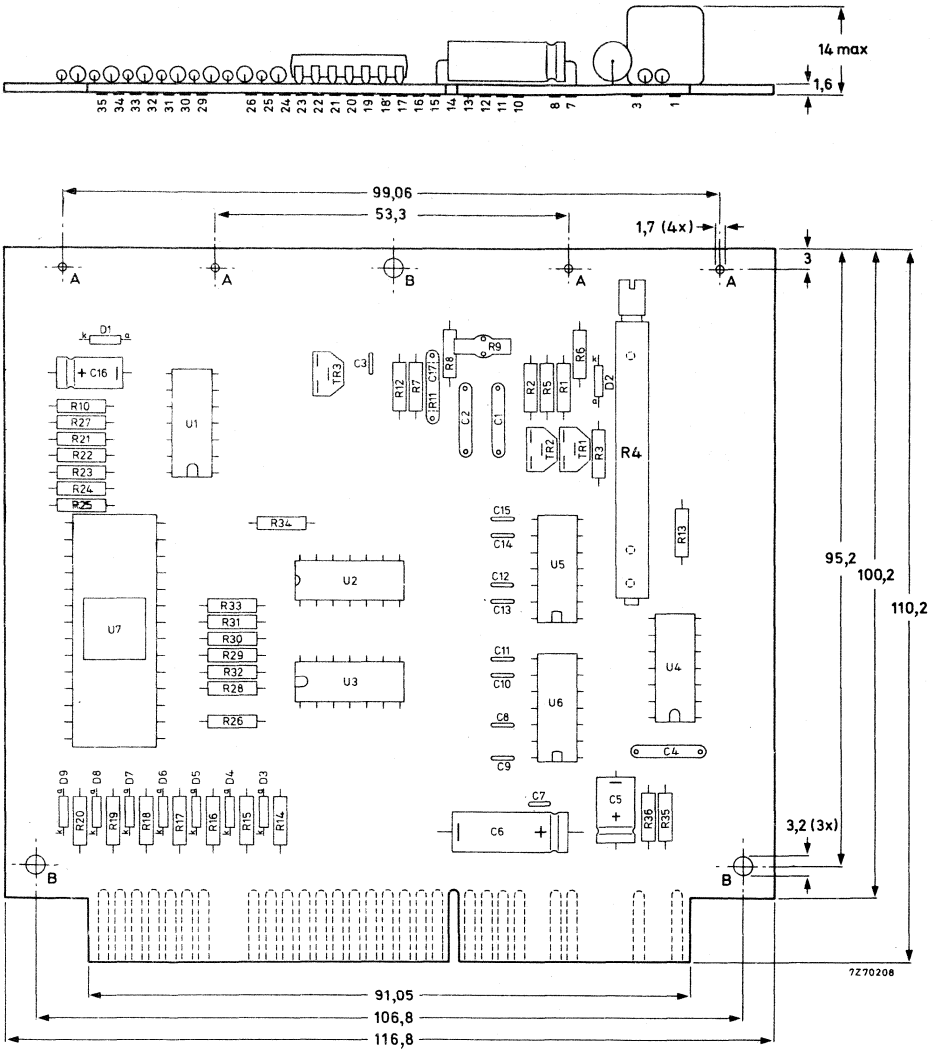


Fig. 1

Holes A are provided for mounting of an extractor.
Holes B are provided for screw-mounting the module.

Amplifier circuit CC64 see Fig. 2.

Terminals an printed-wiring connector

1 = supply printer head
3 = Q_7 , output solenoid 7
5 = Q_6 , output solenoid 6
7 = Q_5 , output solenoid 5
9 = Q_4 , output solenoid 4
11 = Q_3 , output solenoid 3
13 = Q_2 , output solenoid 2
15 = Q_1 , output solenoid 1
22 = V_{P3} , +24 V supply
23 = V_{P3} , +24 V supply
24 = 0 V , of V_{P3} supply
25 = 0 V , of V_{P3} supply
26 = 0 V , of V_{P1} supply
27 = V_{P1} , +5 V supply
29 = G_1 , control input
30 = G_2 , control input
31 = G_3 , control input
32 = G_4 , control input
33 = G_5 , control input
34 = G_6 , control input
35 = G_7 , control input

Pins on the printed-wiring board *)

36 = supply printer head
37 = Q_7 , output solenoid 7
38 = Q_6 , output solenoid 6
39 = Q_5 , output solenoid 5
40 = Q_4 , output solenoid 4
41 = Q_3 , output solenoid 3
42 = Q_2 , output solenoid 2
43 = Q_1 , output solenoid 1

*) These pins are provided for supply and control of the printer head MPH1 via its cable connector.

Requirements for electrical connection

Terminal 1 is only to be used for supply of the printer head of the mosaic printer.

Terminals 22 and 23 of the printed-wiring connector must be interconnected.

Terminals 24 and 25 of the printed-wiring connector must be interconnected.

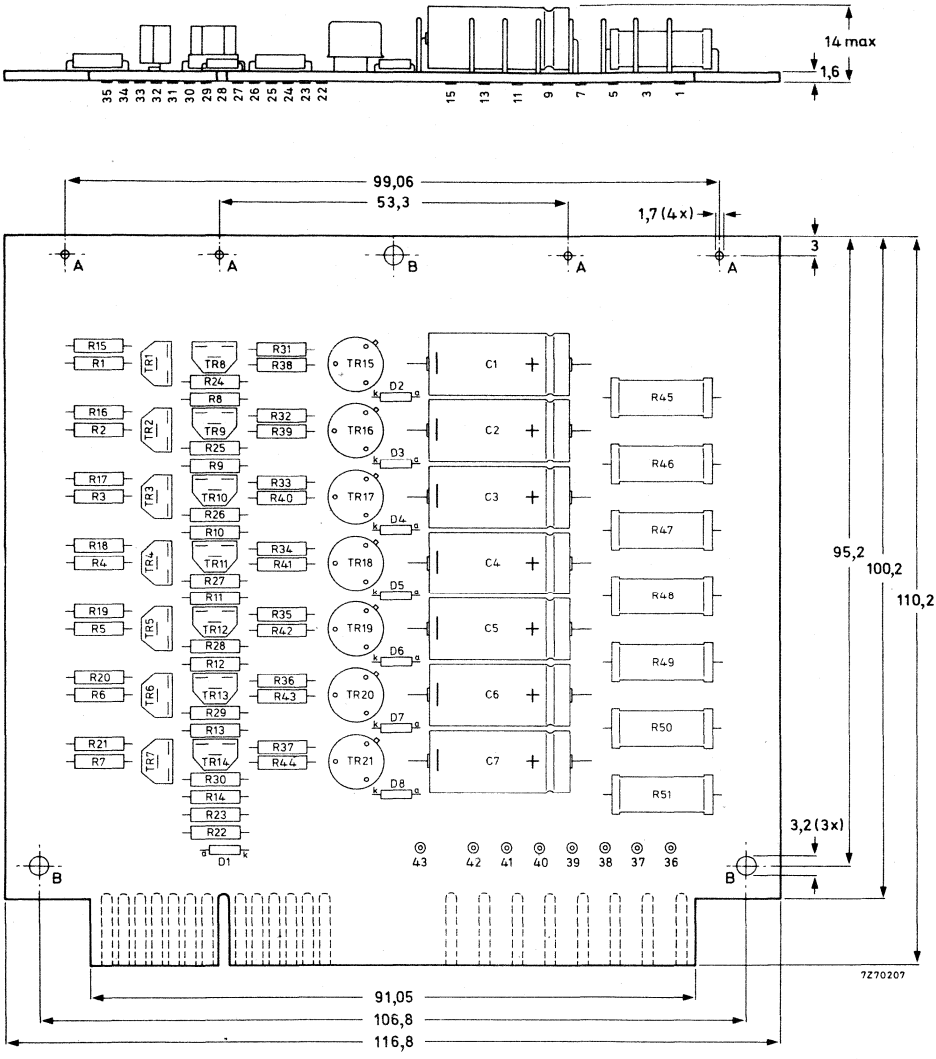


Fig. 2

Holes A are provided for mounting of an extractor.
Holes B are provided for screw-mounting the module.

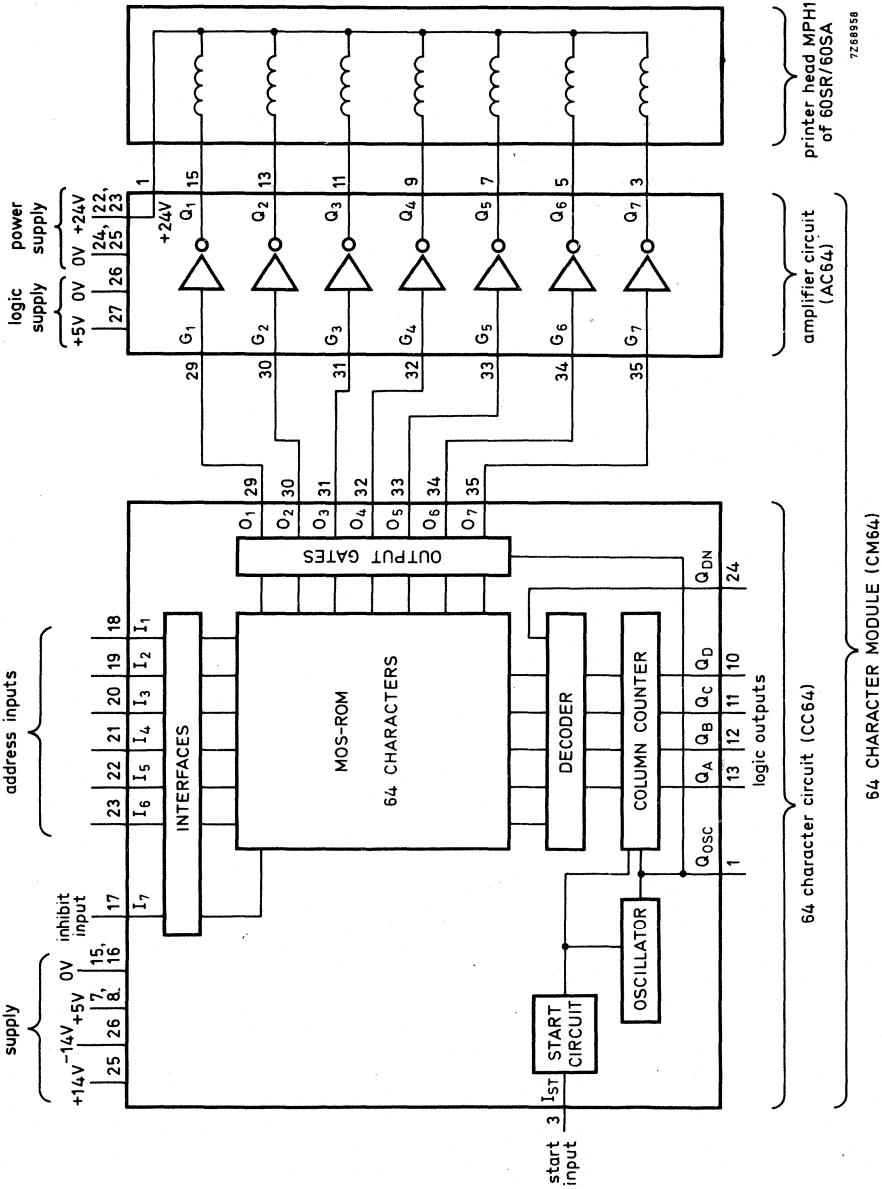


Fig. 3. Block diagram of the CM64

OPERATION

The heart of the system is a MOS-Read-Only-Memory with a total capacity of 2240 bits. For each character, 5 x 7 bits are reserved resulting in a content of maximum 64 characters. Statically operated the ROM has 6 address-inputs to select the required character. The address selecting codes for the various characters are in conformity with the USASCII code. Once a character is selected the column inputs of the ROM have to be scanned sequentially by the column counter.
By scanning the 5 column inputs, 5 groups of 7 bits each are obtained to form the character selected. The 7 output lines of the ROM control the 7 amplifier stages required for energizing the 7 solenoids of the printer head. (See Fig. 3).

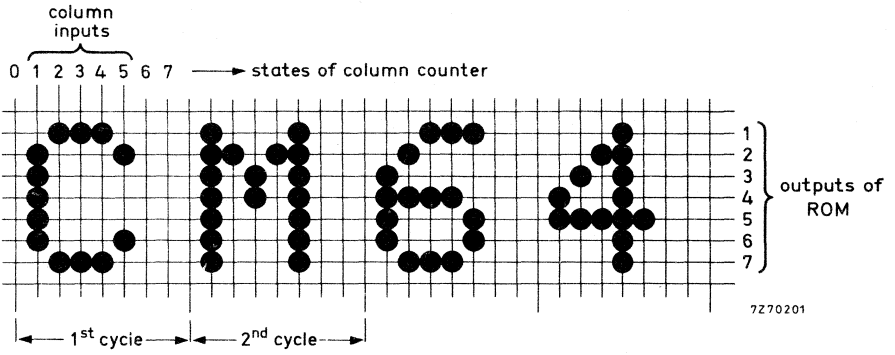


Fig. 4

The column counter is an 8-position counter. The 0-position is the start, or reset, position. The next 5 positions (1 to 5) are used to drive sequentially the 5 column inputs of the ROM. Positions 6 and 7, and the 0-position of the successive scanning cycle, define the spacing between two adjacent characters. In position 6 of the counter a "Demand New Character" signal is generated. This signal is an indication that the code on the address inputs may be changed.
The column scanning frequency is derived from an oscillator with a frequency of approximately 400 Hz. The frequency of the oscillator can be adjusted to match the CM64 to the printing speed of the mosaic printer, i.e. 20 characters on one line.
The oscillator is started and stopped by the start circuit.
After starting the oscillator first generates a HIGH-level signal at its output. When the output level of the oscillator becomes LOW, the column counter changes state (to position 1) and the first column input is scanned. At the following HIGH-level of the oscillator signal, the output gates are opened, allowing the first selected group of 7 bits to be printed. Similarly the remaining 4 columns are selected and printed, to complete the whole character. As soon as the column counter has left its start position, the signal to the start input is no longer required, because a feedback signal from the column counter maintains oscillation.
After completion of one cycle of 8 steps, the feedback signal stops the oscillator automatically. A new start signal is required to initiate a new cycle. When the start signal is applied continuously the feedback signal is overruled and the character printing is not stopped.

TECHNICAL DATA

Power supplies

Character circuit CC64:

V_{P1}		4,75 to 5,25	V
I_{P1} at V_{P1} = 5 V		100	mA
V_{P2}		12 to 15	V
I_{P2} at V_{P2} = 14 V		40	mA
V_N		−12 to −14	V
I_N at V_N = −14 V	max.	0,5	mA
Power consumption		1	W

Amplifier circuit AC64:

V_{P1}		4,75 to 5,25	V
I_{P1} at V_{P1} = 5 V		180	mA
V_{P3}		21,6 to 26,4	V
I_{P3}		see note	
Power consumption		20	W

Ambient temperature range

Character circuit CC64	operating	0 to +70	°C
	storage	−25 to +70	°C
Amplifier circuit AC64	operating	0 to +55	°C
	storage	−25 to +70	°C

Note

Supply V_{P3} is only to drive the 7 solenoids of the printer head MPH1.
Current I_{P3} is max. 6 A (0, 85 A per solenoid) during approx. 1,25 ms, with a period time of 2,5 ms. In practice I_{P3} has an average peak value of 1,7 A.
As the connection wire from the power supply to the AC64 has some inductance, it is recommended that a capacitor be connected (approximately 30 µF per meter of wire) between the supply terminals 22 + 23 and 24 + 25 of the AC64 board.

Ratings Limiting values in accordance with Absolute Maximum System (IEC 134)

Supply voltage	V_{P1}	max.	5,5	V
	V_{P2}	max.	15	V
	V_N	max.	−15	V
	V_{P3}	max.	26,4	V
Input voltage (all inputs)				
CC64	V_i	max.	5,5	V
AC64	V_G	max.	5,5	V
Output peak current of				
AC64	I_{Qp}	max.	1	A

STATIC DATA

Character circuit CC64

Character address inputs I_1 to I_6 (TTL-compatible)

Input voltage HIGH	V_{IH}	min.	+2,0	V
Input current at V_{IH} = +2,4 V, V_{P1} = +5,25 V	I_{IH}	max.	40	μA
Input voltage LOW	V_{IL}	max.	+0,8	V
Input current at V_{IL} = +0,4 V, V_{P1} = +5,25 V	$-I_{IL}$	max.	1,6	mA

Inhibit input I_7 (TTL-compatible)

Input conditions	Character generation is enabled when I_7 signal is HIGH			
Input voltage HIGH	V_{IH}	min.	+2,0	V
Input current at V_{IH} = +2,4 V, V_{P1} = +5,25 V	I_{IH}	max.	40	μA
Input voltage LOW	V_{IL}	max.	+0,8	V
Input current at V_{IL} = +0,4 V, V_{P1} = +5,25 V	$-I_{IL}$	max.	1,6	mA

Start input I_{st}

Input conditions	Column counter is started when I_{st} signal is LOW			
Input voltage HIGH	V_{IH}	min.	+2,0	V
Input current at V_{IH} = +2,4 V, V_{P1} = +5,25 V	I_{IH}	max.	40	μA
Input voltage LOW	V_{IL}	max.	+0,6	V
Input current at V_{IL} = +0,2 V, V_{P1} = +5,25 V	$-I_{IL}$	max.	1,6	V

Character outputs O_1 to O_7

Output conditions		HIGH corresponds to a dot LOW corresponds to a blank		
Output voltage HIGH at $-I_{OH}$ = 0,5 mA	V_{OH}	min.	(V_{P2}-7)	V
Output voltage HIGH at $-I_{OH}$ = 1 mA	V_{OH}	min.	(V_{P2}-14,5)	V
Output current for a blank	$-I_{OL}$	max.	10	µA

The outputs are intended to drive the inputs G_1 to G_7 of the amplifier circuit AC64.

Oscillator output Q_{osc} (TTL-compatible), V_{P1} = +4,75 V

Output voltage HIGH at $-I_Q$ = max. 40 µA	V_{QH}	min.	+2,4	V
Output voltage LOW at I_Q = max. 1,6 mA	V_{QL}	max.	+0,4	V
Fan-out			1 TTL gate load	

'Demand new character' output Q_{DN} (TTL-compatible), V_{P1} = +4,75 V

Output voltage HIGH at $-I_Q$ = max. 320 µA	V_{QH}	min.	+2,4	V
Output voltage LOW at I_Q = max. 12,8 mA	V_{QL}	max.	+0,4	V
Fan-out			8 TTL gate loads	

Column counter outputs Q_A to Q_D (TTL-compatible), V_{P1} = +4,75 V

Output voltage HIGH at $-I_Q$ = max. 80 µA	V_{QH}	min.	+2,4	V
Output voltage LOW at I_Q = max. 3,2 mA	V_{QL}	max.	+0,4	V
Fan-out			2 TTL gate loads	

State table:

positions of column counter	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

logic "1" is the HIGH-state
logic "0" is the LOW-state

Amplifier circuit AC64

Control inputs G_1 to G_7

The correct input signals are supplied by the outputs O_1 to O_7 of the CC64.

If the AC64 is to be supplied with input signals from a source other than the CC64, then the following input levels must be used.

Input voltage HIGH	V_{GH}	min.	+2,4	V
Input current at V_{GH} = +2,4 V [1]	I_{GH}	max.	0,4	mA
Input current at V_{GH} = +4,75 V	I_{GH}	max.	1,0	mA
Input voltage LOW	V_{GL}	max.	1,0	V
Input current at V_{GL} = +1,0 V	I_{GL}	max.	20	µA
Input current at V_{GL} = 0 V	$-I_{GL}$	max.	1,0	mA

Outputs Q_1 to Q_7

These drive the seven solenoids in the printer head MPH1 of the Mosaic Printers 60SA and 60SR. The common return lead from the MPH1 must be connected to terminal 1 or tag 36.

Output peak current	I_{Qp}	max.	1	A

DYNAMIC DATA

Character circuit CC64

Scanning time for one column [2]	t_{sc}	min.	1,8	ms
		max.	3,3	ms
Cycle time for one character	t_{char}		$8 \times t_{sc}$	
Output activation time during one scan	t_{act}	typ.	1,2	ms
Hold time for address information [3]	t_a		$5 \times t_{sc}$	
Hold time for start signal	t_{st}	min.	1,5	ms
Duration of 'Demand new character' signal	t_{DN}		$1 \times t_{sc}$	

[1] TTL compatible

[2] t_{sc} may be adjusted by means of potentiometer R4 (see Fig. 1) to match the CM64 to the printer speed.

[3] The address information must be present during positions 1 to 5 of the column counter.

Amplifier circuit AC64

Input pulse requirements for controlling the printer head MPH1 of the Mosaic Printers 60SA and 60SR.

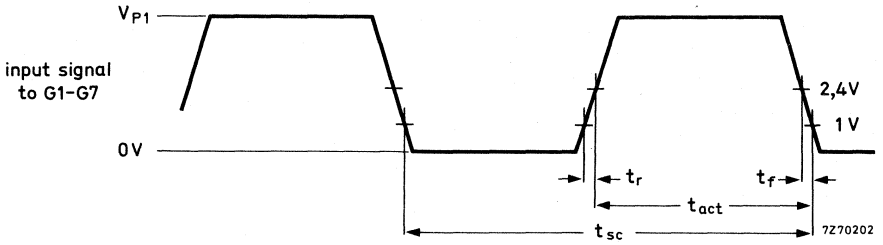


Fig. 5

Rise and fall time	t_r, t_f	max.	25	µs
Signal HIGH duration (solenoids energized)	t_{act}	typ.	1,2	ms
Signal repetition time	t_{sc}	min.	1,8	ms
		max.	3,3	ms

By varying the signal repetition time t_{sc} the maximum number of characters printed across the paper may be adjusted between 18 and 20.

Time diagram of one character cycle

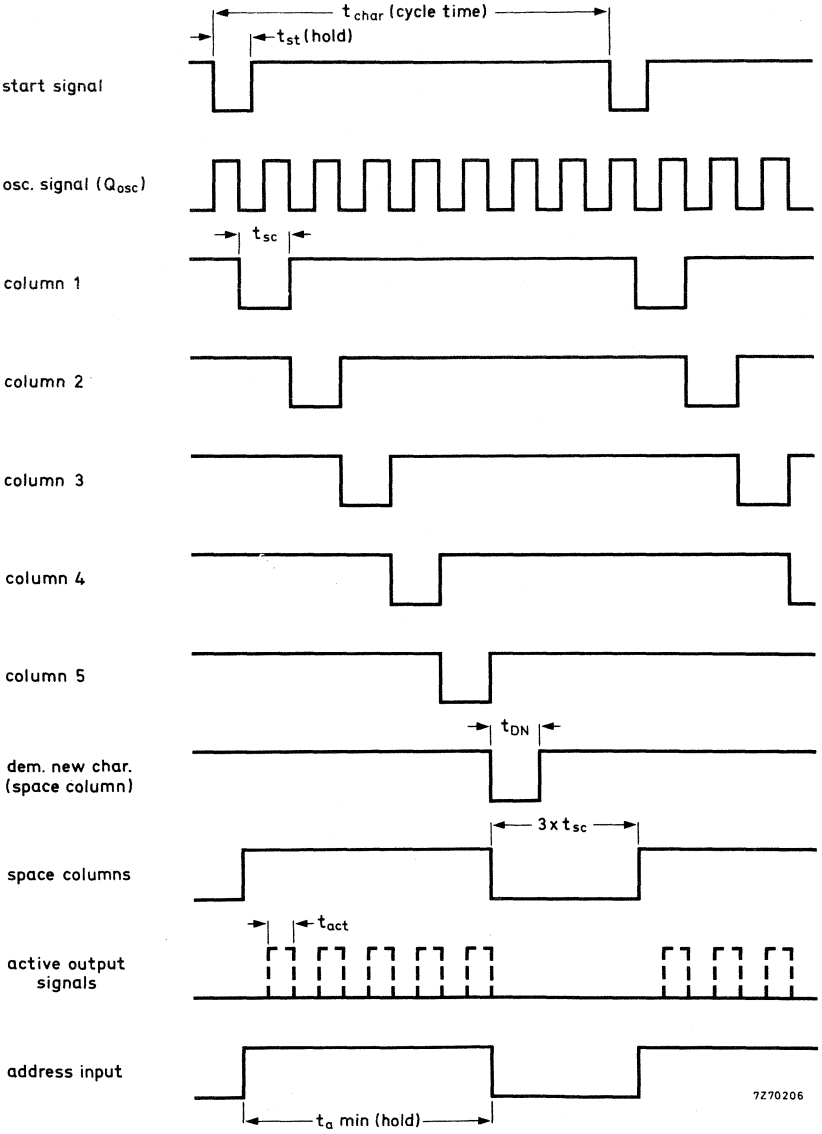
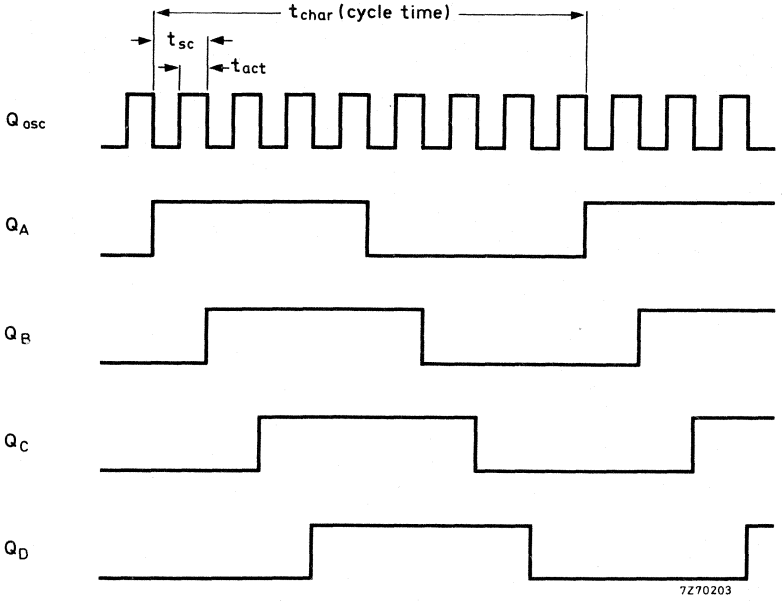


Fig. 6

Time diagram of the column counter outputs (CC64)



See also state table under Static data

Fig. 7

CHARACTER SELECTION GUIDE

The address inputs I_1 to I_6 of the Character Circuit CC64 conform to the USASCII code (except for the sign ≠, this is replaced by £) as given in the table below.

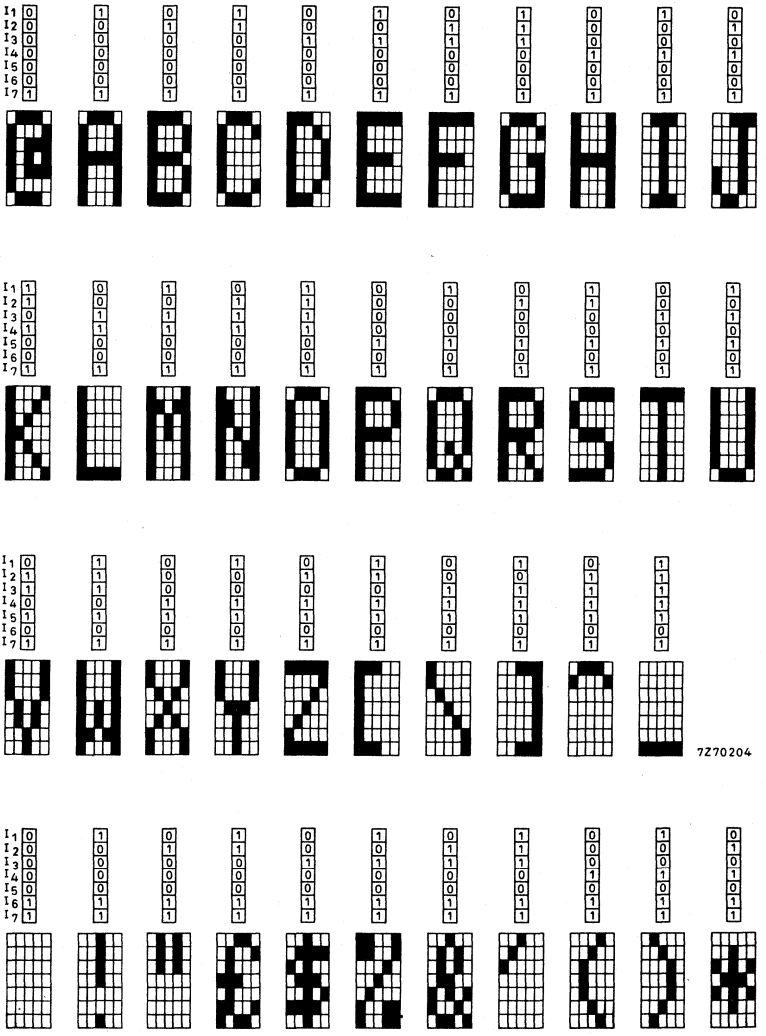
USASCII CODE

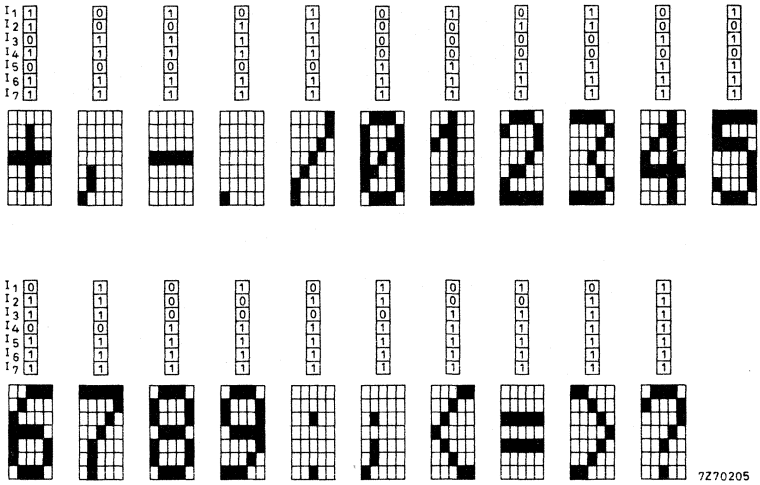
address inputs											
I_1	I_2	I_3	I_4	I_5	I_6	I_5	I_6	I_5	I_6	I_5	I_6
				0	0	1	0	0	1	1	1
0	0	0	0	@		P		space		ϕ	
1	0	0	0	A		Q		!		1	
0	1	0	0	B		R		"		2	
1	1	0	0	C		S		£		3	
0	0	1	0	D		T		$		4	
1	0	1	0	E		U		%		5	
0	1	1	0	F		V		&		6	
1	1	1	0	G		W		'		7	
0	0	0	1	H		X		(		8	
1	0	0	1	I		Y		)		9	
0	1	0	1	J		Z		*		:	
1	1	0	1	K		[		+		;	
0	0	1	1	L		\		,		<	
1	0	1	1	M		]		−		=	
0	1	1	1	N		^		.		>	
1	1	1	1	O		←		/		?	

Logic "1" is the more positive voltage : min. 2 V
Logic "0" is the less positive voltage : max. 0,8 V

CHARACTER PRESENTATION

As already mentioned, each character is built-up within a 5 by 7 dot matrix. The character presentation is shown below. I_1 to I_6 are address inputs, I_7 is the inhibit input.





GENERAL RECOMMENDATIONS

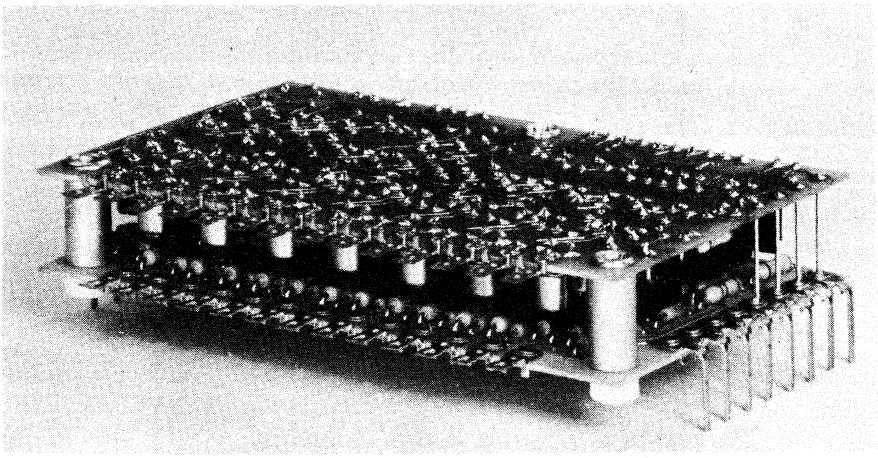
To avoid the effects of any interference pulses on the system it is recommended that each supply terminal (+5 V, +14 V, −14 V, and +24 V) on each panel be connected directly to the relevant supply source. Each 0 V terminal of the CM64, and the 0 V terminals of each supply source, should be connected directly to a central earth point (C.E.P.).
As the connection wire from the power supply to the AC64 has some inductance, it is recommended that a capacitor be connected (approximately 30 μF per meter of wire) between the supply terminals 22 + 23 and 24 + 25 of the AC64 board.

ACCESSORIES

	catalogue number
Printed-wiring connector, type F061 single-sided, 35 contacts	
version for soldering	2422 048 13503
version for wire-wrapping	2422 048 13523
Set of 25 extractors, comprising 25 holders, 100 fixing bushes, 25 text strips, 1 extractor tool	4322 026 38462
Miniature mounting chassis	4322 026 38310

DYNAMIC DRIVE MODULE
for indicator tubes

RZ 28657-5



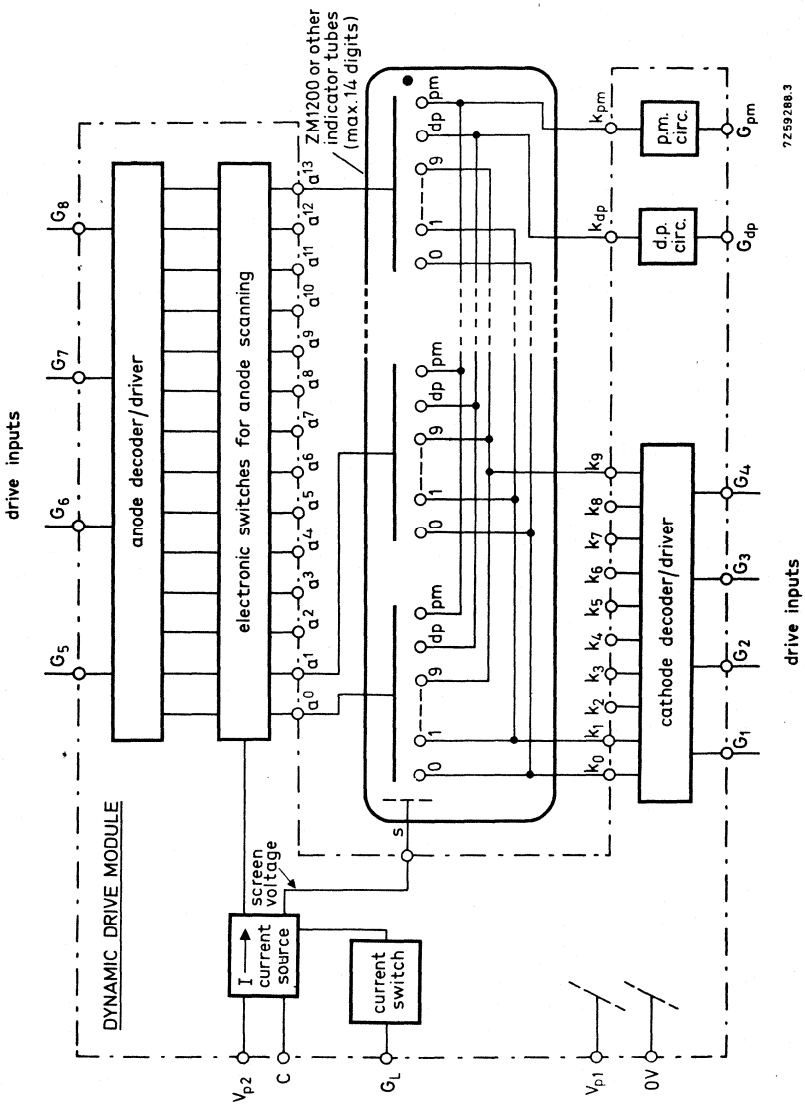
APPLICATION

Dynamic drive of various types of indicator tubes, especially the PANDICON [1]) tubes e.g. ZM 1200 and also a number of single indicator tubes, e.g. ZM 1005 [2]).

[1]) PANDICON - Registered trademark for multiple indicator tubes.

[2]) See Application Information 345 : "Dynamic Drive Module DDM 14 for Cold Cathode Indicator Tubes"

DESCRIPTION



Block diagram of the circuit

Fig. 1

Principle

The identical cathodes of the indicator tubes which are to be driven are connected in parallel. In this way 12 common cathode input lines (numerals 0 to 9, decimal point and punctuation mark) are obtained for all indicator tubes.
A cathode decoder/driver selects one out of the ten cathode lines for the numerals 0 to 9. The input signal for the cathode decoder/driver must be in the 1-2-4-8 code.
The decimal-point cathodes and the punctuation-mark cathodes have their own control circuits (d.p. circuit and p.m. circuit in Block diagram).

The anodes of the various indicator tubes have to be scanned sequentially. For this purpose the 1-2-4-8 code input signal has to be converted into a one-out-of-fourteen code. This is done by means of the anode decoder/driver. Fourteen electronic high voltage switches, connected to the outputs of this decoder, control the anodes of the indicator tubes in sequence.

In other words, the cathode decoder/driver determines what numeral is displayed, while the anode decoder/driver determines where the numeral is displayed.

Operation

Current source

The stabilised current is supplied by a current source, the magnitude of this current being so chosen that the requirements of the PANDICON tube ZM 1200 are met. An external resistor enables the current to be adjusted up to a maximum of 20 mA. Thus, brightness control becomes possible, and in addition a number of single indicator tubes such as the ZM 1005 can be driven.

Current switch (terminal G_L)

The whole display is darkened and consequently the power consumption reduced when the LOW-level is applied to the current switch input G_L. The anode current for the indicator tube(s) is then switched off, resulting in a decrease of power consumption of:

$$\Delta P \approx I_{a\ peak} \times V_{p_2}$$

Blanking

The binary coded signal LHHH(14) or HHHH(15) must be applied to the cathode decoder inputs (G_1 - G_4):

- To blank certain tube positions at will.
- For those positions where the anode switch terminals are left floating.
- When the counter driving the anode decoder/driver does more steps as there are anodes connected (14), but only for the redundant steps.

Moreover, when a sign indicator tube with less than 10 signs (e.g. ZM 1001) is scanned, only the connected cathodes may be selected. In all other cases the blanking code LHHH(14) or HHHH(15) must be applied.

Decimal point circuit and punctuation mark circuit

These circuits drive the decimal point and the punctuation mark separately. When tubes are applied without punctuation mark and decimal point, the outputs of these circuits are left floating.

Circuit protection

The circuit is protected against inadvertent transposition of V_{p_1} and 0V, and V_{p_2} and 0 V, (see also point 6 of next paragraph).
Incidental short-circuits between any of the output terminals or any output terminal and earth (0 V-line) will have no harmful effects on the circuit.

CIRCUIT REQUIREMENTS

Positive logic for all inputs.

1. Cathode decoder/driver

Input conditions: 4 inputs in NBC (1-2-4-8) code
Input voltage levels are compatible with DTL and TTL conditions.

HIGH-level: V_{GH} = 2, 4 to 10 V, I_{GH} = max. 120 µA (3TTL)
V_{GH} = max. 30 V (limiting value)

LOW-level: V_{GL} = 0 to 0, 8 V, $-I_{GL}$ = max. 4, 8 mA at V_{p1} = 5, 25 V, V_{GL} = 0, 4 V
$-I_{GL}$ = max. 5, 4 mA at V_{p1} = 6, 3 V, V_{GL} = 0, 4 V
V_{GL} = min. −4 V (limiting value)

Output conditions: 10 outputs (1 out of 10 "ON")

OFF-state: $V_{k_{off}}$ = min. 70 V, max. 86 V
$\Sigma I_{k_{off}}$ = max. 4 mA (current to non-conducting cathodes)

ON-state: $V_{k_{on}}$ = max. 6 V (at $I_{k_{on}}$ = 20 mA)
$I_{k_{on}}$ = max. 20 mA

2. Anode decoder/driver

Input conditions: 4 input in NBC (1-2-4-8) code
Input voltage levels are compatible with DTL and TTL conditions.

HIGH-level: V_{GH} = 2,4 to 10 V, I_{GH} = max. 80 µA (2 TTL)
V_{GH} = max. 30 V (limiting value)

LOW-level: V_{GL} = 0 to 0,8 V, $-I_{GL}$ = max. 3,2 mA at V_{p1} = 5,25 V, V_{GL} = 0,4 V
$-I_{GL}$ = max. 3,6 mA at V_{p1} = 6,3 V, V_{GL} = 0,4 V
V_{GL} = min. −4 V (limiting value)

Output conditions: 14 outputs (1 out of 14 "ON")

OFF-state: $V_{a_{off}}$ = min. 100 V / max. 120 V
$\Sigma I_{a_{off}}$ = max. 100 µA

ON-state: $V_{a_{on}}$ = V_m of indicator tube + $V_{k_{on}}$
$-I_a$ peak available (C connected to V_{p2}) = 15 to 22 mA
(C not connected to V_{p2}) = 2,5 to 5,5 mA

3. Decimal point and punctuation mark

Input conditions: Input voltage levels are compatible with DTL and TTL conditions.

HIGH-level: V_{dpH}, V_{pmH} = 2,4 to 10 V, I_{iH} = max. 40 µA (1 TTL)
V_{dpH}, V_{pmH} = max. 30 V (limiting value)

LOW-level: V_{dpL}, V_{pmL} = 0 to 0,8 V, $-I_{iL}$ = max. 1,6 mA at V_{p1} = 5,25 V, V_{iL} = 0,4 V
$-I_{iL}$ = max. 1,8 mA at V_{p1} = 6,3 V, V_{iL} = 0,4 V
V_{dpL}, V_{pmL} = min. −4 V (limiting value)

Output conditions:

OFF-state: $V_{kdp_{off}}$, $V_{kpm_{off}}$ = min. 70 V / max. 86 V
$\Sigma I_{k_{off}}$ = 4 mA (current to non-conducting cathodes)

ON-state: $V_{kdp_{on}}$, $V_{kpm_{on}}$ = min. 20 V / max. 25 V (at $I_{kpm_{on}}$ = 2 mA)
$I_{kdp_{on}}$, $I_{kpm_{on}}$ = max. 2 mA

4. Screen

The screen-voltage supply circuit meets the specifications of the screen voltage for the PANDICON tube ZM 1200.

V_{screen} = min. 70 V / max. 86 V
$-I_{screen}$ = max. 0,5 mA

5. Current switch input (G_L)

Input conditions: Input voltage levels are compatible with DTL and TTL conditions. The tube is darkened when the input is at LOW-level.

HIGH-level: V_{GLH} = 2,4 to 10 V, I_{GLH} = max. 40 µA (1TTL)
V_{GLH} = max. 30 V (limiting value)

LOW-level: V_{GLL} = 0 to 0,8 V, $-I_{GLL}$ = max. 1,6 mA at V_{p1} = 5,25 V, V_{GLL} = 0,4 V

$-I_{GLL}$ = max. 1,8 mA at V_{p1} = 6,3 V, V_{GLL} = 0,4 V

V_{GLL} = min. −4 V (limiting value)

6. Power supply

V_{p1} = 4,75 to 6,3 V, I_{p1} = nom. 25 mA at V_{p1} = 5 V
= nom. 30 mA at V_{p1} = 6 V
V_{p1} = max. 10 V (limiting value)
V_{p2} = 200 V ± 5%, I_{p2} = nom. 13 mA
= nom. 25 mA (terminal C connected to V_{p2}), see Note

Note: To maintain the protection against the transposition of V_{p2} and 0 V, a diode (BAX17) has to be connected in series with the current adjusting resistor (anode of the diode to V_{p2}, see also point 8).

7. Ambient temperature range

Operating (T_{amb}), PANDICON ZM 1200	−20° to +70 °C
single tubes at max. current	−20° to +60 °C
Storage	−30° to +85 °C

8. Tube anode current

The anode current is adjustable up to 20 mA by means of an external resistance between terminal C and V_{p2}, see Figs. 2 and 3.

$I_{a\ peak}$, terminal C not connected 5 mA
terminal C connected to V_{p2} 20 mA

9. Duty cycle

Maximum 1 : 6
Minimum 1 : 14 (if blanked during redundant steps, this can be increased)

10. Scanning frequency

Maximum 50 kHz

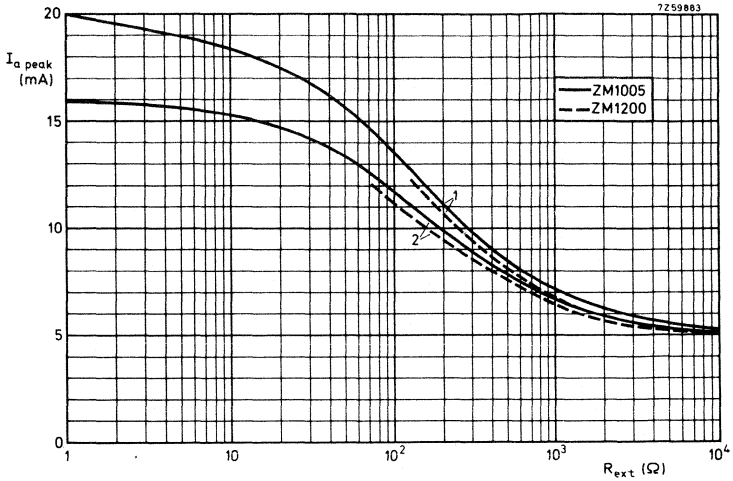


Fig. 2 $I_{a\ peak}$ versus R_{ext} (for measuring circuit, see Fig. 3)
1 = without BAX 17, 2 = with BAX 17
V_{p2} = 200 V, V_{p1} = 5 V, T_{amb} = 25 °C.

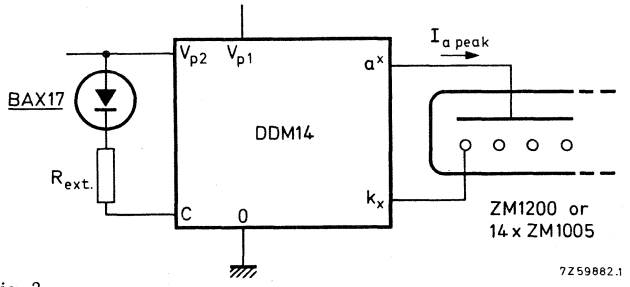


Fig. 3

11. Truth table of anode decoder/driver

G5 1	G6 2	G7 4	G8 8	Anode
L	L	L	L	a0
H	L	L	L	a1
L	H	L	L	a2
H	H	L	L	a3
L	L	H	L	a4
H	L	H	L	a5
L	H	H	L	a6
H	H	H	L	a7
L	L	L	H	a8
H	L	L	H	a9
L	H	L	H	a10
H	H	L	H	a11
L	L	H	H	a12
H	L	H	H	a13

12. Truth table of cathode decoder/driver

G1 1	G2 2	G3 4	G4 8	Cathode
L	L	L	L	k0
H	L	L	L	k1
L	H	L	L	k2
H	H	L	L	k3
L	L	H	L	k4
H	L	H	L	k5
L	H	H	L	k6
H	H	H	L	k7
L	L	L	H	k8
H	L	L	H	k9
L	H	H	H	blanking codes
H	H	H	H	

MECHANICAL DATA

The circuit is mounted on two printed wiring boards stacked with the component sides facing each other.

Both p.w. boards carry the tags for connecting to the indicator tubes at the same side. These tags enable the tube connections to be made either via a cable directly to the tube or via the "mother" p.w. board.

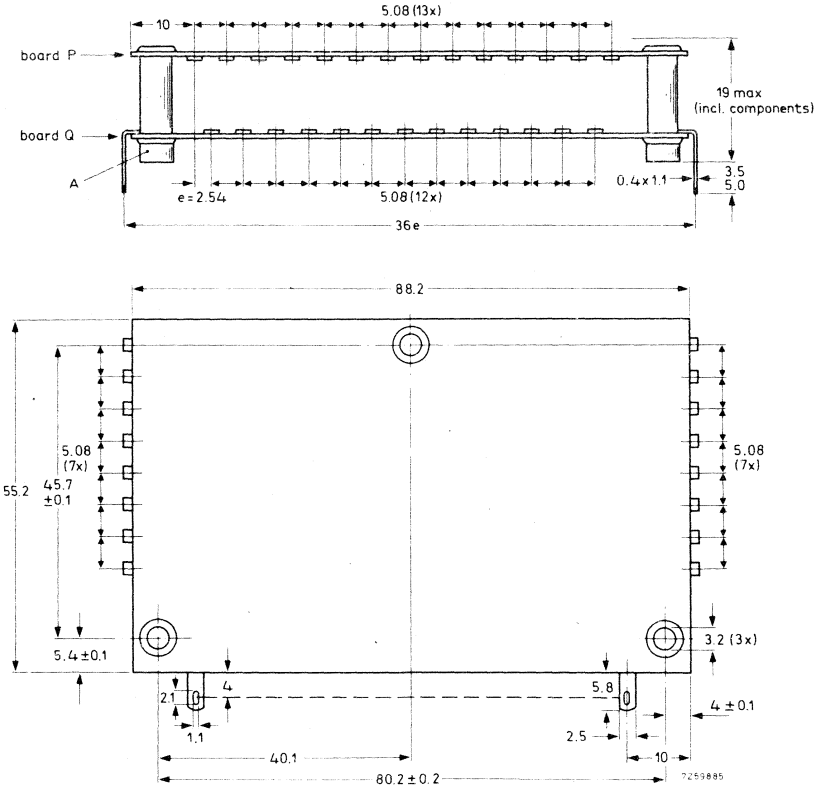
The connections for the supply voltages and the logic signals are made only via the bottom print of the module.

Care is taken that when the module is mounted on a "mother" p.w. board, no short circuits will occur between the bottom print of the module and the "mother" p.w. board.

It is possible to screw the module to, e.g., a front-panel, mounting-holes being provided for the purpose.

The overall dimensions of the module are approx. 91,5 x 61 x 19 mm.

Dimensions in mm



For screw mounting, remove the plastic end-caps A from the studs.

Fig. 4

Terminal configuration

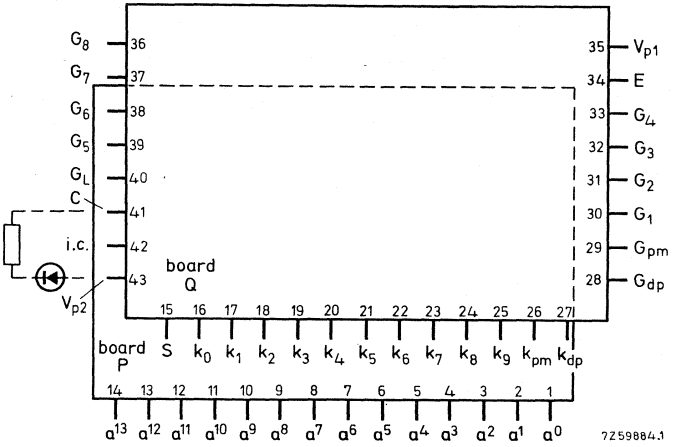


Fig. 5

Terminals:

1 = a^0 = anode ind. tube 1
2 = a^1 = " " " 2
3 = a^2 = " " " 3
4 = a^3 = " " " 4
5 = a^4 = " " " 5
6 = a^5 = " " " 6
7 = a^6 = " " " 7
8 = a^7 = " " " 8
9 = a^8 = " " " 9
10 = a^9 = " " " 10
11 = a^{10} = " " " 11
12 = a^{11} = " " " 12
13 = a^{12} = " " " 13
14 = a^{13} = " " " 14
15 = s = screen of ind. tube
16 = k_0 = cathode line 0
17 = k_1 = " " 1
18 = k_2 = " " 2
19 = k_3 = " " 3
20 = k_4 = " " 4
21 = k_5 = " " 5
22 = k_6 = " " 6
23 = k_7 = cathode line 7
24 = k_8 = " " 8
25 = k_9 = " " 9
26 = k_{pm} = cathode punct. mark
27 = k_{dp} = cathode dec. point
28 = G_{dp} = input dec. point
29 = G_{pm} = input punct. mark
30 = G_1 = 1-input cathode dec.
31 = G_2 = 2-input " "
32 = G_3 = 4-input " "
33 = G_4 = 8-input " "
34 = E = common supply 0V
35 = V_{p1} = supply 4.75 to 6.3 V
36 = G_8 = 8-input anode dec.
37 = G_7 = 4-input " "
38 = G_6 = 2-input " "
39 = G_5 = 1-input " "
40 = G_L = blanking input
41 = C = current adjusting
42 = i.c. = internally connected
43 = V_{p2} = supply (+ 200 V)

TEST SPECIFICATION

The module is designed to meet the tests below.

Shock test according to method 202B of MIL-STD-202C, 3 blows 50 g in 3 perpendicular directions.

Vibration test according to method 201A of MIL-STD-202C.
Frequency 10-55 Hz, amplitude 0.76 mm max., cycle time 1 min, 2 hours in 3 perpendicular directions.

Temperature-cycling test according to method 102A of MIL-STD-202;
5 cycles from −30 to +100 °C.

Long term humidity test according to I.E.C. 68, test C.
Duration 21 days at 40 °C and R.H. = 90 −95 %.

Solderability according to method 210 of MIL-STD-202.

Contents

COUNTER MODULES 50-SERIES

Accessories for counter modules 50-Series

NORBITS 60-SERIES AND 61-SERIES

60-Series NORbits

61-Series NORbits

Accessories for NORbits

CIRCUIT BLOCKS 90-SERIES

INPUT/OUTPUT DEVICES

Power stacks with diodes and/or thyristors

HYBRID INTEGRATED CIRCUITS

PERIPHERAL DEVICES

Argentina: FAPESA I.y.C., Av. Crovara 2550, Tel. 652-7438/7478, BUENOS AIRES.
Australia: Philips Industries Ltd., Elcoma Division, 67 Mars Road, Tel. 42 1261, LANE COVE, 2066, N.S.W.
Austria: Österreichische Philips, Bauelemente Industrie G.m.b.H., Zieglergasse 6, Tel. 93 26 11, A-1072 WIEN.
Belgium: M.B.L.E., 80, rue des Deux Gares, Tel. 523 00 00, B-1070 BRUXELLES.
Brazil: IBRAPE S.A., Av. Paulista 2073-S/Loja, Tel. 278-7144, SAO PAULO, SP.
Canada: Philips Electron Devices, 116 Vanderhoof Ave., Tel. 425-5161, TORONTO 17, Ontario.
Chile: Philips Chilena S.A., Av. Santa Maria 0760, Tel. 39-40 01, SANTIAGO.
Colombia: SADAPE S.A., Calle 19, No. 5-51, Tel. 422-175, BOGOTA D.E. 1.
Denmark: Miniwatt A/S, Emdrupvej 115A, Tel. (01) 69 16 22, DK-2400 KØBENHAVN NV.
Finland: Oy Philips Ab, Elcoma Division, Kaivokatu 8, Tel. 1 72 71, SF-00100 HELSINKI 10.
France: R.T.C., La Radiotechnique-Compelec, 130 Avenue Ledru Rollin, Tel. 355-44-99, F-75540 PARIS 11.
Germany: Valvo, U.B. Bauelemente der Philips G.m.b.H., Valvo Haus, Burchardstrasse 19, Tel. (040) 3296-1, D-2 HAMBURG 1.
Greece: Philips S.A. Hellénique, Elcoma Division, 52, Av. Syngrou, Tel. 915 311, ATHENS.
Hong Kong: Philips Hong Kong Ltd., Components Dept., 11th Fl., Din Wai Ind. Bldg., 49 Hoi Yuen Rd, Tel. K-42 72 32, KWUNTONG.
India: INBELEC Div. of Philips India Ltd., Band Box House, 254-D, Dr. Annie Besant Rd, Tel. 457 311-5, Prabhadevi, BOMBAY-25-DD.
Indonesia: P.T. Philips-Ralin Electronics, Elcoma Division, 'TIMAH' Building, Jl. Jen. Gatot Subroto, Tel. 44 163, JAKARTA.
Ireland: Philips Electrical (Ireland) Ltd., Newstead, Clonskeagh, Tel. 69 33 55, DUBLIN 14.
Italy: Philips S.p.A., Sezione Elcoma, Piazza IV Novembre 3, Tel. 2-6994, I-20124 MILANO.
Japan: NIHON PHILIPS, 32nd Fl., World Trade Center Bldg., 5, 3-chome, Shiba Hamamatsu-cho, Minato-ku, Tel. 03-435-5268, TOKYO.
Korea: Philips Korea Ltd., Philips House, 260-199 Itaewon-dong, Yongsan ku, Tel. 73-7222, C.P.O. Box 3680, SEOUL.
Mexico: Electrónica S.A. de C.V., Varsovia No. 36, Tel. 5-33-11-80, MEXICO 6, D.F.
Netherlands: Philips Nederland B.V., Afd. Elonco, Boschdijk 525, Tel. (040) 79 33 33, NL-4510 EINDHOVEN.
New Zealand: EDAC Ltd., 70-72 Kingsford Smith Street, Tel. 873 159, WELLINGTON.
Norway: Electronica A.S., Vitaminveien 11, Tel. (02) 15 05 90, P.O. Box 29, Grefsen, OSLO 4.
Peru: CADESA, Jr. Ilo, No. 216, Apartado 10132, Tel. 27 73 17, LIMA.
Philippines: ELDAC, Philips Industrial Dev. Inc., 2246 Pasong Tamo, Tel. 86-89-51 to 59, MAKATI-RIZAL.
Portugal Philips Portuguesa S.A.R.L., Av. Eng. Duharte Pacheco 6, Tel. 68 31 21, LISBOA 1.
Singapore: Philips Singapore Private Ltd., Elcoma Div., P.O. Box 340, Toa Payoh Central P.O., Lorong 1, Toa Payoh, Tel. 53 88 11, SINGAPORE 12.
South Africa: EDAC (Pty.) Ltd., South Park Lane, New Doornfontein, Tel. 24/6701-2, JOHANNESBURG.
Spain: COPRESA S.A., Balmes 22, Tel. 329 63 12, BARCELONA 7.
Sweden: ELCOMA A.B., Lidingövägen 50, Tel. 08/67 97 80, S-10 250 STOCKHOLM 27.
Switzerland: Philips A.G., Edenstrasse 20, Tel. 01/44 22 11, CH-8027 ZUERICH.
Taiwan: Philips Taiwan Ltd., 3rd Fl., San Min Building, 57-1, Chung Shan N. Rd, Section 2, P.O. Box 22978, Tel. 5513101-5, TAIPEI.
Turkey: Türk Philips Ticaret A.S., EMET Department, Gümüssuyu Cad. 78-80, Tel. 45.32.50, Beyoglü, ISTANBUL.
United Kingdom: Mullard Ltd., Mullard House, Torrington Place, Tel. 01-580 6633, LONDON WC1E 7HD.
United States: North American Philips Electronic Component Corp., 230, Duffy Avenue, Tel. (516) 931-6200, HICKSVILLE, N.Y. 11802.
Uruguay: Luzilectron S.A., Rondeau 1567, piso 5, Tel. 9 43 21, MONTEVIDEO.
Venezuela: Industrias Venezolanas Philips S.A., Elcoma Dept., Av. Principal de los Ruices, Edif. Centro Colgate, Apdo 1167, Tel. 36.05.11, CARACA

Printed in The Netherlands

9399 261 26501